

A PennWell Publication

# solid state technology

march 1987

TK  
7872  
S4  
S472  
6.30  
no. 3  
1987

UNIVERSITY OF CALIFORNIA

## Silicon Materials Status

\*\*\*\*\*5-DIGIT 9024  
985 59302 0193888 22373 L  
SERIAL SEC.  
UNIV OF CALIFORNIA  
ENG & MATH SCIENCE LIBR  
8270 BOEHLER HALL  
LOS ANGELES CA 90024

SSTEAP(3)(1987)

# Markets & the Technology

a perspective from Dataquest

DB a company of The Dun & Bradstreet Corporation

## Japan's Push into Creative Semiconductor Research: 3-Dimensional ICs

**Since the early 1980s, Japanese semiconductor companies have made a concerted push into creative research programs under the auspices of the Japanese government. Dataquest has identified 30 of these joint**

R&D projects—projects that will have a major impact on the global semiconductor industry by the early 1990s (Table I). They are patterned after the highly successful VLSI Project of 1976–1980, which was organized by the Japanese Ministry of International Trade and Industry (MITI) to develop the 64K DRAM and photolithography equipment. This month we will examine one of these efforts—MITI's Future Electron Devices Project—which may be considered to be Japan's "VLSI Project of the 1980s".

### Future Electron Devices Project

In October 1981, MITI's Agency for Industrial Science and Technology (AIST) organized the Future Electron Devices Project to develop three types of next-generation devices and integrated circuits: 3-D ICs, superlattice devices, and hardened ICs. Budgeted at \$114 million, the 8-year project has assigned to it (on a rotating basis) 300 corporate researchers from 14 company members of the Future Electron Devices R&D Association. A committee of university professors advises AIST on basic research goals. In 1984, the companies were assigned the following research areas:

- 3-D ICs: Matsushita, Mitsubishi, NEC, Oki, Sanyo, Sharp, Toshiba
- Superlattices: Fujitsu, Hitachi, Sony, Sumitomo Electric
- Hardened ICs: Hitachi, Toshiba, Mitsubishi
- Fab & Testing Equipment: Canon, Mitsubishi, Seiko Instrument and Electronics

The project is divided into 3 phases:

- Phase 1 (1981–1984)—multilayer structure and basic process technology,
- Phase 2 (1985–1987)—test element and device design,
- Phase 3 (1988–1990)—functional 3-D ICs and system design.

Currently, half of the researchers are assigned to the 3-D ICs area where MITI believes Japan has a two-year lead. By March 1985, the project had generated 373 technical papers (60% in 3-D ICs) and 282 patents (78% in 3-D ICs).

### 3-Dimensional ICs

Three-dimensional ICs are a major attraction to Japanese companies because of their poten-

tial use in megabit memories, "smart" MPUs (MPUs with lasers), high-speed logic, and complex image sensors with higher densities, faster speeds, and multiple functions. MITI's ultimate goal is to create devices having 8 to 9 layers, but 4 to 5 layers may be more realistic, given interconnect and heat build-up problems. For example, four 1Mb DRAMs could be stacked to develop a faster 4Mb device than could be realized in a one-level 4Mb structure.

Table I—Japanese Government Semiconductor-Related Joint R&D Projects

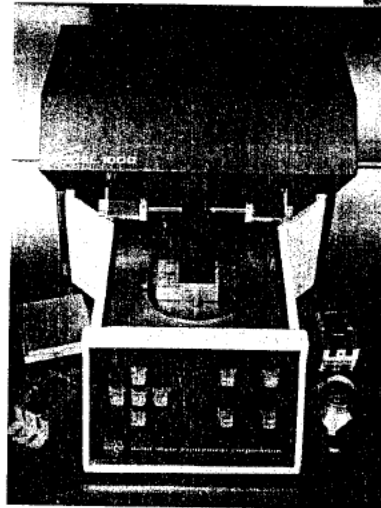
Duration	Budget (\$M)	Agency*	Project
1979-86	112.5	MITI	Optical Measurement and Control Systems
1979-91	375.0	MITI	Fifth Generation Computer
1981-86	11.0	STA	Perfect GaAs Crystals
1981-86	11.0	STA	Nanomechanisms
1981-90	143.7	MITI	Scientific Supercomputer
1981-90	114.0	MITI	Future Electron Devices
1981-90	50.0	MITI	Fine Ceramics
1982-87	10.0	STA	Bioholonics Systems
1983-88	10.0	STA	Bioinformation Transfer
1983-88	N/A	STA	Speech Synthesis and Recognition
1983-90	125.0	MITI	Advanced Robotics (Jupiter)
1984-90	730.0	NTT	Information Network System (INS) Computer
1985-90	N/A	STA	Solid State Surfaces
1985-91	156.3	MITI	Sigma Automated Software Development
1985-90	40.0	MITI	Biochips/Biocomputer
1985-93	N/A	MITI	Next-Generation IC Equipment
1985-88	N/A	Tokyo U.	TRON Project (32-bit MPU)
1985-N/A	23.5	Kyoto U.	Supercomputer (with Matsushita)
1986-96	93.6	MITI	Synchrotron Orbital Radiation (SOR)
1986-96	62.5	MITI	Optoelectronic ICs (OEICs) for Optocomputers
1986-96	625.0	MPT/MITI	Automated Translation Telephone
1986-88	N/A	JIRA	Robot Sensors
1986-88	N/A	MPT	High Resolution TV System
1986-N/A	1.9	MPT/MITI	Electronic Dictionary
1986-N/A	N/A	Tohoku U.	Automotive Electronics and Materials
1987-N/A	N/A	MITI	New Diamond Substrates
1987-89	N/A	9 firms	Mirai IC Card Project (1200 users in Tokyo)
1987-92	26.8	STA	Optical Measurements Technology Development
1987-96	62.5	MITI/MPT NTT/KDD/ NHK	Next-Generation Telecommunication Systems (solid state power amplifiers & transceivers)
1987-96	94.0	MITI	Optical Materials for High-Output Lasers and Optical Fibers

\*MITI = Ministry of International Trade and Industry  
MPT = Ministry of Posts and Telecommunications  
STA = Science and Technology Agency  
NTT = Nippon Telegraph & Telephone (privatized in 1985)  
JIRA = Japan Industrial Robot Association  
NHK = Japan Broadcasting Company  
KDD = Kokusai Denshin Denwa

Source: Dataquest

# What's new in Hermetic Package Sealing?

## The Model 1000



Seals square, rectangular, circular and irregular packages to 6.5 inches. Higher thruput because of increased sealing speeds.

99+% yields using SSEC UNILIDS.

All sealing parameters are programmable by keyboard, self teaching or optional Data Collection/Program Storage Computer.

Storage of up to 400 sealing programs within the system, unlimited storage when used with the optional computer.

User friendly human interface via keyboard and 40 character alpha/numeric display.

Keyboard inside drybox with tactile feedback and spacing optimized for use with drybox gloves.

All drybox system parameters such as moisture level, oxygen level, vacuum oven temperature and pressure, etc. are continuously monitored by microprocessor with audio and display alarm when preset limits are exceeded.

RS-232-C with all handshaking signals is standard.

Optional Data Collection/Program Storage Computer for vacuum bake/sealing documentation and SECS II interface.

Direct digital operation increases reliability due to reduced number of electronic and mechanical components required.

Onboard diagnostics facilitate troubleshooting through keyboard and display.

*Let SSEC's unequalled sealing application experience guide you into the next generation of hermetic sealing equipment... The Model 1000.*



## Solid State Equipment Corporation

1015 Virginia Drive, Fort Washington Industrial Park  
Fort Washington, PA 19034 (215) 643-7900 TWX: 510-661-0197

Fabrication Equipment and Supplies for the Integrated Circuit Industry

WESTERN OFFICE: Sunnyvale, California  
Telephone: (408) 732-5288 TWX: 910-339-9504

EUROPEAN OFFICE: Konstanz, West Germany  
Telephone: 7531/22041 Telex: 73 34 10

INDIA: SMS Associates, New Delhi • Telephone: 670346

During Phase 1, the project explored three basic 3-D process technologies:

- Multilayered silicon-on-insulator (SOI) prepared using either beam annealed recrystallization (electron and laser beam), or low temperature epitaxial growth (CVD, MOCVD, MBE, and ionized beam deposition)
- Multilayered processing using intralayer processes (lithography, etching, doping, deposition, and intraconnection) as well as out-layer processes (planarization, through-hole shield layers)
- Two- and three-layer basic device feasibility

To date, the Future Electron Devices Project has achieved moderate success. In 1985, Mitsubishi announced a 2-layer 256 x 1-bit SRAM and a 1100-gate array using laser-activated polysilicon. Concurrently, NEC fabricated a two-layer 53-stage ring oscillator and a 32-bit dynamic shift register using SOI. Sharp, a leading optoelectronics vendor, has introduced a prototype 5-level video signal processor by planarizing a polyimide-like resin. Matsushita has developed a 3-layer device featuring a CMOS SRAM, a level detector, and an 8-bit photosensor. Perhaps the most significant development, because of its potential for dramatically increasing density levels to 64Mb and beyond, was Toshiba's 3-D IC technology for future 4Mb and 16Mb DRAMs.

At MITI's annual project symposium in 1985, researchers presented a wide variety of papers. Some of these addressed GaAs-on-IC processes, electron beam recrystallized stacked SOI CMOS devices, etch back planarization, and dual laser beam irradiation techniques. Japanese companies are being encouraged to pursue different processes and to develop a variety of 3-D devices.

Mitsubishi Electric became an industry leader in mid-1986 when it announced prototype, large surface, 3-D devices for 16Mb and larger DRAMs. The devices are processed in laser-recrystallized SOI material. Both a three-layer, 256K SRAM and an image processor were test-manufactured using SOI. The recrystallization process on four-inch diameter wafers was accomplished within 20 minutes. Mitsubishi plans to use recrystallized SOI on six-inch wafers in order to develop 16Mb DRAMs and 10,000-gate arrays on 10 mm x 9 mm chips.

### Where are the Japanese Headed?

Pressured by competition from South Korea, Taiwan, and other emerging Asian countries, Japanese companies are rapidly shifting to creative research. MITI's Future Electron Devices Project shows promise in terms of making significant breakthroughs but, as only one project, it represents just the tip of the iceberg. By the late 1980s, we will see a deluge of Japanese semiconductor patents and technical papers flowing from the 30 joint R&D projects, and this will be followed, in the 1990s, by a variety of innovative ICs such as video RAMs, AI processors, and speech chips, etc. For U.S. and European companies seeking to be major players in the future, the challenge is obvious!

—Sheridan Tatsuno  
Senior Industry Analyst