WARPAGE AND MECHANICAL STRENGTH STUDIES OF ULTRA THIN 150MM WAFERS.

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Abstract

Demand for die produced on ultra thin silicon substrates requires improvement in wafer thinning capability, manufacturing equipment substrate handling and packing methodologies. Existing methods typically consider substrates that are nominally flat and relatively thick (254µm to 613µm). The challenge COM 1 faces on several of its product lines, is that they require that the 150mm diameter substrate be thinned to below 150µm. Wafers at this thickness will tend to bow and warp with unpredictable orientation. This is due to the interaction between stresses from the various frontside and backside dielectric and conductive layers together with those induced by the backside grinding and chemical thinning and the reduced ability of the thin silicon substrate to resist these forces. Existing schemes used for smaller wafer diameters (< 100mm) have proven incapable of successfully thinning, handling and transferring these larger substrates to the assembly sites, resulting in high levels of wafer breakage. To enhance survivability during subsequent handling and shipment of ultra-thin 150mm wafers, the understanding of warpage and die strength becomes critical, which is the focus of this paper.

1. Introduction

Semiconductor wafers are routinely thinned prior to dicing to aid the sawing operation and to allow the final assembled package thickness to be minimized. For semiconductor devices required to operate at high power levels, wafer thinning improves the ability to dissipate heat by lowering the die's thermal resistance. The performance of high power RF semiconductor devices can be severely limited by poor thermal dissipation which in turn has driven a demand for wafers thinner than 150µm [1].

As final thickness is decreased the wafer progressively becomes less able to support its own weight and to resist the stresses generated by the process layers on the wafer frontside. The result is a wafer that is no longer flat and tends to bow and warp in a manner that can vary with the means by which it is supported. A thin wafer supported along its edges in a wafer cassette will have a different form to that of one lying on a flat surface. This presents a severe challenge for process and test equipment initially designed to handle flat, full thickness wafers that must perform processing steps on these ultra-thin substrates [2].

While experience exists in handling and processing thin silicon and compound semiconductor wafer diameters of 100mm and less [3] there is very little experience at handling 150mm wafers where wafer bow is much more severe than for a smaller diameter wafer of equivalent thickness.

Maximizing the silicon wafer strength is important as it improves the ability of the thin wafer to survive the mechanical and thermal stress it is subjected to by handling and further processing. Grind processes will induce damage in the wafer backsurface that can lead to crack propagation, growth and fracture. Grind only processes can be optimized for increased strength [4] however a silicon wet etch process is often necessary to completely remove the damaged layer and maximize die strength.

Figure 1. gives a general description of the process steps required between thinning and final testing on the wafer back surface for a typical high power RF device.

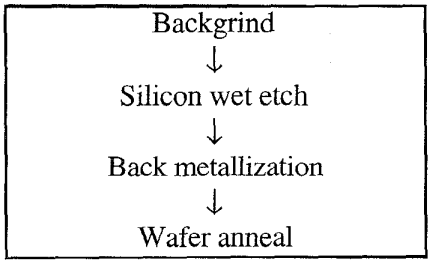

Figure 1.

Wafers with tape applied to their front surface to protect them from mechanical and chemical damage are thinned in the wafer thin operations. The backgrind process utilizes a coarse grind wheel for bulk material removal. This is followed by a fine finishing wheel to reduce the depth of damage induced by the coarse grind. A silicon wet etch removes damaged silicon in a hydrofluoric/

nitric acid based mixture followed by stain removal etches.

After the protective tape is removed the wafer back surface is metallized by coating it with a layer of sputtered gold. A thermal anneal is then required to form a gold-silicon eutectic layer completing the backside processing.

This paper describes efforts to characterize both the strength and deformation of 150mm substrates as a function of the wafer thin process and subsequent processing. This is driven by the need to make such processing manufacturable and to understand how to further decrease the device thickness to improve performance.

2. Die strength

2.1 Experimental and results

A series of 150mm silicon wafers were prepared with differing grind, wet etch and backmetal processing. All wafers had the same nominal final thickness. Die strengths were measured by sawing these wafers into standard 100x100 mil die. The top surface of the individual die were then subjected to a compressive loading, the die strength being the force at which the sample fractured[5].

Wafers described in Figure 2. were prepared in order to investigate the effects of grind finish, wet etch time and back metallization on die strength.

Sample ID	Process
A	Coarse grind only
B	Coarse grind + 3 min. wet etch
C	Fine grind only
D	Fine grind + 1 min. wet etch
E	Fine grind +3 min. wet etch
F	Fine grind only
G	Fine grind + 3 min. wet etch
H	Fine grind + 3 min. wet etch + Gold dep. + anneal
I	Fine grind + Gold dep. + anneal

Figure 2. Backside processing description

2.2 Discussion

Die strength for each wafer thin process are shown in figs 3 and 4. The data is represented by the individual data points plus the "means diamond" which schematically represents the mean (horizontal line) and standard error (upper and lower apex of the diamond) of the sample. Overlapping mean diamonds indicate that to a 95% confidence the sample groups cannot be considered different from each other [6].

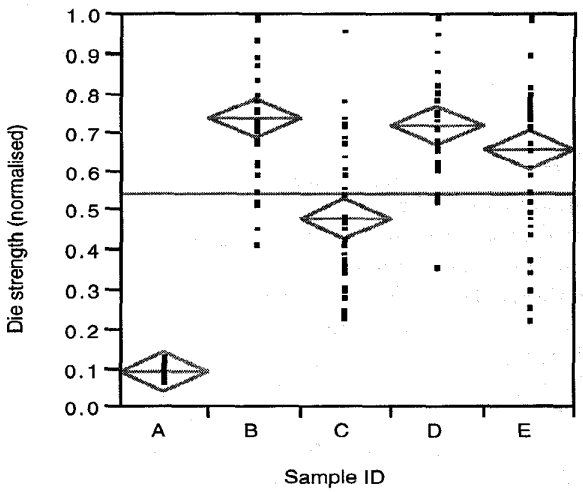

Figure 3. Die strength variation with wafer thinning process.

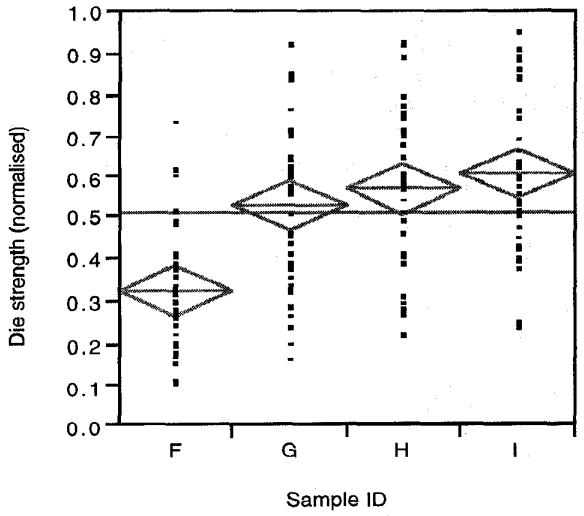

Figure 4. Die strength variation with process flow

Fig. 3 shows that coarse grinding of wafers lead to low die strengths. Fine grinding yielded better results however the highest die strengths for both fine and coarse surfaces could only be achieved with the inclusion of a wet etch. For fine ground surfaces the 3 min. wet etch did not yield an significant improvement over a 1 min. etch.

Fig. 4. shows that the wafer receiving fine grind only had the lowest overall die strength while the three other wafers all had higher but similar levels. The addition of the wet etch increases the strength by removing the grind

induced layer of damaged and deformed silicon however a similar effect has been produced by the formation of the backside gold eutectic layer. This suggests that the eutectic reaction between the silicon and the gold backmetal consumes most of the damaged silicon that contributes to the weakening of the wafer.

3. Wet etch rate

3.1 Experiment and results

In order to understand the depth of damage caused by the grind processes, wafers were ground with both our "coarse" and "smooth" finish processes and wet etched for varying times. The frontsides of the wafers were protected from the etch by a silicon nitride film.

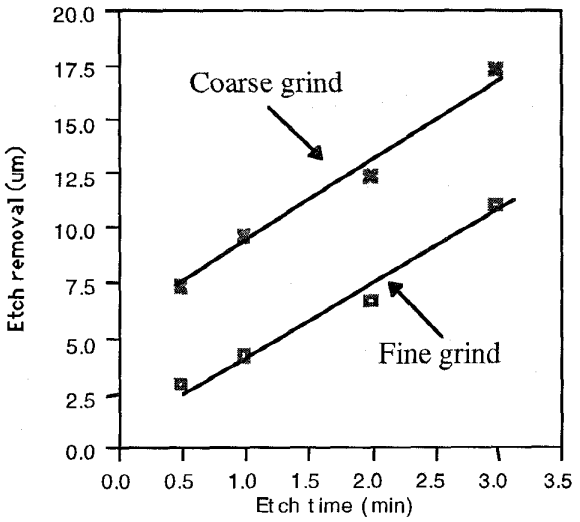

Figure 5. Silicon wet etch removal vs. etch time

3.2 Discussion

The slope of the fitted lines in fig. 5 show that between 0.5 and 3 min. both "coarse" and "fine" samples had similar etch rates. During the initial 30 seconds of the etch however there has been an accelerated removal rate. The thickness of silicon removed during this phase is a measure of the depth of damage being much greater for the coarse ground sample as evidenced by the offset between the two lines. This confirms the data obtained from the die strength testing in that both coarse and fine finishes were significantly strengthened by wet etching but that etch times over 1 min. did not confer additional improvement.

4. Wafer bow

4.1 Experiments and results

Wafer bow was measured using two methods; the first utilized the ability of a cassette to cassette wafer transfer tool to measure the effective thickness (t) of a bowed wafer by sensing the highest and lowest points of its top and bottom surfaces respectively (fig. 6). An alternative technique used a non contact wafer thickness measurement tool which places the bowed wafers over an array of capacitive transducers. Each sensor determines the distance from its surface to the lower surface of the wafer (d_x) and uses the data to map bow across the wafer (fig. 7).

Measurements made by the first method tended to give higher bow as the wafer, supported by its edges was subject to the additional deforming effect of gravity. The second method provided more support for the wafer with gravity tending to flatten out the bow. Both methods gave useful information pertinent to the manner in which wafers were handled in process.

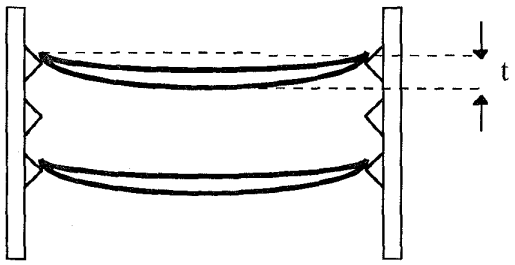

Figure 6. Effective thickness measurement, t

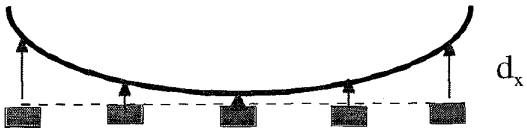

Figure 7. Capactive measurement of wafer bow

4.2 Discussion

In order to understand how both the cumulative film stress generated by wafer processing and the final wafer thickness affect the final wafer bow it is important to consider the theoretical nature of this interaction.

Equation 1. follows from classical plate bending theory [7] and while it relies on a number of initial conditions [8] to be met it has been used successfully to measure thin film stresses[9].

$$\sigma = \frac{E}{6Rt\,(1-\nu)}\, h^2 \quad ....(1)$$

where,

$E/(1-\nu)$ = substrate biaxial modulus (Pa)
h = substrate thickness (m)
t = film thickness (m)
R = radius of curvature of the wafer (m)
σ = film stress (Pa)

The above equation shows that the cumulative film stress is inversely proportional to the induced radius of curvature of the wafer or directly proportional to the wafer bow as bow and radius of curvature are related geometrically to the wafer bow [8] and that the bow of the wafer is inversely proportional to the final substrate thickness. While this equation works best with single unpatterned films it can be used on product wafers where the cumulative effects of processing can be considered to have a single thickness T, and cumulative film stress, σ_T.

It follows that Equation 1. can be simplified to show;

$$\text{Wafer bow} \propto 1/h^2 \quad ....(2)$$

$$\text{Wafer bow} \propto \sigma_T \quad ....(3)$$

Fig. 9 shows how the bow of a fully processed RF bipolar wafers measured after grind varied with its final thickness. The data was fitted using equation (2) and highlights how wafer bow quickly becomes severe as wafer thickness are reduced below 150µm.

The two unfitted data points represent the bow of thinned wafers measured after gold deposition. Both show how the additional film stress has substantially increased the bow. Additional measurements on gold coated wafers thinned to 150µm and below were not made as the bow exceeded the cassette pitch size causing the wafers to wedge in the slot.

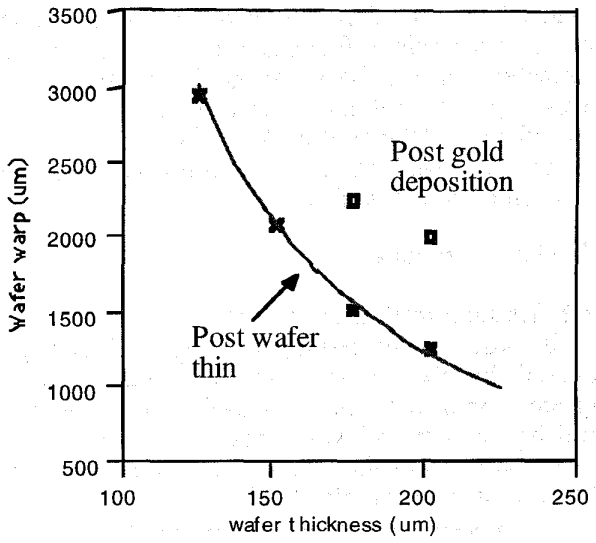

Figure 9. Wafer bow (effective thickness) as a function of wafer thickness.

5. Manufacturability considerations

Ultra thin wafers (<150µm) exhibiting bow of 3000+µm have presented considerable challenges to our wafer processing and handling equipment. The extra effective volume that these wafers occupy mean that standard 25 slot wafer cassettes had to be replaced with larger pitch designs that allow more access between wafers. Materials have also been chosen that resist the tendency of their razor sharp edges produced by the thinning process to cut and wedge into the cassette.

In almost all cases it was necessary to modify process equipment to successfully transfer thin wafers. Handling systems without vacuum to hold the wafer had their 'end effector' or wafer holder re-designed to offer more backside support, minimizing the addition effect gravity can play in increasing bow. The depth of the recess in the end effector was also increased to hold the wafer more securely. In some cases differing handler calibrations were necessary from those used on standard thickness wafers.

Systems utilizing vacuum handling did allow the wafer to be flattened against the end effector thereby reducing its bow. Standard vacuum settings however were often insufficient to pull the wafer down and form a good seal against the end effector while higher levels of vacuum however were shown to locally deform the wafer around the vacuum orifices inducing damage of even fracture of the wafer. Even with optimal vacuum settings there was a finite number of

times that a wafer could withstand repeated vacuum handling operations.

Finally, package and shipping methodologies had to be totally redesigned to assure survival of the wafers sent to our customer base all over the world.

6. Conclusion

Ultra thin wafers (less than 150µm) are critical in meeting package thickness and thermal dissipation requirements for high power RF semiconductor devices. Ultra thin wafers pose new challenges for manufacturing. Die strength, which is critical for survivability, becomes a major concern. The damage induced into the silicon by backgrind must be removed to maximize the die strength. Wet etching through the depth of damage is an effective way for damage removal, whether the backgrind operation uses a course grind only or whether a coarse/fine grind combination was used. Once the depth of damage was removed, additional etch time does not result in a significant increase in die strength. The eutectic reaction formed during gold deposition and anneal is also an effective method for increasing the die strength.

Though the wafer bow and direction can vary greatly in ultra thin wafers, the results indicate, for at least unpatterned wafers, that they follow classical plate bending theory in which the bow is inversely proportional to the square of the wafer thickness and directly proportional to the cumulative film stress. With bows in excess of 3000µm for these ultra thin 150µm diameter wafers, puts considerable challenges to wafer processing and handling equipment. The challenges occur in many areas including cassette design/material selection, wafer support/vacuum handling, and pack/ship methodologies. It is obvious that producing ultra thin 150mm diameter poses some interesting and unusual challenges.

7. Acknowledgments

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References

[1] Norm Dye and Helge Granberg, "Radio Frequency Transistors", Butterworth-Heinemann, 1993.

[2] S.I.Lugosi, R.W.Earle, "Handler Modifications for Ultra thin Wafers", SEMICON West, July 1996.

[3] N.Goto et al.,"Mechanical Thinning of Compound Semiconductor Wafers by Grinding", Sumitomo Electric Review, #33, January 1992.

[4] S.Lewis, "Backgrinding Wafers for Maximum Die Strength", Semiconductor International, July 1992.

[5] B.Hudson, D.Perrin, "The effects of wafer processing on silicon die strength", ISTFA 1990. International Symposium for Testing and Failure Analysis,1990.

[6] JMP®, Copyright© SAS Institute.

[7] G.GStoney, Proc.R.Soc.London Ser.A82, 172 (1909).

[8] J.L.Kawski, J.Flood, "Cumulative thin Film Stresses from Wafer Fabrication Proceses and its Effects on Post Backgrind Wafer Shape", 1993 IEEE/SEMI Advanced Semiconductor Manufacturing Conference.

[9] I.Blech, D.Dang, "Silicon wafer deformation after backside grinding", Solid State Technology, August 1994.