



US005160998A

United States Patent [19][11] **Patent Number:** **5,160,998**

Itoh et al.

[45] **Date of Patent:** **Nov. 3, 1992****[54] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME****[75] Inventors:** Junichi Itoh, Inagi; Kazuyuki Kurita, Yokohama, both of Japan**[73] Assignee:** Fujitsu Limited, Kanagawa, Japan**[21] Appl. No.:** 780,564**[22] Filed:** Oct. 21, 1991**Related U.S. Application Data****[63]** Continuation of Ser. No. 233,108, Aug. 15, 1988, abandoned.**[30] Foreign Application Priority Data**

Aug. 18, 1987 [JP] Japan 62-203483

[51] Int. Cl.⁵ **H01L 29/34****[52] U.S. Cl.** **257/760; 257/633****[58] Field of Search** 357/71, 54, 52, 40, 357/65**[56] References Cited****U.S. PATENT DOCUMENTS**

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Primary Examiner—Andrew J. James*Assistant Examiner*—Sara W. Crane*Attorney, Agent, or Firm*—Nikaido, Marmelstein, Murray & Oram**[57] ABSTRACT**

A semiconductor device including a semiconductor substrate; a metal wiring layer formed on the semiconductor substrate; a first insulation layer formed on the metal wiring layer, the first insulation layer being formed by a tensile stress insulation layer having a contracting characteristic relative to the substrate; and a second insulation layer formed on the first insulation layer, the second insulation layer being formed by a compressive stress insulation layer having an expanding characteristic relative to the substrate. The tensile stress insulation layer is produced by thermal chemical vapor deposition or plasma assisted chemical vapor deposition which is performed in a discharge frequency range higher than 2 megahertz; and the compressive stress insulation layer is produced by plasma assisted chemical vapor deposition which is performed in a discharge frequency range lower than 2 megahertz.

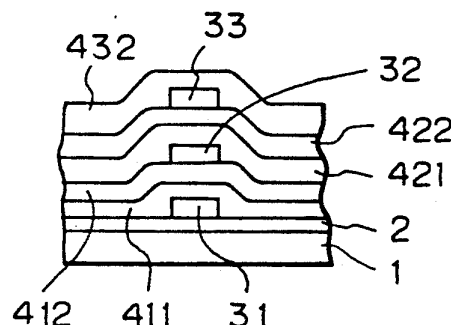
5 Claims, 6 Drawing Sheets

Fig. 1

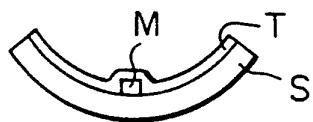


Fig. 2

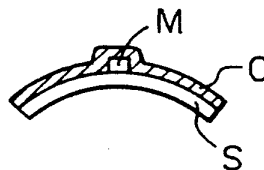


Fig. 3

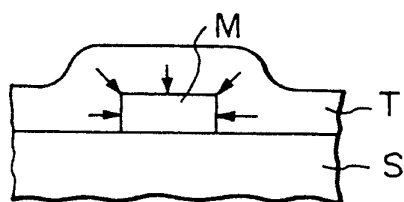


Fig. 4

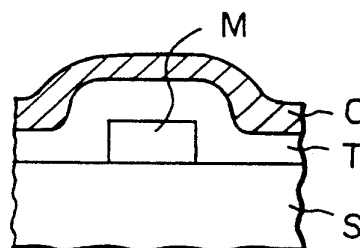


Fig. 6

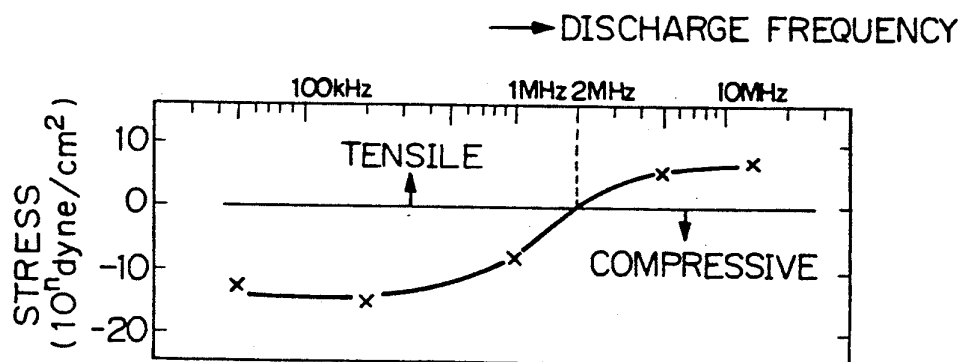


Fig. 5(a)

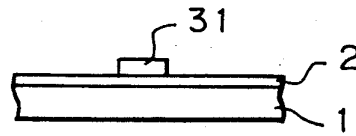


Fig. 5(b)

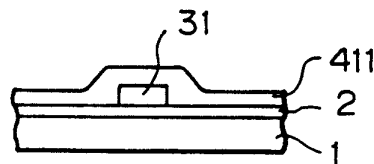


Fig. 5 (c)

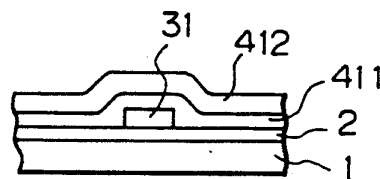


Fig. 5 (d)

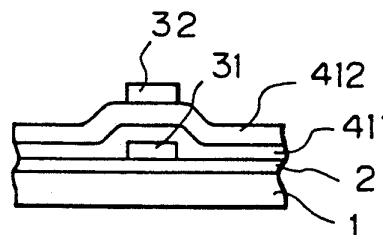


Fig. 5(e)

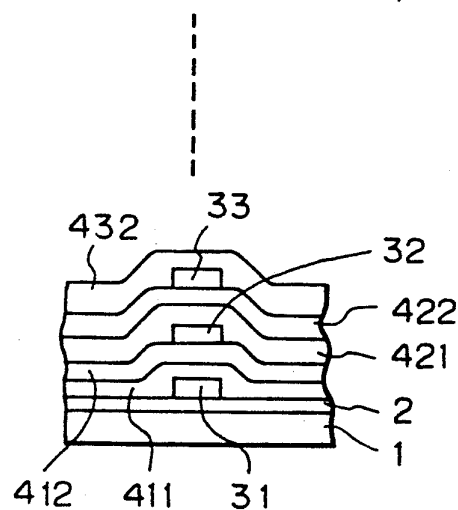


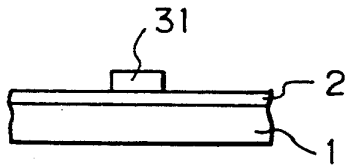
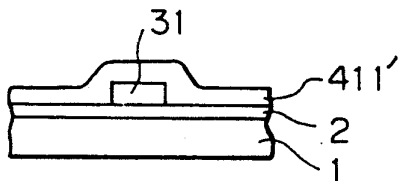
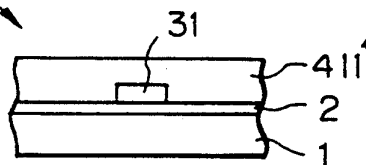
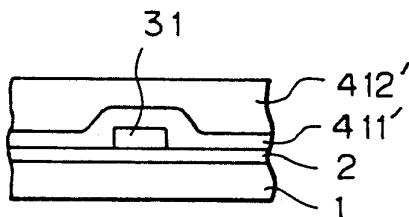
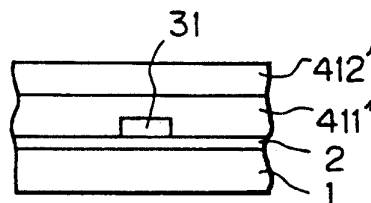
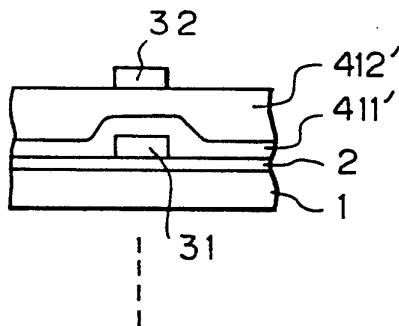
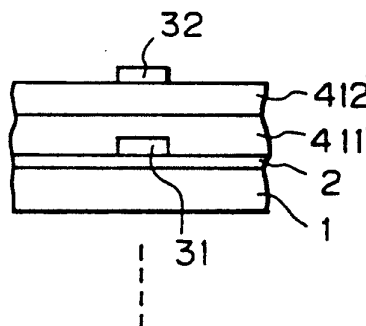
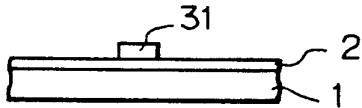
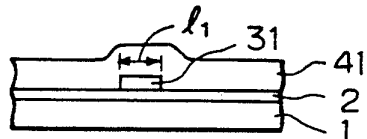
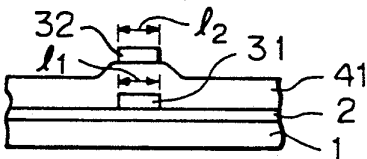
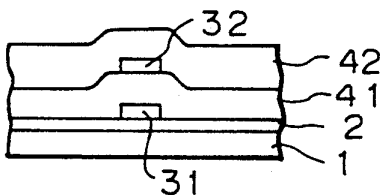
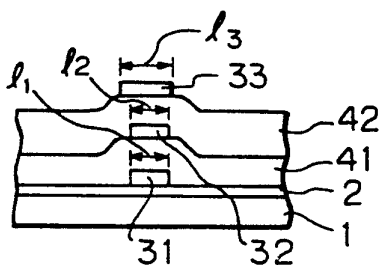
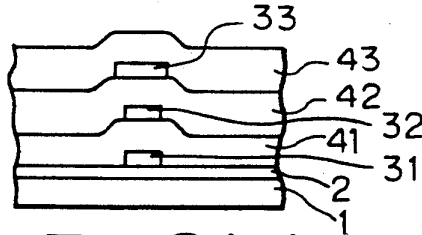
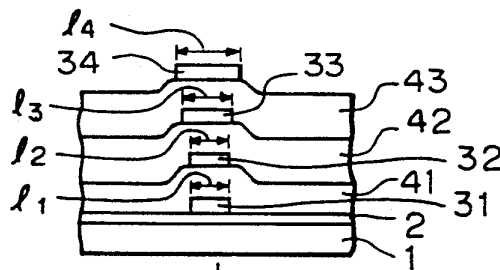
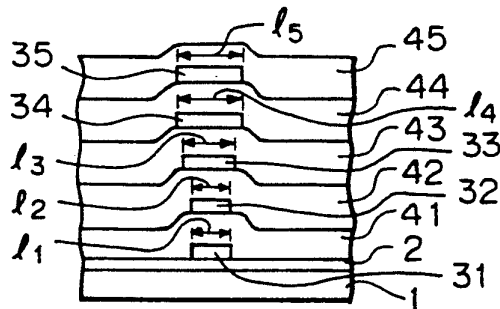
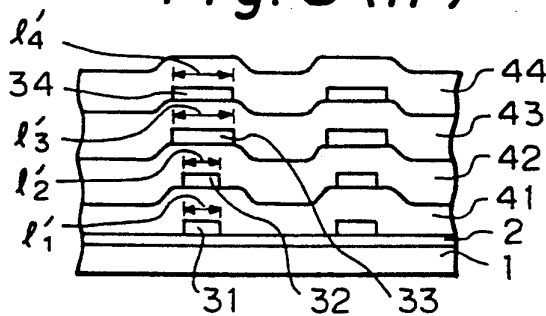
Fig. 7(a)*Fig. 7(b)**Fig. 7(b')**Fig. 7(c)**Fig. 7(c')**Fig. 7(d)**Fig. 7(d')*

Fig. 8(a)*Fig. 8(b)**Fig. 8(c)**Fig. 8(d)**Fig. 8(e)**Fig. 8(f)**Fig. 8(g)**Fig. 8(h)**Fig. 8(h')*

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