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Commissioner for Patents

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**RESPONSE**

Sir:

Responsive to the prior Office Action, please amend this application as follows.

IN THE CLAIMS

1. (Currently amended) An integrated circuit structure comprising:

a first substrate comprising a first surface having interconnect contacts;

a second substrate comprising a first surface having interconnect contacts; and

a bond layer between the first surface of the first substrate and the first surface of the second substrate, comprising:

a plurality of bonds formed from the interconnect contacts of the first surfaces of the first and second substrates and forming portions of signal paths between the first surface of the second substrate and the first surface of the first substrate; and,

at least one bond formed between the first surfaces of the first and second substrates and not forming portions of a signal path between the first surfaces of the first and second substrates, wherein at least one of the first substrate and second substrate is substantially flexible and at least one of the first substrate and the second substrate is a semiconductor substrate.

2. (Currently amended) The structure of claim 1, wherein the second substrate is one of a thinned monocrystalline semiconductor substrate and a thin~~ned~~ polycrystalline semiconductor substrate.

3. (Previously presented) The structure of claim 1, wherein circuitry is formed on the second substrate comprising one of active circuitry and passive circuitry.

4. (Previously presented) The structure of claim 1, wherein circuitry is formed on the second substrate comprising both active circuitry and passive circuitry.

5. (Previously presented) The structure of claim 1, wherein the first substrate is a substrate having circuitry formed thereon.

6. (Previously presented) The structure of claim 5, wherein the circuitry of the first substrate is one of active circuitry and passive circuitry.

7. (Previously presented) The structure of claim 5, wherein the circuitry of the first substrate comprises both active circuitry and passive circuitry.

8. (Previously presented) The structure of claim 1, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

9. (Previously presented) The structure of claim 8, wherein at least two of the first, the second and the at least one additional thinned substrates are formed using a different process technology, wherein the different process technology is selected

from the group consisting of DRAM, SRAM, FLASH, EPROM, EEPROM, Ferroelectric and Giant Magneto Resistance.

10. (Previously presented) The structure of claim 8, wherein at least one of the first, the second and the at least one additional thinned substrates comprises a microprocessor.

11. (Previously presented) The structure of claim 8, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs tests on the at least one substrate that has memory circuitry formed thereon.

12. (Previously presented) The structure of claim 8, wherein at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations, wherein at least one memory location of the plurality of memory locations is used for sparing and wherein data from the at least one memory location on the at least one substrate having memory circuitry formed thereon is used instead of data from a defective memory location on the at least one substrate that has memory circuitry formed thereon.

13. (Previously presented) The structure of claim 8, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs programmable gate line address assignment with respect to the at least one substrate having memory circuitry formed thereon.

14. (Previously presented) The structure of claim 8, further comprising a plurality of interior vertical interconnections that traverse at least one of the first, the second and the at least one additional thinned substrates.

15. (Previously presented) The structure of claim 8, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates.

16. (Previously presented) The structure of claim 8, wherein at least one of the first, the second and the at least one additional thinned substrates has reconfiguration circuitry.

17. (Previously presented) The structure of claim 8, wherein at least one of the first, the second, and the at least one additional thinned substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

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