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First Named Inventor:	Glenn J. Leedy , Parkland, FL (US)	Issue Date of Patent:	-

Title of Invention: Three dimensional structure memory

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Sir:

Responsive to the prior Office Action, please amend this application as follows.

IN THE CLAIMS:

1. (Currently amended) A stacked integrated circuit comprising:

a plurality of substantially flexible integrated circuits having topside and bottom-side surfaces, wherein said integrated circuits are stacked in relation to one another, wherein at least one of the substantially flexible integrated circuits comprises a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting to expose a surface, and subsequently polishing the exposed surface to form a polished surface~~, at least one of said integrated circuits comprising a monocrystalline semiconductor substrate~~; and

interconnections electrically connecting the plurality of substantially flexible integrated circuits, wherein the interconnections are formed only on said surfaces.

2. (Previously presented) The apparatus of claim 1, wherein at least one of the plurality of substantially flexible integrated circuits has a thickness of one of 10 microns or less and 50 microns or less.

3. (Previously presented) The apparatus of claim 1, wherein at least one of the plurality of substantially flexible integrated circuits comprises one of a single crystal semiconductor material and a polycrystalline semiconductor material.

4. (Previously presented) The apparatus of claim 1, wherein the plurality of substantially flexible integrated circuits comprise one of a logic integrated circuit and a memory integrated circuit.

5. (Original) The apparatus of claim 4, wherein the logic integrated circuit is a microprocessor integrated circuit.

6. (Previously presented) The apparatus of claim 1, wherein the plurality of substantially flexible integrated circuits comprise logic integrated circuits.

7. (Previously presented) The apparatus of claim 1, wherein at least two of the interconnections electrically interconnecting the plurality of substantially flexible integrated circuits are vertical interconnections.

8. (Previously presented) The apparatus of claim 1, wherein at least one of the plurality of substantially flexible integrated circuits is formed with a low stress dielectric.

9. (Previously presented) The apparatus of claim 8, wherein the low stress dielectric is at least one of a silicon dioxide dielectric, an oxide of silicon dielectric and caused to have a stress of about 5×10^8 dynes/cm^2 or less.

10. (Previously presented) The apparatus of claim 1, wherein at least two of: at least one of the substantially flexible integrated circuits comprises dielectric having a stress of about 5×10^8 dynes/cm^2 or less; the dielectric is at least one of silicon dioxide and an oxide of silicon; at least one of the substantially flexible integrated circuits has one of logic circuitry and memory circuitry formed thereon; at least one conductive path passes

through a substrate of a substantially flexible integrated circuit and is insulated by an insulation material from said substrate.

11. (Previously presented) The apparatus of claim 1, wherein at least three of: at least one of the substantially flexible integrated circuits comprises dielectric having a stress of about 5 x 10^8 dynes/cm^2 or less; the dielectric is at least one of silicon dioxide and an oxide of silicon; at least one of the substantially flexible integrated circuits has one of logic circuitry and memory circuitry formed thereon; at least one conductive path passes through a substrate of a substantially flexible integrated circuit and is insulated by an insulation material from said substrate.

12. (Previously presented) The apparatus of claim 1, wherein at least four of: at least one of the substantially flexible integrated circuits comprises dielectric having a stress of about 5 x 10^8 dynes/cm^2 or less; the dielectric is at least one of silicon dioxide and an oxide of silicon; at least one of the substantially flexible integrated circuits has one of logic circuitry and memory circuitry formed thereon; at least one conductive path passes through a substrate of a substantially flexible integrated circuit and is insulated by an insulation material from said substrate.

13. (Previously presented) The apparatus of claim 1, comprising at least one conductive path that passes through a substrate of a substantially flexible integrated

circuit and is insulated by an insulation material from said substrate, wherein said substrate is a monocrystalline semiconductor substrate.

14. (Previously presented) The apparatus of claim 1, wherein the bottom-side surface of at least one of the plurality of substantially flexible integrated circuits is polished.

15. (Previously presented) The apparatus of claim 1, wherein data processing is performed by at least two of the substantially flexible integrated circuits in cooperation with one another.

16. (Previously presented) The apparatus of claim 1, further comprising:

a memory array having a plurality of memory cells, a plurality of data lines, and a plurality of gate lines, each memory cell storing a data value and comprising circuitry for coupling that data value to one of said data lines in response to a gate control signal on one of said gate lines;

circuitry for generating a gate control signal in response to an address, including means for mapping addresses to gate lines; and

a controller for determining that one of said memory cells is defective and for altering said mapping to eliminate references to said one of said memory cells.

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