Application Number:	10/672,961
Filing or 371 (c) Date:	09-26-2003
Application Type:	Utility
Examiner Name:	LEWIS, MONICA
Group Art Unit:	2822
Confirmation Number:	9439
Attorney Docket Number:	ELM-2 CONT. 4
Class / Subclass:	438/238
First Named Inventor:	Glenn Leedy , Saline, MI

Title of Invention: Three dimensional multi layer memory and control logic integrated circuit structure

Commissioner for Patents

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RESPONSE

Sir:

Responsive to the Office Action of 10/10/2008, please amend this application as follows.

IN THE CLAIMS

1-87. (Canceled)

88. (Currently Amended) An integrated circuit structure comprising:

a first substrate comprising a first surface having interconnect contacts formed thereon; and

a second substrate comprising a first surface having interconnect contacts formed thereon; and

a thermal diffusion bond between the first surface of the second substrate and the first surface of the first substrate that forms conductive paths between the interconnect contacts of the first surfaces of the first and second substrates, wherein ~~the second substrate is a thinned substrate having circuitry formed thereon, and~~ the first substrate is ~~a comparatively rigid substrate in comparison to~~ at least twice as thick as the second substrate, the first surface of the second substrate overlapping at least a majority of the first surface of the first ~~and second~~ substrate~~s having the same lateral dimensions~~.

89. (Withdrawn) The apparatus of claim 88, wherein the second substrate is one of a thinned monocrystalline semiconductor substrate and a thinned polycrystalline semiconductor substrate.

90. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate is one of active circuitry and passive circuitry.

91. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate consists of both active circuitry and passive circuitry.

92. (Withdrawn) The apparatus of claim 88, wherein the first substrate is a substrate having circuitry formed thereon.

93. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate is one of active circuitry and passive circuitry.

94. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate comprises both active circuitry and passive circuitry.

95. (Previously Presented) The structure of claim 88, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

96. (Withdrawn) The apparatus of claim 95, wherein at least two of the first, the second and the at least one additional thinned substrates are formed using a different process technology, wherein the different process technology is selected from the group consisting of DRAM, SRAM, FLASH, EPROM, EEPROM, Ferroelectric and Giant Magneto Resistance.

97. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates comprises a microprocessor.

98. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs tests on the at least one substrate that has memory circuitry formed thereon.

99. (Withdrawn) The apparatus of claim 95, wherein at least one substrate of the first, the second and the at least one additional thinned substrates has

memory circuitry formed thereon, the memory circuitry having a plurality of memory locations, wherein at least one memory location of the plurality of memory locations is used for sparing and wherein data from the at least one memory location on the at least one substrate having memory circuitry formed thereon is used instead of data from a defective memory location on the at least one substrate that has memory circuitry formed thereon.

100. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs programmable gate line address assignment with respect to the at least one substrate having memory circuitry formed thereon.

101. (Withdrawn) The apparatus of claim 95, further comprising a plurality of interior vertical interconnections that traverse at least one of the first, the second and the at least one additional thinned substrates.

102. (Withdrawn) The apparatus of claim 95, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates.

103. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates has reconfiguration circuitry.

104. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second, and the at least one additional thinned substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video

encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

105. (Withdrawn) The apparatus of claim 95, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling the data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters said mapping to remove references to the one of the plurality of memory cells that is defective.

106. (Previously Presented) The structure of claim 95, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

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