IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Atty. Docket
LEEDY	090316-3DS-II
Serial: 12/405,234	Group Art Unit: 2822
Filed: 03/17/2009	Examiner: Tsz K. Chiu

Commissioner for Patents

P.O. Box 1450

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RESPONSE

Sir:

Responsive to the prior Office Action, please amend this application as follows.

IN THE CLAIMS:

1. (Currently amended) A stacked integrated circuit comprising:

a circuit substrate;

a first integrated circuit having circuitry formed on a front surface thereof, the front surface being bonded to the circuit substrate; and

one or more additional integrated circuits each having circuitry formed on respective front surfaces thereof, each additional integrated circuit being bonded by the front surface thereof to a back surface of an adjacent integrated circuit;

wherein at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and comprises a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface ~~wherein at least one of the first integrated circuit and the one or more additional integrated circuits comprises a monocrystalline semiconductor substrate~~.

2. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, wherein the circuit substrate is an integrated circuit substrate having circuitry formed on a front surface thereof wherein the front surfaces of the integrated circuit substrate and the first integrated circuit are bonded together.

3. (Original) The apparatus of claim 2, further comprising a thermal diffusion bond joining the integrated circuit substrate and the first integrated circuit.

4. (Original) The apparatus of claim 2, further comprising thermal diffusion bonds joining each additional integrated circuit to an adjacent integrated circuit.

5. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising a second integrated circuit and vertical interconnects connecting circuitry of the first integrated circuit and circuitry of the second integrated circuit, wherein a plurality of interconnects are closely arrayed to form a group of interconnects.

6. (Original) The apparatus of claim 5, wherein a group of interconnects extends continuously between multiple integrated circuits.

7. (Original) The apparatus of claim 5, wherein the interconnects are formed at least in part by a thermal diffusion bond.

8. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, wherein the first integrated circuit and the additional integrated circuit are formed with one of single crystal semiconductor material and polycrystalline semiconductor material.

9. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising a second integrated circuit, wherein one of the first and additional integrated circuits are formed using a different process technology than another of the first and second integrated circuits, the different process technology being selected from a group consisting of DRAM, SRAM, FLASH, EPROM, EEPROM, Ferroelectric and Giant Magneto Resistance.

10. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, wherein at least one of the first and additional integrated circuits comprises a microprocessor.

11. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising at least one memory integrated circuit and at least one logic integrated circuit, wherein the at least one logic integrated circuit performs testing of the at least one memory integrated circuit.

12. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising at least one memory integrated circuit having multiple memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one memory integrated circuit is used instead of data from a defective memory location on the at least one memory integrated circuit.

13. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising at least one memory integrated circuit and at least one logic integrated circuit, wherein the at least one logic integrated circuit performs programmable gate line address assignment with respect to the at least one memory integrated circuit.

14. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, wherein a plurality of interior vertical interconnections traverse at least one of the integrated circuits.

15. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising a second integrated circuit, wherein continuous vertical interconnections connect circuitry of the first and second integrated circuits.

16. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising a second integrated circuit, wherein information processing is performed on data routed between circuitry on the first and second integrated circuits.

17. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, wherein at least one integrated circuit has reconfiguration circuitry.

18. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising at least one logic integrated circuit having logic for performing at least one of the following functions: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

19. (Currently amended) The apparatus of ~~claim 1,~~ claim 41, further comprising:

a memory array having a plurality of memory cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell storing a data value and comprising circuitry for coupling that data value to one of said data lines in response to a gate control signal on one of said gate lines;

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