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I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE ON THE DATE SHOWN BELOW.

Name of person signing certification: Sharon E. Ryan

Date: 9/11/98 Signature: Sharon E. Ryan

Attorney's Docket No. 008442-057

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#12
Response
FJ
9-11-98

In re Patent Application of	)	
	)	
Glenn J. Leedy	)	Group Art Unit: 2822
	)	
Application No.: 08/835,190	)	Examiner: Collins, D.
	)	
Filed: April 4, 1997	)	
	)	
For: THREE DIMENSIONAL STRUCTURE MEMORY	)	
	)	

RESPONSE UNDER 37 C.F.R. §1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The following remarks are responsive to the Office Action of August 21, 1998.

REMARKS

The Office Action of August 21, 1998 has been carefully considered. Reconsideration and allowance of the application in view of the following Remarks is respectfully requested.

The Office Action states in Paragraph 5 thereof, "Applicant's arguments with respect to claims 1, 3-23, 25-30, and 62-107 have been considered but are moot in view of the new ground(s) of rejection. New references disclosing multilayer interconnection systems have been added."

In other respects the Office Action would appear to be substantially the same as the

previous Office Action of January 28, 1998. Applicant submits that the newly-cited references of Miller and Bureau (cited by Applicant in the Disclosure Statement of September 19, 1997) are not especially germane to the claimed invention, nor is Finnila, cited by Applicant in a subsequent disclosure statement of July 23, 1998. Applicant further maintains that the claimed invention is not taught or suggested by Yasumoto, for reasons set forth hereafter.

First in regard to Miller, Miller does not relate to the stacking of integrated circuit wafers but rather relates to stacking of *printed circuit board modules*. Note, for example, col. 3, lines 47-54:

> Fig. 5 is a perspective view of a stack comprising identical modules 10-1, 10-2 and 10-3 mounted on mother board 20, with connectors 50 serving both as spacers and as means for interconnecting opposing connecting areas on the modules and mother board. Such connectors can be the stacking connectors or elastomeric connectors described above, or other suitable connectors.

Bolting together printed circuit boards as in Miller is far afield from the claimed invention.

In regard to Bureau, Bureau discloses depositing a layer of polyimide onto a substrate (column 4, last sentence). A multi-layer metal/polymer electrical interconnection system is then built up layer by layer. Chips are then installed to form a 2-D circuit structure. Multiple 2-D structures may be joined to form a 3-D circuit structure using an intervening "stencil" or frame. As illustrated in the figures of Bureau, the stencil surrounds each individual chip. Although not mentioned in Bureau, typically with such a structure an underfilling technique would be used in which a resin is injected so as to fill the remaining spaces between the chips and stencil and the polymeric substrate. Such underfilling is typically required to overcome the effects of CTE (coefficient of thermal expansion) mismatch. Bureau fails to teach or suggest the claimed invention.

Furthermore, Finnila, cited by Applicant fails to teach or suggest the claimed invention.

Finnila teaches forming a silicon device layer on top of an insulating layer (so-called Silicon-On-Insulator, or SOI); i.e., Finnila uses SOI substrate processing techniques to achieve an isolated semiconductor layer on a rigid, standard-thickness substrate. He subsequently thins the substrate, but always keeps the thinned substrate bonded to a rigid substrate, such as the temporary substrate (26) or the permanent substrate (structure 1 or 42).

In Finnila, all device processing (thermal oxide formation, doping, annealing, contact drive-in, etc.) is performed before the SOI substrate is thinned. The only steps that Finnila performs after the SOI substrate is thinned are metallization and dielectric deposition processing. It should be made clear that although he says that "conventional processing steps" (5:31-36) are used, these steps are highly restricted due to the requirement that processing temperatures be limited to less than 132°C, which is the melting point of Indium. Furthermore, based on typical characteristic of available waxes, the "wax" or bonding layer (24, 5:4-5) used to temporarily hold the SOI wafer for thinning and backside processing has a maximum temperature of 200°C. Applicant knows of no waxes that would be compatible with vacuum processing of dielectric deposition or vacuum dry etching (called RIE) due to outgassing (which would cause the temporarily restrained substrate to delaminate from the holding substrate 26) or temperature (typically in excess of 350°C for oxide and nitrides). Presumably, Finnila is using spin-on glass dielectric with very low curing temperatures and wet etch processing. The aluminum film of the aluminum I/O bond pads applied to the last circuit layer necessary for wiring bonding (5:34-35), however, can only be deposited through a sputtering process step which is a vacuum process step; Applicant knows of no "wax" which can withstand vacuum processing without outgassing which would delaminate the thinned substrate.

Finnila does not indicate a need to use low-stress dielectrics. Furthermore, the dielectrics he is using (thermal oxide or spin-on glass) are known to have very high compressive stresses in excess of 1×10^{10} dynes cm^2, which would be sufficient to cause the semiconductor layer to delaminate from the "wax" or the Indium bump with epoxy underfill.

Serious doubt is therefore cast on the workability of Finnila.

Unlike Miller and Bureau, Finnila does teach forming an interconnect that passes through a semiconductor substrate. In other respects, however, the method of Finnila is far different from that of the present invention. Finnila does not teach or suggest the claimed sequence of bonding two substrates by thermal diffusion bonding, thinning one of the bonded substrates, and performing backside processing of the thinned substrate to form pass-throughs and contacts. Moreover, Finnila contains no suggestion of forming a semiconductor memory controller on one substrate and a semiconductor memory array on a separate substrate as recited in Claim 1.

Hence, none of the foregoing references lends substantial strength or support to the primary reference, Yasumoto.

As explained in the previous response, the bonding and interconnect methods, especially, of the invention of Claim 1 are far different from those of the prior art. In accordance with the invention, bonding occurs by thermal diffusion bonding. As described in the specification, various metals commonly used in semiconductor processing are particularly amenable to thermal diffusion bonding in which complementary surfaces are bonded together through the application of heat and pressure. A requirement for thermal diffusion bonding is that the complementary surfaces be highly planar. This degree of planarity is achieved using a semiconductor processing technique of only recent origin known as Chemical Mechanical Polishing, or CMP. The materials and methods used to perform thermal diffusion bonding as described and claimed are fully compatible with existing semiconductor processing techniques. Hence, a bonding step may be followed by further semiconductor processing, which may in turned be followed by a further bonding step, etc. A three-dimensional device stack having a large number of device layers may thereby be produced. Furthermore, three-dimensional processing is performed *at the wafer level* as opposed to at the chip level. The number of work pieces to be handled is therefore greatly reduced, typically several hundred-fold, as compared to three-dimensional processing techniques performed at the chip level.

Yasumoto performs bonding together of *finished chips* to form three-dimensional structures. (Yasumoto, col. 10, lines 6-17; col. 13, lines 38-40.) Further conventional semiconductor processing steps (which are invariably performed in wafer form) are not contemplated, but rather are precluded. In Yasumoto, bonding depends upon an adhesive resin layer. This layer is intended to address the planarity problem, which could not have been addressed by CMP, since the reference predates by nearly a decade the advent of CMP. (The use of such adhesive resin layers would, by itself, be likely to preclude further conventional semiconductor processing of a three-dimensional structure in that such layers cannot, in general, tolerate the high levels of heat associated with typical semiconductor processes.)

Also in accordance with the invention, interconnects are formed that pass entirely through whole substrates. This interconnect structure is referred to in the specification as fine-grain vertical interconnect. As further described in the specification, such fine grain vertical interconnects are formed by *thinning* and *backside processing* of a preceding substrate and *complementary frontside processing* of a succeeding substrate. (Specification, page 15, step 3), followed by bonding of the backside and complementary frontside. This sequence may be repeated an arbitrary number of times to produce a stacked IC of 10 layers, 20 layers or more.

With the exception of Finnila, none of the references teach or suggests an interconnect that passes through a substrate. Accordingly, all of the references are limited to two circuit layers where those circuit layers are formed *within* a substrate. Yasumoto (col. 12, lines 60-64) alludes to the possibility of a three-dimensional semiconductor structure having four or more multilayer structure portions obtained when two or more of the multilayer structural portions 118 are provided between two outer multilayer structural portions 24 and 24'. The intermediate circuit layers of such a structure, however, are not formed *within* a substrate but rather are thin-film transistor layers formed *on* a substrate with the substrate being subsequently removed. (Yasumoto, Figure 7 and 8. Interconnects 112 and 134 pass through a TFT device layer but do not pass through a substrate, the substrate having been removed.) Only in the case of the two outer multilayer structural portions 24 and 24' is the circuit layer

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