IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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First Named Inventor:	Glenn J. Leedy , Carmel, CA (US)	Issue Date of Patent:	-
Entity Status:	Small	AIA (First Inventor to File):	No

Title of Invention: Three dimensional structure memory

RESPONSE

Sir:

Responsive to the prior Office Action, please amend this application as follows.

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IN THE CLAIMS

1. (Currently amended) A thin and substantially flexible ~~substrate~~ structure comprising:

a thin, substantially flexible semiconductor layer of one piece; and

a dielectric layer formed on the semiconductor layer and having a stress of about 5×10^8 dynes/cm^2 tensile or less.

2. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 1, further comprising:

a vertical interconnect conductor extending vertically through the semiconductor layer; and

a vertical dielectric insulator extending vertically through the semiconductor layer and around the interconnect conductor and having a stress of about 5×10^8 dynes/cm^2 tensile or less.

3. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, wherein:

the thin semiconductor layer includes vertical holes etched therethrough; and

the vertical interconnect conductors and the vertical dielectric insulators are formed in the vertical holes of the thin semiconductor layer.

4. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, wherein the thin semiconductor layer comprises monocystalline silicon.

5. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, wherein the thin semiconductor layer is formed from a semiconductor wafer.

6. (Canceled)

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7. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2~~6~~, wherein the thin and substantially flexible substrate has a thickness of 50 microns or less.

8. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 5, wherein the semiconductor wafer comprises monocrystalline silicon, and the thin semiconductor layer comprises monocrystalline silicon from the semiconductor wafer .

9. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, wherein the thin semiconductor layer is unitary.

10. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, wherein the thin semiconductor layer extends from edge to edge of the thin and substantially flexible substrate.

11. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 10, wherein the dielectric layer extends from edge to edge of the thin and substantially flexible substrate.

12. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 6, wherein the thin semiconductor layer comprises a polished surface formed by removing material during thinning of the thin semiconductor to expose a surface thereof and then polishing the exposed surface.

13. (Currently amended) The thin and substantially flexible ~~substrate of~~structure of Claim 2, further comprising:

a bottomside surface and a topside surface;

a contact formed on the bottomside surface and electrically connected to the vertical interconnect conductor; and

an interconnect, contact or circuit formed on or near the topside surface and electrically connected to the vertical interconnect conductor;

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wherein the interconnect, contact or circuit is electrically connected to the contact on the bottomside surface via the vertical interconnect.

14. (Currently amended) A thin and substantially flexible circuit comprising:

a thin semiconductor layer of one piece;

a dielectric layer formed on the semiconductor layer and having a stress of about 5 x 10^8 dynes/cm^2 tensile or less; and

circuitry ~~formed within~~supported by the thin semiconductor layer and the dielectric layer defining an integrated circuit die having an area, wherein the thin semiconductor layer extends throughout a substantial portion of the area of the integrated circuit die.

15. (Previously presented) The thin and substantially flexible circuit of Claim 31, wherein:

the thin semiconductor layer includes vertical holes etched therethrough; and

the vertical interconnect conductors and the vertical dielectric insulators are formed in the vertical holes of the thin semiconductor layer.

16. (Previously presented) The thin and substantially flexible circuit of Claim 31, wherein the thin semiconductor layer comprises monocystalline silicon.

17. (Previously presented) The thin and substantially flexible circuit of Claim 31, wherein the thin semiconductor layer is formed from a semiconductor wafer.

18. (Canceled)

19. (Currently amended) The thin and substantially flexible circuit of Claim 31~~18~~, wherein the thin and substantially flexible substrate has a thickness of 50 microns or less.

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20. (Previously presented) The thin and substantially flexible circuit of Claim 17, wherein the semiconductor wafer comprises monocrystalline silicon, and the thin semiconductor layer comprises monocrystalline silicon from the semiconductor wafer .

21. (Previously presented) The thin and substantially flexible circuit of Claim 31, wherein the thin semiconductor layer is unitary.

22. (Previously presented) The thin and substantially flexible circuit of Claim 31, wherein the thin semiconductor layer extends from edge to edge of the thin and substantially flexible substrate.

23. (Previously presented) The thin and substantially flexible circuit of Claim 22, wherein the dielectric layer extends from edge to edge of the thin and substantially flexible substrate.

24. (Currently amended) The thin and substantially flexible circuit of Claim ~~18~~24, wherein the thin semiconductor layer comprises a polished surface formed by removing material during thinning of the thin semiconductor to expose a surface thereof and then polishing the exposed surface.

25. (Previously presented) The thin and substantially flexible circuit of Claim 31, further comprising:

a bottomside surface and a topside surface;

a contact formed on the bottomside surface and electrically connected to the vertical interconnect conductor; and

an interconnect, contact or circuit formed on or near the topside surface and electrically connected to the vertical interconnect conductor;

wherein the interconnect, contact or circuit is electrically connected to the contact on the bottomside surface via the vertical interconnect.

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