

[54] TRENCH METHOD FOR THREE DIMENSIONAL CHIP CONNECTING DURING IC FABRICATION

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[21] Appl. No.: 239,281

[22] Filed: May 6, 1994

[51] Int. Cl.⁶ H01L 21/44

[52] U.S. Cl. 438/459; 438/152; 438/667; 438/107

[58] Field of Search 437/203, 915, 437/208, 209; 148/DIG. 164

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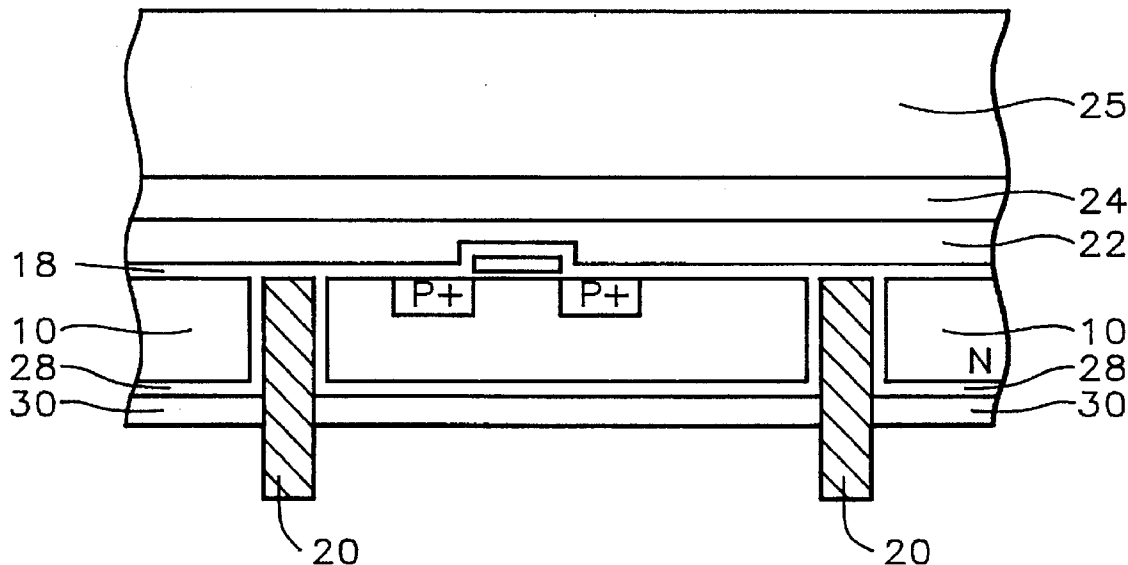
Primary Examiner—George Fourson

33 Claims, 6 Drawing Sheets

Assistant Examiner—C. Everhart
Attorney, Agent, or Firm—William H. Wright

[57] ABSTRACT

A new method of connecting three-dimensional integrated circuit chips using trench technology is described. Semiconductor device structures are provided in and on the top side of a semiconductor substrate of a first and a second three-dimensional integrated circuit chip. Deep trenches are etched into the first semiconductor substrate. A conductive material is deposited into the trenches. An insulating material is deposited over the surface of the substrate, polished and planarized. The bottom side of the first semiconductor substrate is ground, polished, and selectively etched so that the deep trenches form protrusions from the bottom surface. A passivation layer and a polyimide layer are deposited on the bottom surface of the first semiconductor substrate and etched away around the protrusions. A passivation layer and a polyimide layer are deposited over the top surface of the second semiconductor substrate. Connection windows are etched through the two layers to the top conducting surface of the second semiconductor substrate. The first and second integrated circuits are aligned so that the protrusions on the bottom surface of the first integrated circuit chip fit into the connection windows in the top surface of the second integrated circuit chip. The polyimide layer on the bottom surface of the first integrated circuit contacts the polyimide layer on the top surface of the second integrated circuit completing the connection between the two chips.



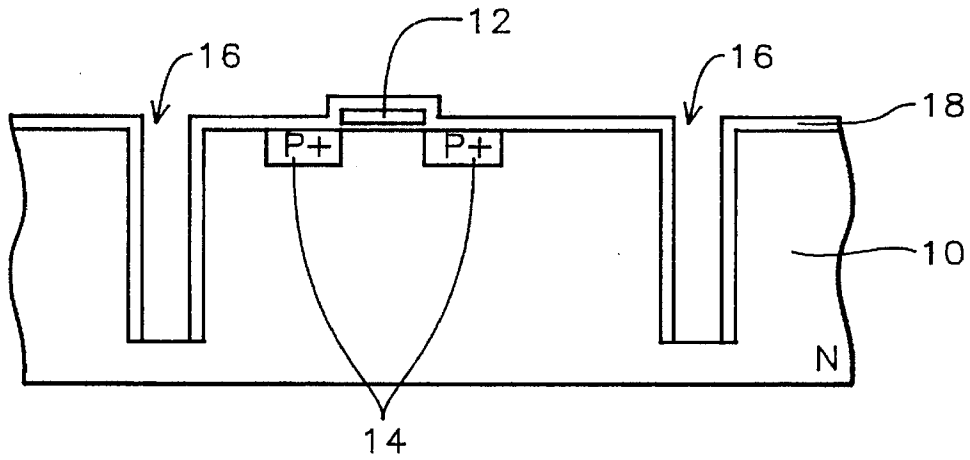


FIG. 3

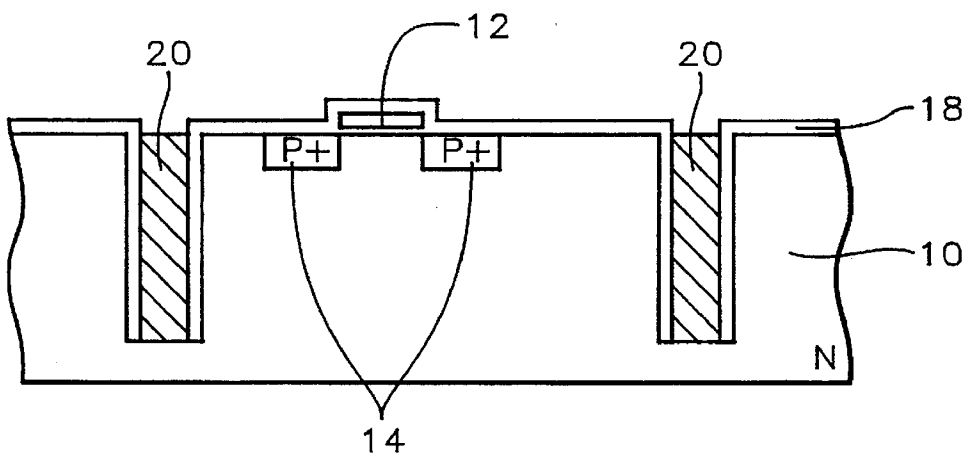


FIG. 4

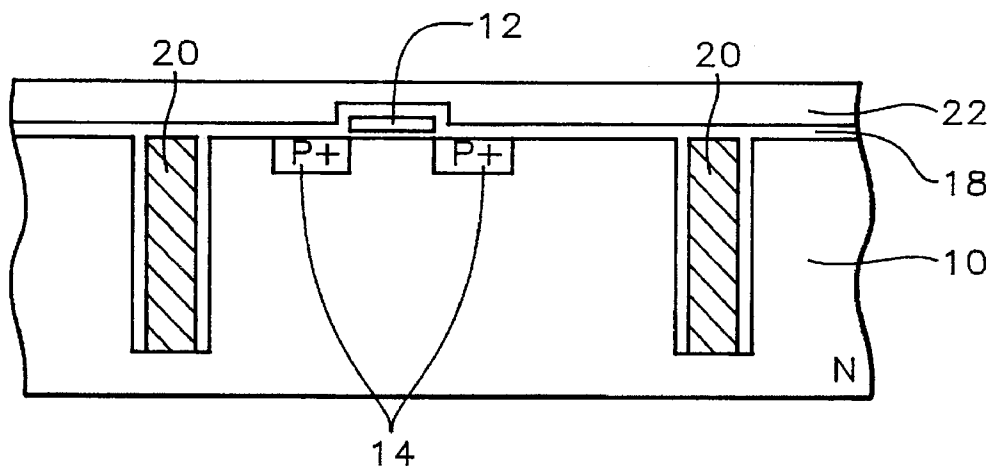


FIG. 5

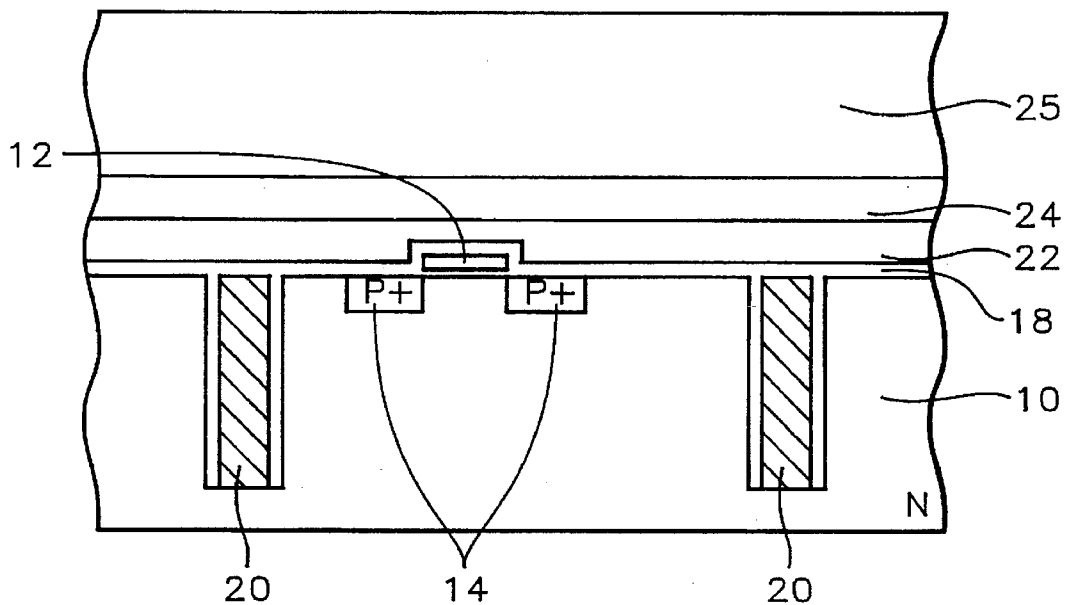


FIG. 6

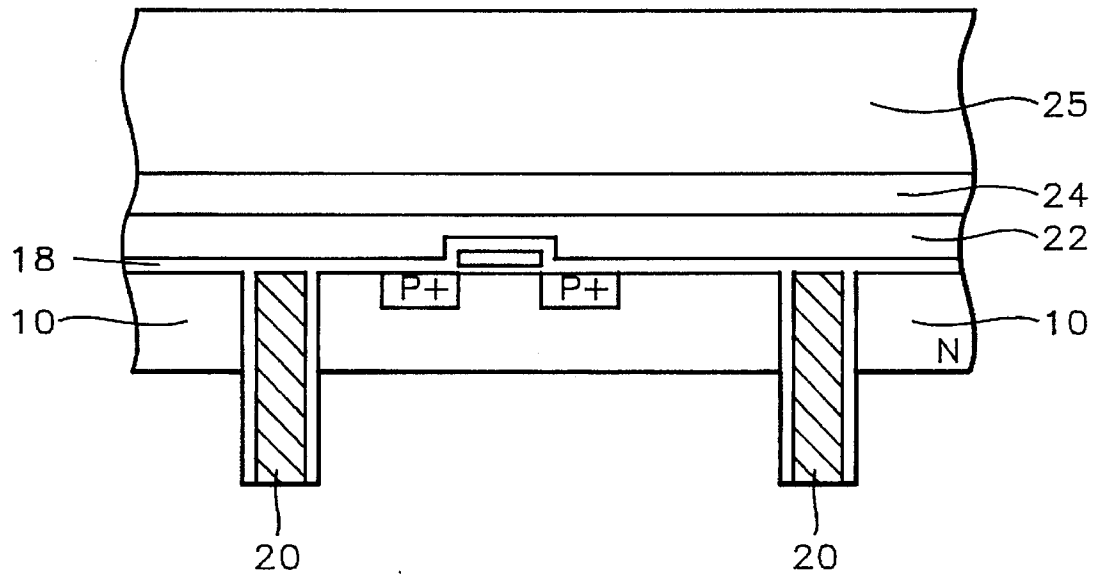


FIG. 7

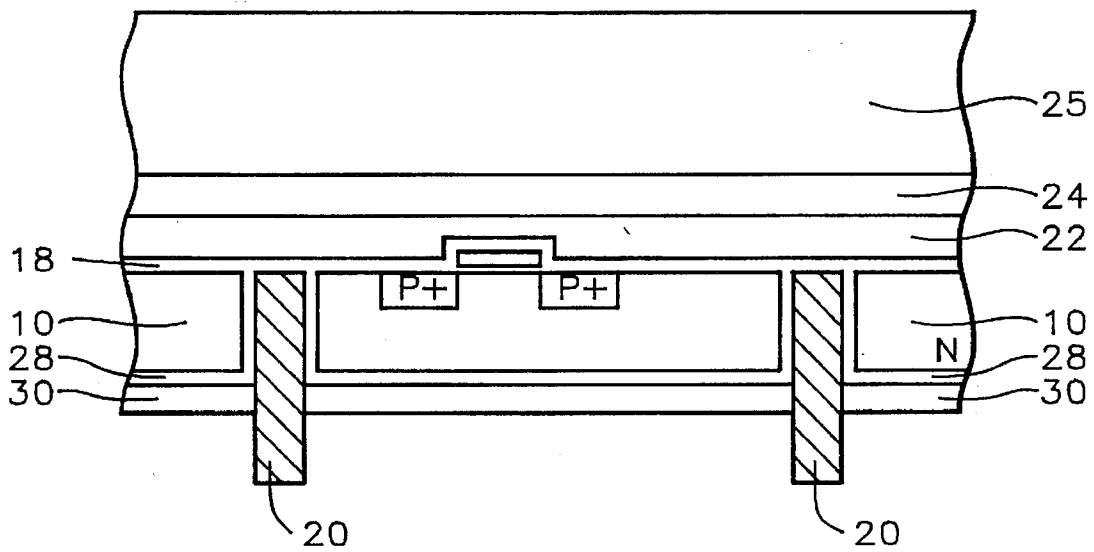


FIG. 8

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