



[54] MEMBRANE DIELECTRIC ISOLATION IC FABRICATION

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[51] Int. Cl.⁵ H01L 21/00

[52] U.S. Cl. 437/7; 437/974; 437/62; 437/238; 437/241; 437/907; 148/DIG. 135

[58] Field of Search 437/974, 7, 8, 62, 66, 437/238, 241; 156/662; 148/DIG. 135

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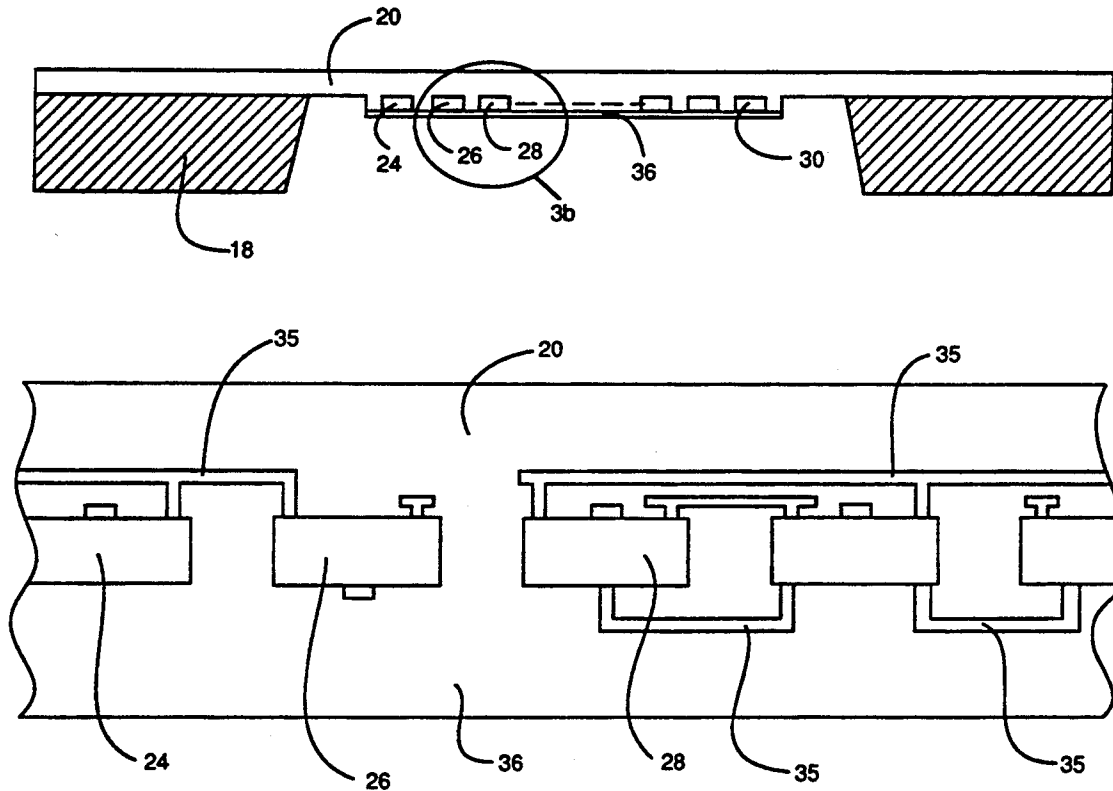
Primary Examiner—Brian Hearn

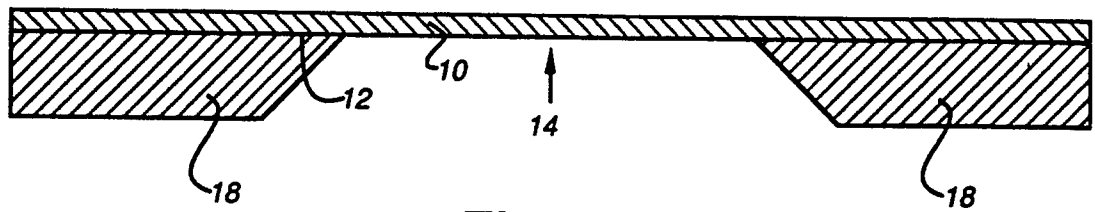
Assistant Examiner—Trung Dang
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

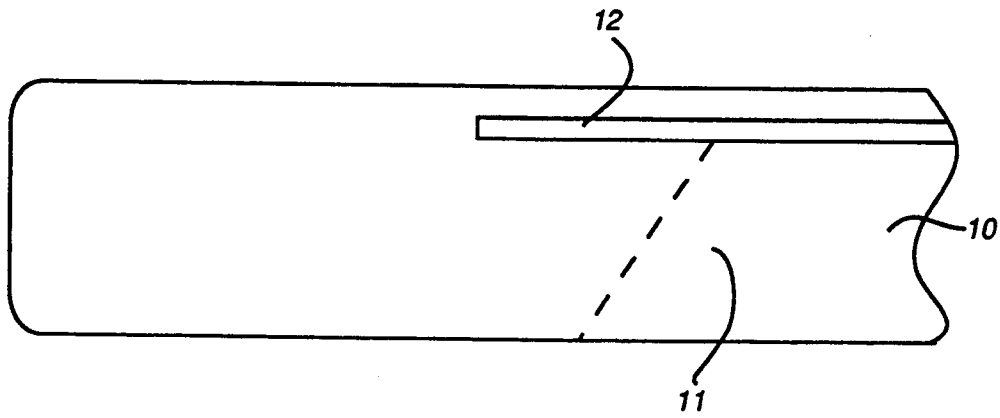
General purpose methods for the fabrication of integrated circuits from flexible membranes formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers. Semiconductor devices are formed in a semiconductor layer of the membrane. The semiconductor membrane layer is initially formed from a substrate of standard thickness, and all but a thin surface layer of the substrate is then etched or polished away. In another version, the flexible membrane is used as support and electrical interconnect for conventional integrated circuit die bonded thereto, with the interconnect formed in multiple layers in the membrane. Multiple die can be connected to one such membrane, which is then packaged as a multi-chip module. Other applications are based on (circuit) membrane processing for bipolar and MOS-FET transistor fabrication, low impedance conductor interconnecting fabrication, flat panel displays, maskless (direct write) lithography, and 3D IC fabrication.

16 Claims, 64 Drawing Sheets

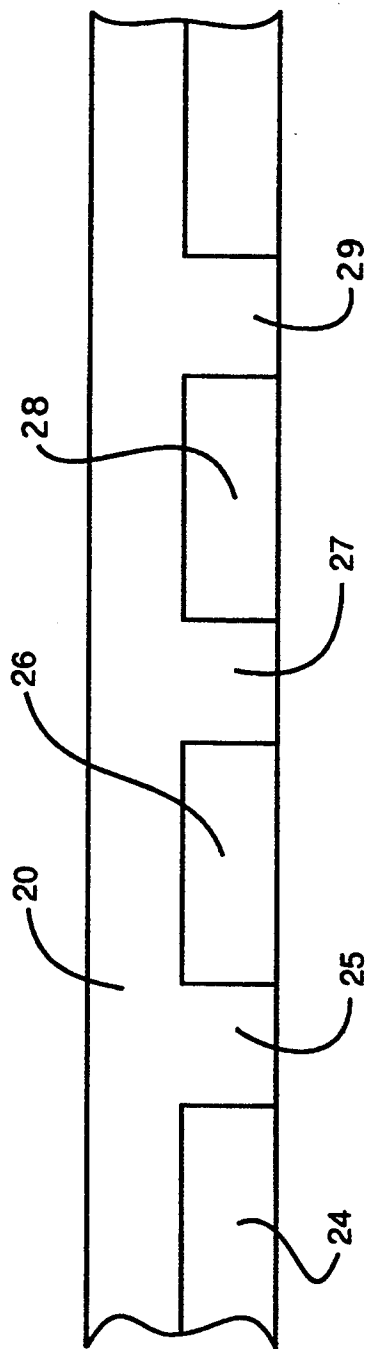




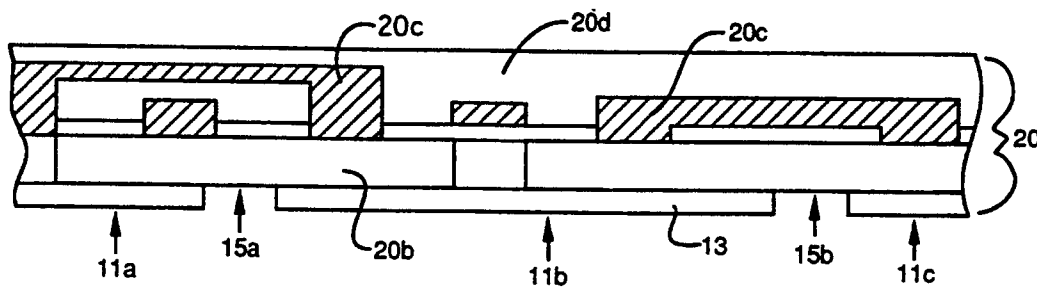
Fig_1a



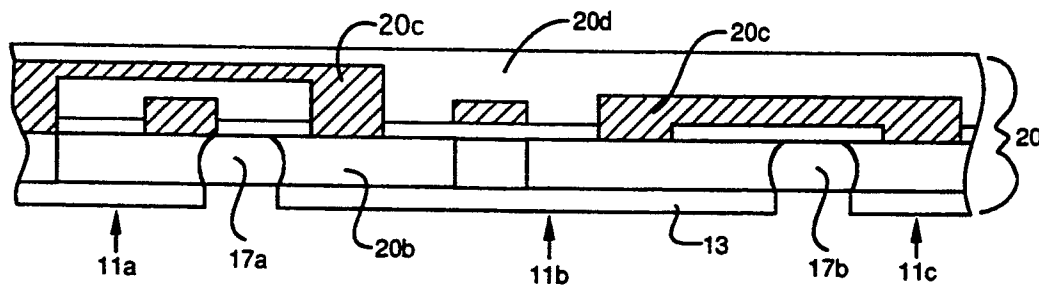
Fig_1b



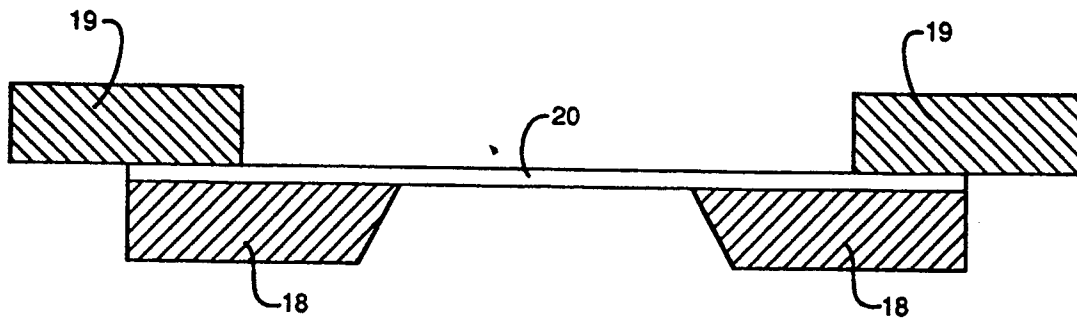
Fig_1c



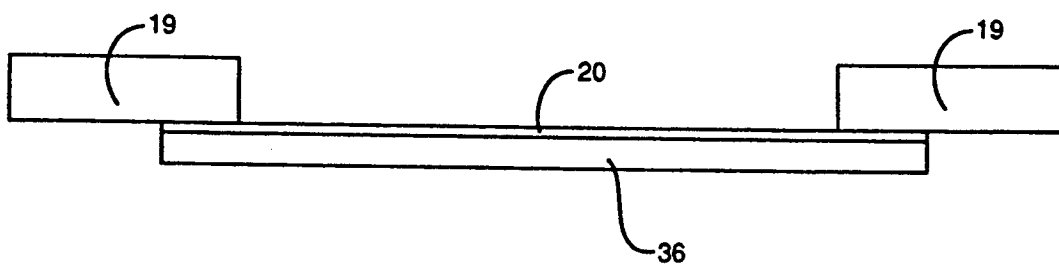
Fig_1d



Fig_1e



Fig_1f



Fig_1g

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