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First Named Inventor:	Glenn J. Leedy , Parkland, FL (US)	Issue Date of Patent:	-

Title of Invention: Three dimensional structure memory

Commissioner for Patents
P.O. Box 1450
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RESPONSE

Sir:

Responsive to the prior Office Action, please amend this application as follows.

1. (Currently amended) An integrated circuit structure comprising:

a first circuit layer comprising a first substrate, comprising a first surface having interconnect contacts, and a second surface opposite the first surface, and a second circuit layer comprising a second substrate comprising a first surface and a second surface each having interconnect contacts, wherein the second surface is opposite the first surface;

wherein at least one of the first and second circuit layers is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting and subsequently polished to form a polished surface, and wherein the at least one of the first and second substrates-circuit layers comprises at least one vertical interconnect extending from a the first surface thereof to an the opposite second surface thereof and formed within a via etched into the semiconductor substrate to accommodate the vertical interconnect, the vertical interconnect comprising a conductive center portion and an insulating portion surrounding the conductive center portion and adjoining sides of the via, wherein said at least one of the first and second substrates is formed from a semiconductor wafer or portion thereof;

a third circuit layer comprising a third substrate comprising and a first surface having interconnect contacts; and

a plurality of bonds forming signal paths between the interconnect contacts of the surfaces of the second substrate-circuit layer and the interconnect contacts of the first surfaces of the first and third substrates-circuit layers;

~~wherein at least one of the substrates is thinned to provide at least one thinned substrate, and wherein a second surface opposite the first surface of said at least one thinned substrate is a polished surface.~~

2. (Currently amended) An integrated circuit structure comprising:

a first circuit layer comprising a first substrate and having topside and bottomside surfaces, wherein the topside surface of the first substrate-circuit layer has interconnect contacts, and a second circuit layer comprising a second substrate and having topside and bottomside surfaces, wherein the topside and the bottomside surfaces of the second substrate-circuit layer have interconnect contacts;

wherein at least one of the first and second circuit layers is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting and subsequently polished to form a polished surface, and wherein the at least one of the first and second substrates-circuit layers comprises at least one vertical interconnect extending from a first the topside surface thereof to an opposite the bottomside surface thereof and formed within a via etched into the semiconductor substrate to accommodate the vertical interconnect, the vertical interconnect comprising a conductive center portion and an insulating portion surrounding the conductive center portion and adjoining sides of the via, wherein said at least one of the first and second substrates is formed from a semiconductor wafer or portion thereof;

a third circuit layer comprising a third substrate having topside and bottomside surfaces, wherein the bottomside surface of the third substrate-circuit layer has interconnect contacts;

a plurality of bonds between the bottomside surface of the second substrate-circuit layer and the topside surface of the first substrate-circuit layer;

conductive paths formed between the interconnect contacts of the topside of the first substrate-circuit layer and the interconnect contacts of the bottomside of the second substrate-circuit layer, and conductive paths formed between the interconnect contacts of the topside of the second substrate-circuit layer and the interconnect contacts of the bottomside of the third substrate-circuit layer, the conductive paths providing electrical connections between at least two of the first, second and third substrate-circuit layers;

~~wherein at least one of the the substrates is thinned to provide at least one thinned substrate, and wherein the bottomside surface of said at least one thinned substrate is a polished surface.~~

3. (Currently amended) An integrated circuit structure comprising:

a first circuit layer comprising a first substrate and having a first and a second surface, wherein said second surface is opposite to said first surface, and a second circuit layer comprising a second substrate and having a first and a second surface, wherein said second surface is opposite to said first surface;

wherein at least one of the first and second circuit layers is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting and subsequently polished to form a polished surface, and wherein the at least one of the first and second ~~substrates-circuit layers~~ comprises at least one vertical interconnect extending from a ~~the~~ first surface thereof to an ~~opposite~~ the second surface thereof and

formed within a via etched into the semiconductor substrate to accommodate the vertical interconnect, the vertical interconnect comprising a conductive center portion and an insulating portion surrounding the conductive center portion and adjoining sides of the via, ~~wherein said at least one of the first and second substrates is formed from a semiconductor wafer or portion thereof;~~

a third circuit layer comprising a third substrate and having a first and a second surface, wherein said second surface is opposite to said first surface;

a plurality of bondformed contacts between the first surface of the first ~~substrate~~ circuit layer and the first surface of the second ~~substrate~~ circuit layer and between the second surface of the second ~~substrate~~ circuit layer and the first surface of the third ~~substrate~~ circuit layer; wherein at least two of said contacts are selected from a group consisting of: a conductive signal path; a conductive contact; and a non-conductive contact;

~~wherein at least one of the substrates is thinned to provide at least one thinned substrate.~~

4. (Currently amended) An integrated circuit structure comprising:

a first circuit layer comprising a first substrate and having a first and a second surface, wherein said second surface is opposite to said first surface, and a second circuit layer comprising a second substrate and having a first and a second surface, wherein said second surface is opposite to said first surface;

wherein at least one of the first and second circuit layers is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate made from a

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