MULTICHIP MODULE TECHNOLOGIES AND ALTERNATIVES:

THE BASICS

Cover Photo

Courtesy of Unisys photographer, Paul Robinson. The top MCM is a hermetic processor module utilizing the *latest* MCM-D technology with fine pitch, high lead count, flip TAB connections. The bottom three packages are MCM-C modules with conventional wire bond connections. These modules are described in Chapter 14.

MULTICHIP MODULE TECHNOLOGIES AND ALTERNATIVES:

THE BASICS

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DEDICATION

This book is dedicated with sincere gratitude
to the 42 authors who contributed their knowledge,
suggestions and many hours of writing
to form the chapters we requested.
Without their diligence, timeliness of response and
patience with our requests
for additional or alternative information,
there would be no book.

ABOUT THE EDITORS

Daryl Ann Doane, President, DAD Technologies, Inc., is a specialist in the manufacturing of IC devices and packages, and in the marketing of materials, equipment and processes for such manufacturing. She has published more than 40 reports, papers and reviews documenting new process development and yield optimization. DAD Technologies, Inc. is a technology-based consulting organization serving both producers and users. Clients have included both government and commercial organizations connected with IC fabrication and packaging.

Dr. Doane previously served as Director, Microelectronics R&D for Hunt Chemical (now Olin Hunt Specialty Products). Prior to that she was a Member of the Technical Staffs of AT&T Bell Laboratories, RCA and Hewlett-Packard Laboratories.

Dr. Doane is a member of the American Physical Society (APS), Materials Research Society (MRS), International Society for Hybrid Microelectronics (ISHM), International Electronics Packaging Society (IEPS), and is a Senior Member of the IEEE. She received the 1980 Distinguished New Engineer Award from the Society of Women Engineers. She also served as President of the New Jersey Section of that Society.

Dr. Doane presently serves as Director of Technical Marketing for the IEEE-CHMT (Components, Hybrids & Manufacturing Technology) Society. She also is an elected member of the Board of Governors of the National CHMT Society. She served previously as Chairman of the San Diego Chapter of the CHMT Society.

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Paul D. Franzon is currently an Assistant Professor in the Department of Electrical and Computer Engineering at North Carolina State University. He has over eight years experience in electronic systems design and design methodology research and development. During that time, in addition to his current position, he has worked at AT&T Bell Laboratories in Holmdel NJ, at the Australian Defense Science and Technology Organization, as a founding member of a successful Australian technology start-up company, and as a consultant to industry, including positions on Technical Advisory Boards.

Dr. Franzon's current research interests include design sciences/methodology for high speed packaging and interconnections systems and also for high speed and low power chip design. In the past, he has worked on problems and projects in wafer scale integration, IC yield modeling, VLSI chip design and communications systems design. He has published over 45 articles and reports.

His teaching interests focus on microelectronic systems building including package and interconnection design, circuit design, processor design and the gaining of hands-on systems experience for students.

Dr. Franzon is a member of the IEEE, ACM and ISHM. He serves as the Chairman of the Education Committee for the National IEEE-CHMT Society.

Dr. Franzon received a BS in Physics and Mathematics, a BE with First Class Honors in Electrical Engineering and a PhD in Electrical Engineering all from the University of Adelaide, Adelaide, Australia.

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FOREWORD

Far from being the passive containers for semiconductor devices of the past, the packages in today's high performance computers pose numerous challenges in interconnecting, powering, cooling and protecting devices. While semiconductor circuit performance measured in picoseconds continues to improve, computer performance is expected to be in nanoseconds for the rest of this century - a factor of 1000 difference between on-chip and off-chip performance which is attributable to losses associated with the package. Thus the package, which interconnects all the chips to form a particular function such as a central processor, is likely to set the limits on how far computers can evolve.

Multichip packaging, which can relax these limits and also improve the reliability and cost at the systems level, is expected to be the basis of all advanced computers in the future. In addition, since this technology allows chips to be spaced more closely, in less space and with less weight, it has the added advantage of being useful in portable consumer electronics as well as in medical, aerospace, automotive and telecommunications products. The multichip technologies with which these applications can be addressed are many. They range from ceramics to polymer-metal thin films to printed wiring boards for interconnections; flip chip, TAB or wire bond for chip-to-substrate connections; and air or water cooling for the removal of heat.

While there are several books now on packaging, these books deal with the subject of multichip modules as part of packaging in general, or they treat a particular multichip module technology or they are at an advanced level. What is needed, therefore, is a *comprehensive book at the basic level*, structured so that anyone entering the field can quickly learn about the technologies, understand the tradeoffs, review the product examples, and make systems level decisions.

Such a book has been provided by Daryl Ann Doane and Paul D. Franzon. They have worked with an outstanding team of packaging experts from industry and universities. Together they have produced **Multichip Module Technologies and Alternatives: The Basics**, an outstanding book for both industry and university use. It is equally appropriate as an introduction to the multichip module technologies for those just entering the field, and as an up-to-date basic technical book for those currently practicing in it.

The books deals with the subject of multichip modules along three parts: systems level perspectives including packaging technology options and costs, the basics of ceramic, thin film and printed wiring board technologies as well as chip and module level connections; thermal and electrical design considerations including electrical testing; and finally product examples illustrating how multichip modules have been useful.

The basic and integrated nature of the book clearly reflects the dedication and the hard work of the editors and the authors.

Rao R. Tummala
IBM Fellow

PREFACE

Welcome!

Welcome to our book. We feel it is a unique book in the field of packaging and we hope you find it both useful and enjoyable. We (editors and authors) have certainly enjoyed bringing it to you!

Uniqueness of the Book

This is a very unique book! Its uniqueness comes about in two ways: first in the approach to the subject, and second, in the approach to the writing of the book.

First, we feel that this book helps define a turning point in the discipline of packaging. The "bottleneck" to increased systems performance is now more often the package than the chip. One effect of this is that suddenly a whole "breed" of engineers need to gain an understanding of how package design affects their systems performance and cost goals. Another effect is the widespread recognition that multichip module packaging technologies are possible solutions to this performance limitation. The attendant explosive growth in the MCM technology alternatives available is a testimony to this recognition.

Until recently, packaging was mainly the domain of mechanical and materials specialists, and furthermore was rarely taught at universities. *This has changed.* Almost overnight, the pressure of high on-chip speeds and high transistor counts meant that packaging became a subject that must be understood by just about any engineer involved in designing a system. When these engineers tried to establish their understanding they found themselves in a virtual "Tower of Babel." First, often the same terms were used for different things or, just as bad, different terms were used for the same thing. Second, as this was the domain of specialists, significant background was required in each discipline in order to understand it. This book turns the discipline of packaging into a subject accessible to the generalist rather than just one accessible to the specialist. Common terms are defined and crosslinked to the terms in current usage. Each discipline is presented in such a way that is both understandable to all and is useful. In providing this book, we help turn packaging into a discipline in which anyone can participate. We also present a book highly suited for teaching within a university.

The book also is unique in how it was created! Packaging is a multidisciplinary subject. We realized that no two people can claim mastery of all the disciplines needed and involved in the subjects we wished to cover. We also realized that rapid writing was important. Thus an edited text was called for. But edited texts are often poorly lacking in terms of understandability and flow. Usually an editor relies on selecting appropriate experts and then accepting what each expert writes with minor alterations.

This book is very different. It could be called a "closely edited" text. Each chapter has had the heavy hand of development of both editors in it. This happened in several forms. Often we spent many hours with individual authors defining what we thought was appropriate and guiding them in the actual writing. In all cases, as well as seeking outside reviewers, we wrote "anonymous" reviews ourselves. In some cases, we directly adjusted the text after it was submitted. Thus we are responsible for the final product as much as each chapter author is.

The result, we feel, is a book that has the authority that comes with a book written by a team of experts, but has the understandability, completeness and flow of a book written by a single author, At least we hope that the book comes as close to that ideal as possible!

Audience

For whom is the book intended? **This book is for everyone!** The emphasis in the book is on understanding the fundamentals and the reporting of real

experiences rather than including a huge amount of data. It is intended for those who need a broad exposure to the concepts underlying the design, fabrication, packaging, assembly, manufacturing of multichip modules and the costs associated with alternative packaging technologies. The book is intended for applications, manufacturing and design engineers as well as for technical decision makers and managers who are confused about MCM issues but who wish to understand the fundamentals and basics. Specifically, it will be useful to

- **engineers** in design, processing, fabrication, manufacturing, assembly and test who need to choose a packaging technology for specific product and application goals;

- **managers** determining technology alternatives for new systems needs;

- **marketing; sales technologists** who need a working knowledge of the alternative MCM technologies.

The book also is a suitable text for advanced undergraduate and graduate students in design, electrical, mechanical and systems engineering as well as for students in the applied sciences as discussed further on in this Preface.

Philosophy of the Book

What are the key decisions needed when considering using MCM technologies? There are four perspectives: materials, manufacturing, systems performance and cost requirements. The book presents the basics of MCM technologies from these four perspectives with an emphasis on decision-making. How do you choose a packaging technology from a systems performance, cost perspective? What are the fundamental materials and manufacturing issues that need to be considered? Is the packaging strategy appropriate to the design goal?

This book is applications-oriented in the sense that it discusses

- Examples of MCMs and the products and systems in which they have been used,
- Examples of equipment and processes used to design, build and test MCMs,
- Actual case studies and insights provided by leading companies themselves rather than a summary of reported results.

Organization of the Book

The book is divided into four parts which we call

- Part A - The Framework
  (Making Decisions: The Big Picture)
- Part B - The Basics
- Part C - Case Studies
- Part D - Closing the Loop

Each Part begins with what we call a "frame" in which we summarize the purpose or goals of the Part. The frames alert the reader to what theme dominates in the Part, and what can be learned from it. The frames are set apart from the rest of the book by the border around their pages.

For example, in Part A, the goal is to present a basis for understanding multichip module technology possibilities for packaging. We call this a *framework for understanding*. The basic definitions needed for understanding are presented. Some alternative packaging approaches are discussed, and the themes of decision-making and the design process that run through the book are also introduced. The reader is alerted to look for the global picture in Part A, an overview that a breadth of knowledge is required for understanding, and that an awareness of the basic concepts introduced is Part A will enable him or her to follow the detailed technical information in Part B.

Part B provides an understanding of the technical fundamentals in the design, fabrication and testing of multichip modules. The tutorials in Part B are unique in the published literature. For example, there is detailed coverage of MCM-L, the fabrication technology based on laminate structures. Another special feature of Part B is the discussion of multichip module-to-printed wiring board (second level) connections in Chapter 10. The test chapter (Chapter 13) provides specific guidelines on how to design MCM products for testing and how to reduce test cost and effort. In each Chapter, the reader is alerted to the options associated with the technologies presented so that these options can be related to product applications.

Part C consists of "reports" from some companies that have created and are selling successful MCM products. The development of their MCM technologies, internally from existing expertise, is described. Here the reader will benefit from the insights shared by these companies.

Finally, Part D "closes the loop." It focuses on what aspects of all the technologies presented are likely to have the greatest impact on meeting future needs from a systems perspective. It also presents a *forward view* by describing

some open, unsolved problems, open challenges that must be met if future systems are not to be constrained in performance by limitations in packaging technologies.

Use as a Textbook

We feel that this book is highly usable as a packaging textbook. It covers this interdisciplinary topic at a level that is accessible to all while providing concrete learning material. This book emphasizes decision-making and design, and thus, relates directly to what practicing engineers do for a living. It would be useful in both graduate courses and advanced undergraduate courses. It has the tightness and continuity of a textbook in contrast to a typical edited book. In our opinion, this book is superior to any current packaging "textbook" for use as a text mainly because of the style of presentation.

Despite its title, it could be used for many courses that do not feature only MCMs. Throughout this book, single chip packaging is presented as an alternative to be considered. The design chapters apply equally well to single chip and multichip package design. The only single chip package elements that are missing are a discussion of how plastic packages are made and a specific discussion of how boards are assembled. Chapter 9 covers some of these related points. Board manufacturing is covered in Chapter 5. Single chip ceramic package manufacturing uses similar processes as those for making ceramic MCMs which are discussed in Chapter 6.

There are several types of courses that can use this book. One of us (PDF) uses the book in a semester long graduate course on packaging design for electrical engineers. That course starts with an overview of packaging alternatives (Chapters 1 and 2, with 5 to 10 as references), discusses systems level decision-making (Chapter 3 and parts of the Case Studies), and briefly discusses cost (parts of Chapter 4). Almost half of the course is concerned with electrical design of packaging (Chapter 11). A small amount of time is spent on thermal design (Chapter 12), to the level of detail needed by an electrical engineer, and on the appropriate impact of testing on design (Chapter 13).

The book also would be useful for a more technology and manufacturing oriented course. There Chapters 1 and 2 would be used to introduce the course. Establishing the reasons for the multiple packaging alternatives available and how to choose among them would be covered with the aid of Chapter 3. Chapter 4 provides a detailed look into the impact of manufacturing costs. Chapters 5 through 10 would be used to teach the bulk of the course. Brief references to Chapters 11 through 13 would provide technologists with an

understanding of how their decisions affect design. Chapter 17 would offer a detailed manufacturing viewpoint.

Finally, this book also could be useful to mechanical and chemical engineers and materials science-based courses on packaging.

Daryl Ann Doane
Paul D. Franzon

ACKNOWLEDGMENTS

With the publication of this book, it is a special pleasure for one of us (DAD) to express gratitude and appreciation to Paul B. Wesling, Tandem Computers. His longstanding and patient role as mentor and resource person has provided an immeasurable educational opportunity and insight regarding the value of technical publications. He currently serves as Vice President of Publications for the IEEE Components, Hybrids and Manufacturing Technology (CHMT) Society. He has been a *pioneer* in the area of technical publications related to peer-reviewed journals, reprint as well as conventional books and Conference Proceedings. His innovative ideas in publications have been adopted by Societies outside of the IEEE, and also are reflected in the value and vision for this book. Thank you, Paul!

Several people advised us on technical and organizational topics. They generously contributed their time and valuable expert knowledge in extended discussions. In particular, Dr. Robert C. Sundahl, Intel, Dr. Walter J. Bertram, Alcoa Electronic Packaging and Professor R. Wayne Johnson, Auburn University, shared their ideas on what was needed in the book, as well as providing detailed reviews for several of the chapters. We wish to thank them.

John H. Lau, Hewlett-Packard was helpful in sharing his experience as an editor of three books for Van Nostrand Reinhold. He never tired of answering questions; we appreciate his patience and helpfulness very much.

John Nelson, Unisys, is very special! A faithful colleague and friend, he graciously responded positively to so many requests, providing the value of his longstanding experience and insight in the packaging industry in answering questions pertaining to the book. It has been a wonderful opportunity to discuss the technical aspects of the book, as well as its human side, with him. Many of the unique aspects of the book are due to his suggestions. *We thank him for everything!*

Each chapter in the book was reviewed by at least three individuals whose areas of expertise covered the chapter topic. We also deliberately asked individuals who worked in areas peripheral to a chapter topic to review the chapters for comprehension and clarity. Although we cannot list these more than 54 individuals, we are very appreciative of their efforts, thoroughness and helpful comments. We took them all very seriously.

Still, with all the technical expertise brought to form the contents of this book, there would have been no way to complete a book of this scope, size and complexity had it not been for the unique combinations of dedication and perseverance of the staff and management at Van Nostrand Reinhold (VNR), our publisher. We are very grateful for their efforts. Especially noteworthy was the standard of inspiration set by Mr. Stephen Chapman, Electrical Engineering Editor. He shared our "vision" for the book and persevered on our behalf for the conventional as well as the nonconventional requests we made. He arranged for an accelerated publication schedule so the book could be available when requested. Without his dedication to the book it would not have appeared in such a timely manner.

Sue Alexander of Seaborn Enterprises, Chandler AZ, was responsible for producing the galleys with artwork for the entire book. She demonstrated a high level of skill and innovation in adapting busy tables and complex equations to a text already filled with an unusual amount of photos and artwork. All the while she was faced with unprecedented time constraints. We are very much in awe of the final excellence of her creation in the layout and appearance of the book.

Most of all, we would like to thank those who are close to us. One of us (DAD) wishes to express special thanks to Dr. John L. Doane, Timothy A. ("TAD") Doane and Stevie Doane for their love, support and patience. Their faithful encouragement and sustaining, as well as helpful, assistance contributed significantly to the existence of the book. The other of us (PDF) gives loving thanks to Debra L. Ray in acknowledgment of her forebearance during the many long evenings and weekends when he was not there.

Part A—The Framework
Making Decisions: The Big Picture

"Cheshire Puss," she began, rather timidly,
"Would you tell me, please,
which way I ought to walk from here?"
"That depends a good deal
on where you want to get to,"
said the Cat.

Alice in Wonderland
by Lewis Carroll

In the first part of this book, we provide a *framework (or basis) for understanding* multichip module packaging possibilities. Construction of our framework begins by defining the alternative approaches available with respect to multichip module structures and the packaging strategies involving such structures. It also includes such issues as manufacturability, performance, cost and time-to-market common to any packaging strategy - single chip or multichip. Finally, in the construction of the framework, we suggest a design methodology or decision-making process by which a packaging strategy can be coupled to a particular product goal. There is no single "right" or "wrong" packaging technology, but only relative to a specific application goal.

By constructing our framework of understanding, it is possible to cover a broad base of information in a short time. Such an overview, or global picture, also emphasizes the multidisciplinary nature of the multichip module technologies involved. Because of the breadth of understanding required in the packaging "sciences," there is some confusion about multichip module packaging as a viable, practical technology alternative. Suddenly people who did not have to think at all about packaging must consider complex packaging alternatives. Managers and engineers are being forced to make decisions without a complete understanding of packaging alternatives. In Part A, we bring together the multiple disciplines involved in such decision

making considerations in a way understandable to the nonspecialist and to the student, as well as informative to a worker in the field.

In Chapter 1 of Part A, for example, the multichip module structure is defined and the alternative multichip module technologies are described. The themes of decision-making and the design process that run through the book also are introduced. The challenges presented to growth in the use of MCM systems, such as their performance, cost and associated infrastructure, as well as single chip alternatives, are discussed.

Chapter 2 provides an overview of MCM alternatives concentrating on materials and manufacturing issues. Specific examples of how some multichip modules have been manufactured are discussed.

We also consider (in Chapter 3) the relationships between the "needs" of the system being packaged and the choices of packaging technologies in terms of performance and cost, needs being defined in terms of application or product goals.

Packaging decisions are very sensitive to both direct and indirect costs which are discussed in all the chapters. Specifically, Chapter 4 of Part A focuses on cost modeling, at the component level, and from a manufacturing and design perspective.

In the Framework, the factors that influence high level packaging decisions are explored. Thus, Part A is particularly useful to the technical manager who needs to make decisions on the best applications of this new technology to company products, but does not need to understand the detail required to design these products. The practicing engineer will gain the breadth of knowledge required to understand the full impact of the new technology. The basic concepts introduced will enable an understanding of the detailed technical information provided in Part B. Marketing and sales people also will find this part useful in communicating to customers how the company packaging decisions help meet customer needs.

1

INTRODUCTION

Daryl Ann Doane

1.1 BACKGROUND AND DEFINITIONS

1.1.1 Purpose and Perspective of the Book

This is a book about multichip modules (MCMs). And the strategies involved in implementing them *successfully*! The book discusses the technology alternatives appropriate for MCMs, and the decision-making processes required for choosing the "best" technology for a particular application. The book helps to answer the question: ***Is the technology applicable (or appropriate) to the design goal?***

Multichip modules are not new! The basic science and technologies involved in the design, materials, fabrication and manufacturing of MCMs have been known generally for over 30 years. These packaging technologies span a wide range of technical disciplines, such as chemistry, physics, materials science, electrical and mechanical engineering. The broad range of technologies which now must be understood by an MCM designer, for example, has expanded beyond a conventional experience base. One goal of this book is to provide information so that such an individual can learn about the various available technologies, and how and which one to choose for his or her particular packaging needs.

In the past 30 years, there has been an exponential growth in transistor speed and in the number of transistors per chip. For example, both have doubled over the last three years. Chip interconnection speeds and chip I/O count have not increased at the same rate. As a result, chip interconnections play a more dominant and limiting role in determining overall system speed and performance. Packaging of the chips has become a more significant factor in performance. Systems level performance improvements are now being limited more by the packaging and interconnection technologies, and less by the chip technology itself.

Advanced packaging and interconnection technologies have been mainly the domain of high performance computers whose performance otherwise would have been limited by the package. MCMs are viewed by some as the *only suitable technology* for packaging such systems. Soon the performance of many more systems will be limited by the package, so it is anticipated that MCMs will appear in a wider range of systems in the future.

Some fundamental advantages of MCMs are:

- Increased system speed
- Reduced overall size
- Ability to handle chips with large numbers of input/outputs (I/Os)
- Increased number of interconnections in a given area
- Reduced number of external connections, for a given system function

Every external package connection degrades the system performance somewhat by its parasitics (undesired circuit elements). Each package lead has some parasitic capacitance and inductance that distort the shape of the signals passing through it. Reducing the number of external connections not only reduces these parasitics, but also generally contributes to system reliability. Thus, one way MCMs would reduce the parasitic effects is through the reduction in the number of second level connections they afford.

This book discusses selected technologies and alternatives for MCM design and fabrication. A multidisciplinary approach is used to evaluate the interactions between materials, processes, designs and assembly techniques. Contributions by different authors provide perspectives from many different viewpoints. The emphasis throughout the book is on making decisions among the technology alternatives for specific applications and products.

This chapter has two main purposes. First it provides the definitions needed to understand the book and relates these definitions to terms used in other chapters. These terms are common "jargon" in various disciplines, technologies or corporate cultures, and thus, may vary from chapter to chapter depending on the perspective. By relating these terms to each other and to the basic concepts,

we hope to remove some stumbling blocks in the way of the reader's understanding.

The second purpose of this chapter is to introduce some of the themes and perspectives presented in the book. Major themes include decision-making as it relates to designing MCM-based products and as it relates to implementing MCMs in the marketplace, MCM structures and technologies, and MCM manufacturing. These themes are introduced so that the reader can start relating to the multiple disciplines and approaches that are concerned with packaging right from the start of the book.

1.1.2 ARCHITECTURE - Building a Multichip Module Structure

In this section we define what is meant by a multichip module, and introduce the alternative technologies used to build a MCM structure.

What is a Multichip Module?

In this book we define a multichip module (MCM) as a structure consisting of two or more integrated circuit chips electrically connected to a *common circuit base* and interconnected by conductors in that base. The conductors in the base are usually patterned in multiple layers separated by a suitable insulating dielectric material, with vias for interconnections between layers. The base also provides the required mechanical support for the chips. Figure 1-1 shows schematically an MCM structure.

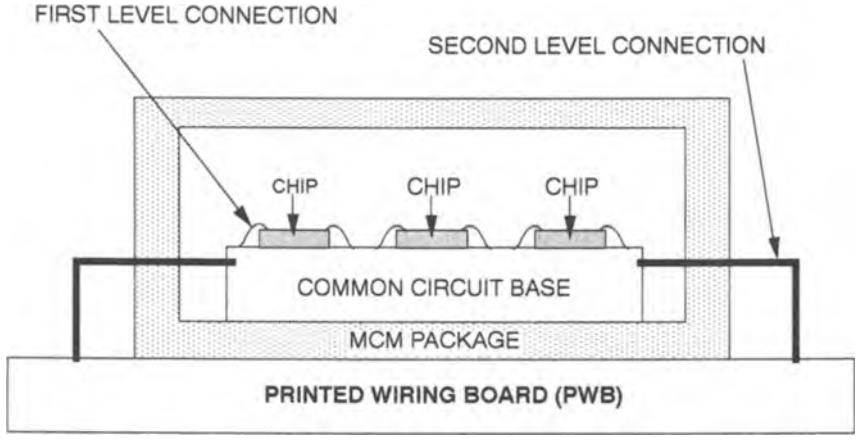

Figure 1-1 MCM architecture (schematic).

Based on this definition of an MCM structure, *multichip modules are not new!* In the very early days, MCMs were called hybrid circuits. Hybrid circuit assemblies are still in use, and usually contain lower lead count analog and digital integrated circuits (ICs), as well as active or passive discrete components. They may contain many layers of metallic conductors and ceramic dielectrics, but they classically have been formed one layer at a time. Chip-on-board (COB) assemblies, where bare chips are wire bonded to conventional printed wiring boards, also have been in use for some time.

Another definition for MCMs is based on the interconnection technologies that can be used in their structures. In particular, the IPC (Institute for Interconnecting and Packaging Electronic Circuits), according to its standard IPC-MC-790 [1], defines three types of technologies that can be used to make MCM structures:

- **MCM-L:** Modules using advanced forms of printed wiring board (PWB) technologies to form the copper conductors on plastic laminate-based dielectrics.

- **MCM-C:** Modules constructed on cofired ceramic substrates using thick film (screen printing) technologies to form the conductor patterns. ("Cofired" means that the conductors and the ceramic are all heated in an oven at one time.)

- **MCM-D:** Modules whose interconnections are formed by the thin film deposition of metals on deposited dielectrics, which may be polymers or inorganic dielectrics.

Some of the authors in this book refer to these structures as laminate MCMs, cofired ceramic or thick film MCMs, and thin film MCMs, respectively. All of these structures satisfy the definition of containing multiple chips electrically connected to, and interconnected on, a single base structure that is eventually connected to a printed wiring board.

A third approach to defining an MCM is based on the packaging efficiency achieved by the technology. Packaging efficiency (or "silicon density") is defined as the percentage of area occupied by silicon ICs [2]. Using this approach, an MCM can be defined as follows: An MCM is a structure in which a packaging efficiency of greater than 30% is achieved. This definition implies a particular degree of technology which allows the chips to be packed closely together. It excludes many hybrid and COB designs. For the purposes of this book, we seek to understand the broader construction of a multichip module structure without the 30% packaging efficiency restriction.

What is the MCM Architecture?

The basic idea of MCMs is to decrease the average spacing between ICs in an electronic system. The fundamental aspect of MCM technology is therefore the chip interconnection technology. This technology includes the method of connecting the I/O conductors on the chips to the common circuit base, and also the method of sending signals through that base between the chips. The main goals are higher performance resulting from reduced signal delays between chips, reduced overall size and reduced numbers of external connections.

The elements that make up an MCM structure, or architecture, are shown in Figure 1-1. These elements are the chips, the first level connections, the common circuit base, the second level connections and the package. The remainder of this section functionally defines these elements and introduces related terminology. Succeeding sections briefly present some of the available technology alternatives.

We use the term *common circuit base*, because it is common to all the chips, because it contains the signal interconnection circuits and the power and ground distribution circuits, and because it provides a mechanical support base for all the chips. Sometimes the top of the common circuit base is called the "substrate" or the "MCM substrate". See, for example, Figure 2-1. In that figure, the lower "substrate base" is that part of the common circuit base that provides mechanical stiffness to the MCM. In Figure 1-2, the "substrate/package circuitry" and the "substrate" correspond, respectively, to the "MCM substrate" and the "substrate base" of Figure 2-1.

Sometimes the substrate and the substrate base are the same. For example, in an MCM-C, the interconnections are formed in a solid ceramic. On the other hand, in an MCM-D, the interconnections are formed in a plastic-like polyimide dielectric. For mechanical support this substrate then needs to be attached to a substrate base, typically ceramic or silicon. (In other places, a silicon substrate base may be called "the substrate," based on its similar function in an IC.)

The first level connections consist of the signal and power/ground wires provided between the chips and the common circuit base. Not shown in Figure

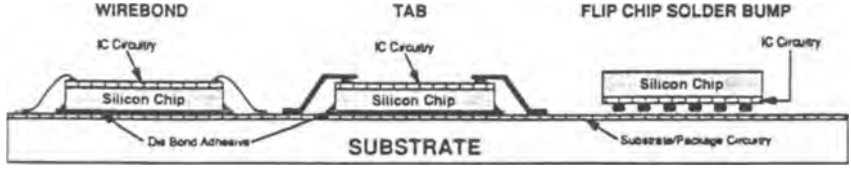

Figure 1-2 Common types of first level connections. Chip to common circuit base. (Courtesy E. Larson).

1-1 is the die attach. The terms "die attach," "chip attach" or "chip connect" are used to describe the physical anchoring of the die to the common circuit base. The wires in the first level connection usually form only part of the die attach. Often the chips are bonded to the common circuit base as well.

Note the distinction between the use of the words "connection" and "interconnection." In this book, the term "connection" is used to refer to the electrical connection between two levels of the packaging architecture in an electronic system. The term "interconnection" (signal interconnection, interconnection structure, or interconnection circuit) refers to the conductors provided within the common circuit base.

The second level connections are the connections between the MCM and the PWB on which it is mounted. Again, these paths refer to the current carrying conductors. Separate structures are sometimes used to fix the MCM physically to the PWB. Second level connection alternatives are explored in Chapter 10.

The package is the final part of an MCM, which can be seen, touched and felt. It provides the following functions:

- Physical protection from environmental (corrosion, humidity) and mechanical (vibrations, shock) stresses and from handling by automatic machinery used during manufacturing processes
- Part of the second level connection elements for the distribution of signals, power, and ground
- A means for removing the heat dissipated in the chips
- A space transformation (fanout) from the fine conductor spacings on chips to the coarser spacings on PWBs

Thus, the electronic package is an electromechanical structure that supports, protects and connects (electrically and thermally) the devices contained within it, independent of the actual number of chips involved - single chip or multichip. The package serves as the link between the component or circuit level functions (such as ICs, discrete devices, resistors, capacitors) and system level functions (such as circuit board assembly and board to board connections). In addition, it often allows testing and burn-in of its contained parts prior to further assembly.

In Table 1-1, we summarize the basic MCM architecture outlined above, and provide some examples of functions and technologies for each level in the architecture. (Sometimes this architecture is called the "hierarchy.") Notice that the order of the levels from top to bottom in Table 1-1 is the same as the physical order, shown schematically in Figure 1-1. In the next sections we define in more detail some of the technologies shown in that Table.

Table 1-1 Basic MCM Architecture.

LEVEL	FUNCTIONS	TECHNOLOGIES
Chips	Digital Analog	Si: CMOS, bipolar GaAs
1st level connection	Conductor connection from chips to common circuit base	Peripheral: wire bond, TAB, flip TAB Area: flip chip solder bump
Common circuit base	Signal interconnection Power and ground conductors	Hybrid circuits MCM-L, MCM-C, MCM-D MCM-Si, MCM-D/C
MCM package	Hermeticity Heat removal Physical protection Conductors	Peripheral conductors: DIP, QFP Area array conductors: PGA, PAC
2nd level connection	Conductor connection to PWB	Plated through-hole Surface mount

1.1.3 First Level Connection and Common Circuit Base Alternatives

Most of the methods for connecting the I/O conductors on the chips to the common circuit base also are used within single chip packages. See Figure 1-2. Wire bonding and tape automated bonding (TAB), for example, are used to make the connections between peripheral conductors on single chips and their packages. With "flip chip" arrangements, such as flip TAB, the chip is flipped over so that its conductors are on the bottom, facing the common circuit base. Flip chip solder bump (FCSB) connections are analogous to the connections beneath single chip surface mount area array packages to conductors on PWBs.

Physical attachment ("chip attach" or "die attach") of the chips to the common circuit base is a distinct operation from wire bonding or TAB conductor connections, but occurs simultaneously with the solder connections in FCSB. With flip TAB, there is no metallurgical bond between the chip and the common circuit base. Sometimes epoxy is used, and sometimes the chip is held in place by the connected TAB leads.

The common circuit base is that part of the MCM structure that defines the MCM technology used: MCM-L, MCM-C or MCM-D. However, MCM signal

interconnection technologies themselves have developed from other technologies, such as patterning ICs on silicon, packaging ICs and mounting ICs on PWBs. The names for these technologies are relatively new [1], but the basic technologies are fairly mature.

For example, decreasing the sizes of conductor lines and spaces on laminate PWBs leads to the MCM-L technology ("L" stands for laminate). MCM-L technology also is an outgrowth of the COB technology, since the packages around individual chips are omitted. The laminate normally includes several layers of patterned metal conductors pressed together (laminated) with interspersed polymer dielectric insulating layers. The adhesive joining of all these layers is done at a relatively low temperature.

MCM-C technology ("C" stands for cofired ceramic, but also may include thick film) is a development of traditional hybrid circuit technology, where printed thick film conductors are used to provide the signal interconnections. To increase the circuit density, multiple thick film layers of conductor and dielectric are used, just as in PWBs. The layers originally had to be built up with sequential ceramic firing operations, since the dielectric was applied as a thick film of ink. Later developments allowed conductors and ceramic layers of alumina to be fired all at once, provided this was done at a higher temperature ("high temperature cofired ceramic" technology or HTCC). One early application of this cofired MCM-C structure, with over 30 ceramic layers, was for mainframe IBM computers [3].

The glass-ceramic dielectrics used originally in ink form were later made into tapes. (The layers of unfired ceramic generically are called "green tape." "Green" is a ceramicist's term for the unfired material, even though the sheets of tape actually may be other colors.) Simultaneous firing of all the layers was then possible at the lower temperatures used in original hybrid circuit technology. This is called "low temperature cofired ceramic" technology or LTCC.

To obtain the highest density MCM signal interconnection circuits, other technologies use techniques such as photolithography developed for patterning circuits on silicon chips. With MCM-D ("D" stands for deposited), both the conductors and the insulating dielectric layers that separate them are deposited. The dielectric is usually an advanced (organic) polymer such as polyimide, although (inorganic) silicon dioxide (SiO_2) is sometimes used. Multilayer conductors are deposited as thin films, such as are used on single layer hybrid circuits for resistors and bonding pads. Vacuum metal deposition processes such as sputtering, polymer deposition processes such as spin and spray coating, chemical vapor deposition (CVD) of SiO_2, and patterning processes such as wet chemical, or plasma (dry) etching and laser etching are familiar chip processing techniques.

The dielectrics used in MCM-D usually are not strong enough to stand alone. Thus, in this technology a separate, different material is used for mechanical stiffness and support. It may be silicon, metal, ceramic containing no conductors, or a PWB or multilayer cofired ceramic that contains conductors. The identification of this material is sometimes included in the technology label. For example, when MCM-D technology is used with a multilayer cofired ceramic substrate base containing the MCM power and ground circuits and signal I/O vias, the technology is called "MCM-D/C." When silicon is used, the MCM technology is called "MCM-Si." MCM-Si technologies may use either thermally grown SiO_2 or CVD SiO_2.

1.1.4 MCM Packaging Alternatives

Packaging technologies involve a consideration of the materials to be used, the geometry of the package, as well as the thermal and electrical design parameters. This section begins by considering the basic functions that a package must perform. Since most MCM packages have been, until now, similar or identical to single chip packages, the classifications of these packages also are summarized. Then, some features of packages specific to MCMs are examined.

Entire books [G1] have been written on microelectronics packaging. For details, the reader is referred to these general references at the end of the chapter. The intent in this section is to provide a working knowledge of the language of packaging and some aspects of packaging that will be useful and relevant to MCM design and technology selection.

Classifications of Packages

Packages can be classified by their main material, the second level connection technique, the means used to remove heat, the method and degree of protection (encapsulation) of the chips, first level connections, and common circuit base. In this part, we explore certain aspects of these classifications. Second level connection classifications are explained more fully in Chapter 10. Available options for heat removal are discussed in Chapter 12.

The most common materials used for the package body are ceramic and plastic. If ceramic is used, it is made using the same approaches used to make ceramic substrates, and then a metal lid is brazed to the package. Plastic bodies usually are made through a process called injection molding, where the chip is placed in a mold into which plastic is injected.

Packages may contain internal cavities, or recesses, for mounting chips or MCM substrates. These cavities provide room for many connections to the package leads.

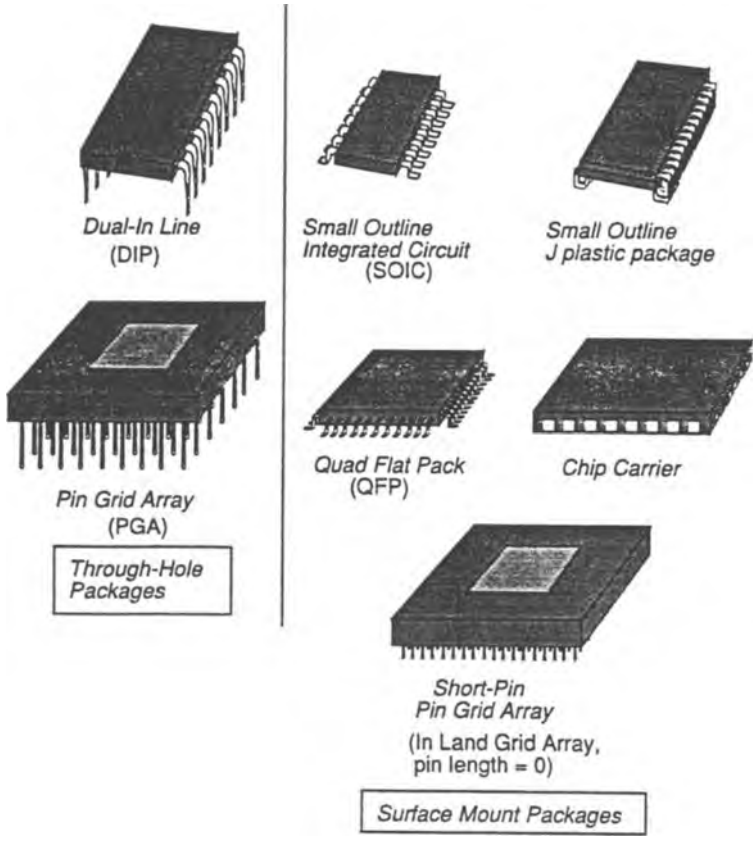

Figure 1-3 Common through-hole and surface mount packages. (Courtesy P. Franzon.)

Some of the single chip types of package also used for MCMs are sketched in Figure 1-3. One way to classify these packages is in terms of the method of mounting to the next level in system assembly: through-hole mounting or surface mounting. The conductors are called leads or (straight) pins; in the case of surface mounted packages they may be pads.

Plated through-holes (PTH) in a printed wiring board (PWB) refer to precision holes drilled through the board and plated with copper. These copper-plated holes form electrical interconnections between bond pads on the

top of the board and the conductors within the board. They also provide interconnections between the different conductor planes within the board.

Current PWB design rules and manufacturing capability limit the use of through-hole packages with high pin counts. For example, current PWB designs can accommodate holes on a 0.100" (2.5 mm) grid. Each package requires one hole for every package pin; each pin is typically 0.035" (0.9 mm) in diameter. Advanced PWBs can accommodate holes with 0.050" spacing. Surface mounted packages, on the other hand, can be connected to pads of the surface of PWBs with 0.025" spacing.

Packages can be grouped further according to physical arrangement of the leads (peripheral or area array), and package lead geometries, such as J-shaped and gull wing. The SOIC (small outline IC) and QFP (quad flat pack) shown in Figure 1-3, for example, have gull wing leads.

In Table 1-2, we classify the common packages, provide their abbreviations, and indicate typical lead (conductor) count and spacing.

The progression in Table 1-2 is from the simple to the advanced. The upper package types in this table all have peripheral leads. We start with dual in-line packages (DIPs), which have leads on only two sides and which are mounted in PTHs. Of the surface mounted packages with peripheral leads, SOJ stands for a small outline package with J- shaped leads, TSOP stands for thin small outline package, and PLCC stands for plastic leaded chip carrier. Next come the area array packages, with PTH mounted pin grid arrays (PGAs) first. If the PGA pins are shortened as shown in Figure 1-3, then PGAs can be surface mounted. Since surface mount pads on a PWB can be spaced more closely than PTHs, the possible lead pitch is reduced.

Area array pad array carriers (PACs) with solder bumps on the underside may be soldered directly to the PWB in a process analogous to connection of the solder bump for flipped chips (FCSB) to their MCM substrate. The process sometimes is called C5 (Controlled Collapse Chip Carrier Connection) for the PAC, and C4 (Controlled Collapse Chip Connection) for the FCSB. PACs are presently in the prototype stage; future lead spacings may drop to 0.02". A PAC is similar to a PGA with zero-length leads. Such a PGA is called a land grid array (LGA).

Properties of MCM Packages

Table 1-2 is only a starting point for MCM packaging: there are many alternatives.

MCM packages often look like regular-sized versions or large versions of well known single chip packages with pins or leads emerging from them. Sometimes the MCM has a highly customized package that does not resemble an existing single chip package. Often the substrate base (mechanical support

Table 1-2 Common Package Classifications.

PACKAGE TYPE	BODY		LEAD		TYPICAL LEAD	
	Plastic	**Ceramic**	**Arrange**	**Connect**	**Pitch (in.)**	**Count**
Dual In-Line	PDIP	Cer/DIP	Peripheral	PTH	0.05 - 0.1	64
Small Outline	SOIC SOJ TSOP	Flat Pack	Peripheral	Surface	0.025 - 0.05	28
Chip Carrier	PLCC		Peripheral	Surface	0.05	84
Quad Flat Pack	PQFP		Peripheral	Surface	0.01 - 0.05	256
Pin Grid Array	PPGA	CPGA	Area	PTH	0.05 - 0.1	144; 299
Short Lead PGA	yes	yes	Area	Surface	0.05	to 500
Pad Array Carrier = Land Grid Array	yes	yes	Area	Surface	0.02 - 0.05	to 1000

structure of the common circuit base) is used to form part of the package. In other cases, a package housing is not used. Instead, leads or pins are attached to the common circuit base for second level connection, and the exposed chips and wires are sealed against moisture by using epoxy or gel.

MCM packages must be mated carefully to the total MCM architecture. For example, the MCM common circuit base technology determines the possible lead geometry of the package. If there are electrical vias through the substrate bases for MCM-D or MCM-Si, the package leads then must be peripheral (as shown schematically in Figure 1-1). To allow area array conductors under the package with MCM-D, a multilayer ceramic package can be added (as in MCM-D/C).

The first level connection determines the possible thermal paths. In the case of flip chip mounting, much of the heat can be taken through the top of the package. Then rather poor thermal conductivity in the MCM substrate can be tolerated. Since there are no electrically sensitive conductors on the backsides of the chips, the chips may be connected through thermal gel or elastic spacers directly to the package top, to which a heatsink or cold plate can be attached.

Hermeticity describes the relative effectiveness, or extent, of sealing of a package. Hermetic packages have very low leak rates in helium testing ($< 10^{-7}$ atm-cc/sec typically). Hermeticity or near-hermeticity is important in packaging, since moisture can cause electrical circuit failures. Water absorption in organic dielectrics results in swelling that can cause separation of conductors, and other electrochemical activity such as copper plating, for example. Also, water may induce migration of silver from conductors, leading to short circuits. HTCC MCM-Cs may be used without a separate package, since the fired ceramics are hermetic. As discussed in Chapter 6, most LTCC ceramics probably are hermetic also. The lowest cost MCM-Ls have simple epoxy encapsulation for protection, without a separate package [4], and thus are not hermetic. Recently, it has been realized that many nonhermetic sealing approaches, including plastic packaging, epoxy and gel encapsulation, are sufficiently resistant against contaminants and moisture to provide good reliability in many, even military, applications. This subject is currently under investigation. See Figure 1-4 for some possible encapsulation options.

The performance of a package is discussed further in Chapter 3.

1.2 FINDING YOUR WAY

The other chapters in **Part A - The Framework** provide further perspective on MCMs. They also provide bases for choices between MCM technologies from the point of view of manufacturability, performance and cost, in Chapters 2, 3 and 4, respectively. Chapter 2 provides an overview related to the materials and the manufacturability of MCMs. Specific examples of how some MCMs have been manufactured are presented. Chapter 3 covers the relationships between the needs of the system being packaged and the alternative technologies that exist ("need" being defined in terms of application or product goals, and being coupled with performance and cost as tradeoffs).

Chapter 4 focuses on MCM cost at the component level in keeping with the book's emphasis on MCM components. Two types of cost models are described. One is manufacturing activity-based (called technical cost modeling), useful when in-house manufacturing details are known. The other is a design activity-based model useful when the only manufacturing-related information available to the designer are vendor quoted prices, for example. Although many companies

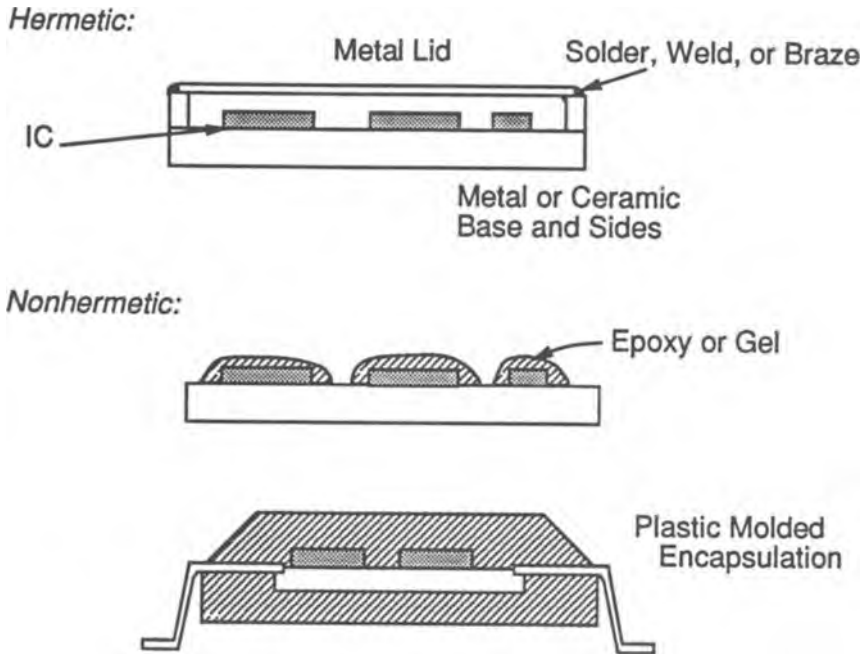

Figure 1-4 Hermetic and nonhermetic package encapsulation options. (Courtesy P. Franzon).

pursue a technology based primarily on previous experience, these chapters may provide the incentive to examine less familiar technologies.

In **Part B - The Basics**, MCM-L, MCM-C, and MCM-D signal interconnection technologies are discussed in some depth in Chapters 5, 6 and 7, respectively. Chapter 8 examines the dielectrics used with MCM-D. The several parts of Chapter 9 treat the physical die attach methods as well as the conductor connection technologies such as wire bonding, TAB, and flip chip methods similar to FCSB for the interior of the MCM. External connection of MCMs to PWBs is considered in Chapter 10.

The maximization of electrical (signal propagation) performance and thermal performance is considered in Chapters 11 and 12, respectively. MCM electrical testing issues are a big factor in overall MCM costs and are considered in Chapter 13.

The Case Studies in Part C consider various developments of actual products based on particular MCM technologies. The Unisys experience with MCM-C and MCM-D is examined in Chapter 14. Hughes MCM-C and MCM-D products

are covered in Chapter 15. Experience with MCM-Si is considered in Chapter 16, and the DEC MCM-D experience is considered in Chapter 17. For examples of MCM-L products, the end of Chapter 5 may be consulted.

1.3 THE IMPORTANCE OF MATERIALS

Even a cursory reading of the various chapters in Parts A and B reveals the central importance of materials properties for MCM technologies. Many of the most important properties are highlighted in Table 1-3, which also shows some of the symbols and units. We mention some examples briefly in this section.

Numerical values for many of these properties are given in Chapters 5 through 8. For example, Table 5-1 lists the properties of dielectrics used in MCM-L, Tables 6-5, 6-7 and 6-8 show the properties of MCM-C materials, including HTCC and LTCC materials, and Table 7-3 gives the properties of dielectrics and conductors used in MCM-D. Tables 8-2, 8-4, 8-5 and 8-6 list important properties for various MCM-D thin film dielectrics, and Table 8-13 summarizes these properties for polyimides.

The electrical properties are most important for high frequency signal interconnections, where they affect the signal delay between chips and the spacing between conductors. These properties are introduced in Chapters 2 and 3, and are discussed in considerable detail in Chapter 11. For example, the speed of signal propagation in a dielectric is inversely proportional to $\sqrt{\varepsilon_r}$, so higher dielectric constants, ε_r, cause longer delays.

Performance is degraded not only by slower propagation between chips, but also by distortion of square-shaped signal pulses. Major sources of this degradation are unintentional resistances, inductances and capacitances in the circuits between chips. These unintentional elements are called parasitic circuit elements. Some of these parasitics are caused by the first level connections; others are related to the materials in the common circuit base; still others are caused by second level connections.

Parasitic resistances, for example, are associated with losses in the metal conductors and in the dielectric of the common circuit base. These resistances increase the rise time of the pulse, which effectively increases the signal delay. Dielectric losses are proportional to the dielectric loss tangent, tan δ. The loss tangent (dimensionless) is sometimes called the dissipation factor, in which case it is normally given in percent.

Parasitic capacitance between conductors is due to the dielectric, and can cause crosstalk coupling of one signal into another. Parasitic mutual inductance is associated with the magnetic fields around current-carrying conductors and can

Table 1-3 Principal MCM Materials Properties.

ELECTRICAL PROPERTIES	THERMAL PROPERTIES	MECHANICAL PROPERTIES	PHYSICAL PROPERTIES	CHEMICAL PROPERTIES
Dielectric constant, ε_r	Coefficient of thermal expansion CTE (ppm/°C)	Young's modulus E (GPa or kpsi)	Microstructure (grain size)	Metal oxidation
				Metal migration
			Flatness and Planarization	Reactivity
Loss tangent tan δ	Thermal conductivity (W/m-K)	Poisson's ratio ν	Hermeticity	Adhesion
Resistivity (Ω-cm)	Shrinkage	Elongation	Melting point	Toxicity
	Thermal stability	Flexural strength (GPa)	Glass transition temperature, T_g	Environmental

also cause crosstalk. To keep the crosstalk acceptably low in high frequency interconnections, the conductor spacing must increase with increased ε_r. These factors are explained further in Chapters 3 and 11.

Thermal properties are important during the processing that forms the MCM and/or during the thermal cycling that occurs in MCM operation. Ceramic shrinkage after processing ("firing") and the thermal stability of organic dielectrics at processing temperatures are examples of dielectric properties important mostly for process design. A high thermal stability means that there is no significant outgassing or change in the mechanical dimensions that could lead to delamination.

Thermal conductivity is most important with high power single and multichip module operation. The thermal conductivity of each path from the chip to the outside world must be considered to maintain the junction temperatures on the chip at acceptable levels during operation. Poor heat transfer through materials with low thermal conductivity can be overcome by placing special conductors ("thermal vias") through the material, or by sending most of the heat through another path, such as a conductor attached to the "backside" (side away from the I/Os) of a flip chip connected die. Optimal design of these paths and also of heat transfer to cooling media such as air and water is examined in Chapter 12.

Differences in the coefficient of thermal expansion (CTE) between chips, common circuit base or package can lead to breakage either during cool down from a processing step or after extended thermal cycling. Whenever the temperature changes, connected parts with different CTEs expand or contract by different amounts, resulting in strain on the interface between parts. With large temperature changes, such as occur during processing, this might result in immediate failure, such as conductor breaks, or conductor peeling from a dielectric. Repeated smaller temperature changes, such as on/off operation in the field, eventually might result in thermal fatigue failures.

The units of CTE are parts per million per °C (ppm/°C). For example, with a CTE of 100 ppm/°C, the length of an unconstrained dielectric originally 10 mm long increases by 0.1 mm in a temperature rise of 100°C. Note particularly that the CTE itself can be a strong function of temperature, and can also be anisotropic (direction dependent). The CTEs (also called the thermal coefficient of expansion, or TCE) for some ceramics and organic dielectrics are tabulated in Chapters 6 and 8.

Some mechanical properties are important for their role in determining the response of materials to temperature cycling. Consider, for example, the bowing or camber of a silicon substrate beneath a thin dielectric. Excessive bowing following cool down from processing can make photolithographic conductor patterning difficult in MCM-Si. This bowing results from the different CTEs of

the substrate and dielectric, and is proportional to the ratio of the Young's modulus of the dielectric to that of the substrate. A large Poisson's ratio corresponding to an almost incompressible dielectric can also cause large bowing. These issues are discussed Chapter 7.

Conductors with high elongation and ceramics with high flexural strength can make a design more robust to thermal and mechanical cycling. In copper, the substantial plastic flow or elongation before breakage is a definite advantage. Similarly, solders that can plastically deform to accommodate CTE mismatch between chips and the MCM substrate can make flip chip solder bump (FCSB) technology more reliable.

Several units of stress for quantities such as Young's (elastic) modulus and flexural strength are in common use. Some equivalences are: 1 GPa = 1000 N/mm^2 = 145 kpsi, where GPa is gigapascal, N is newtons, and kpsi is 1000 pounds per square inch.

The physical and chemical properties listed in Table 1-3 are important mainly in processing. For example, a smooth and flat surface is important for high resolution conductor patterning. A ceramic with a large grain size may have unacceptably large surface roughness. In a multilayer structure, a polymer with good planarization can smooth out the features, or height variations, of layers that it covers.

Adhesion between metal conductors and polymer dielectrics is important in MCM-L and MCM-D processing. The glass transition temperature, T_g, of a glassy polymer is its softening temperature. Generally a lower T_g is beneficial for adhesion of the polymer to other layers and for stress relaxation, but is detrimental to dimensional stability. See the discussion in Chapter 8.

Copper reacts with polyimides and oxidizes at high temperatures. Therefore, copper in multilayer structures often is protected with another metal, such as nickel or chromium, which in turn should not react with the neighboring dielectric. Good conductors, such as copper, silver and gold, melt at temperatures required in HTCC processing, so lower conductivity metals must be used in HTCC structures. These and many other processing issues are covered in detail for each of the MCM signal interconnection technologies in Chapters 5, 6 and 7.

Hermeticity or near-hermeticity is important for long term reliability. This is particularly important for MCM-C devices that may have no separate package. Verification of LTCC ceramic hermeticity allows the use of relatively inexpensive silver conductors, which are susceptible to metal migration when exposed to moisture. Absorption of moisture in polymers may cause swelling and consequent breakage of attached conductors.

Toxicity of compounds of beryllium and alloys of lead under certain conditions, and environmental concerns over chlorinated fluorocarbons and some solvents, has led to searches for alternatives to these materials.

New materials also can make new high performance and/or cheaper technologies practical. For example, porous cordierite ceramic was developed for the interior of MCM-L laminates because it has a relatively high thermal conductivity and Young's modulus, and a relatively low dielectric constant and CTE. Some other new materials possibilities have been touched upon in this short review. Hopefully, readers of this book will be inspired to find new materials solutions to problems that impede the introduction of present and future MCM technologies.

1.4 THE IMPORTANCE OF MANUFACTURING PROCESSES

New MCM manufacturing processes to reduce costs are under active investigation, as can be seen from a reading of the chapters in Part B. These include blurring of the various MCM technology definitions described above.

For example, MCM-L may approach the thin film capability of MCM-D to pattern fine lines by using additive conductor processing instead of the subtractive etch processing traditionally used to pattern conductors on PWBs. The common circuit base is still a low cost laminate. Similarly, new developments of thick film screen printing emulsions and wires may allow fine conductor lines to be patterned on LTCC dielectrics, while at the same time new LTCC dielectrics have been developed with dielectric constants as low as those of the organic dielectrics used in MCM-D. In these ways, performance may approach that of MCM-D but at lower cost.

On the other hand, MCM-D costs can be reduced by increasing yields and using larger substrates. For example, patterning of somewhat wider lines and spaces on MCM-D substrates can lead to higher yields, since there are fewer large defects that can cause shorts and opens than there are small defects. Larger wafers (for MCM-Si) can become useable also. This is a simple example of improved manufacturability, where the yield is less sensitive to process imperfections. This type of manufacturability improvement is important particularly because it reduces costs even without the reduction in process imperfections that normally occur in proceeding up the learning curve to high volume production.

Just as with IC patterning, transfer of a new technology from a prototype lab to the production floor is critical. The production environment offers new challenges to high yields. Superior R&D efforts by U.S. companies have not been matched with equal efforts in transferring technology to production. Fast turnaround and accurate monitoring of factory production flow are essential.

High performance with high yields and accompanying low costs then requires creative and competent people from process design engineers to

technology transfer experts to production technicians. An adequate supply of such people presupposes that manufacturing is viewed as an attractive alternative for students making career choices. Manufacturing competence is critical to a healthy economy [5], and we hope that readers of this book will even find that manufacturing can be glamorous and rewarding!

1.5 THE IMPORTANCE OF INDUSTRY INFRASTRUCTURE

In order for a product (the "final" product) to be designed and produced successfully, a number of intermediate products and services must be available. For MCMs, for example, these include the substrates, the chips, CAD tools and training in how to use them, test machines, etc. In principle, a company could provide such intermediate products and services from internal resources. Such companies are referred to as "vertically integrated companies." However, for most companies this would be inefficient. Thus, a portion of those intermediate products and services must exist outside the company as common, shared resources. These intermediate products and services provided to the industry as a whole are referred to as the "industry infrastructure."

Naturally, the infrastructure needs of any one company depend on what it does not wish to provide from its internal resources. The most common case is the company whose only asset is design expertise. Such a company relies on others to manufacture the ICs, MCMs, PWBs and other assemblies that make up their designs, and to provide the information and tools necessary to carry out their designs. In order to implement high performance MCM-based products successfully, such a company needs the following infrastructure elements:

- One or, preferably, two or more suppliers who can manufacture the same "unpopulated" (without chips) MCM in quantity with high yields and with sufficient manufacturing capability to be cost competitive. Two suppliers are preferred to reduce risk of product starvation if one supplier has a temporary problem, for example. This is referred to as "multi-sourcing." True multi-sourcing is rare now, but most MCM designers are coping adequately with single suppliers. MCMs need to be delivered fully tested and guaranteed.

- One, preferably two or more suppliers of qualified bare die suitable for MCM mounting. By "qualified," it is meant tested, burnt in, and guaranteed to the degree that packaged die are. Generally, it is more efficient for the chip manufacturer to perform these tests than for the chip user. By "suitable," it is meant that die are provided in the following forms:

- Bare, suitable for wire bonding
- With a pad layout suitable for attachment to a standard TAB frame, or with a TAB frame
- With solder bumps, suitable for flip connection. Since die are easiest to solder bump in wafer form, this should be done before dicing and shipping.

One side effect of this requirement is that multiple suppliers provide chips with the same size, pad layout and electrical specifications. One supplier might suffice as long as the extra risk is acceptable. This is rare for chips, however. Chip production is very susceptible to production problems.

- At least two suppliers of the other required package components, such as TAB frames (if not provided by the chip supplier) and heatsinks.

- Manufacturers who can assemble all of these components, determine if they work correctly, and repair them, if needed. Providers of unpopulated MCMs also could offer this service. Standards are required so that automated assembly equipment can be developed.

- Computer-aided design (CAD) tools. These tools produce the MCM physical layout (locations of the chips and the interconnecting circuits, for example) and turn this layout into a suitable format for feeding to production machines. Ideally these tools automatically produce a design that functions correctly.

- Computer-aided engineering (CAE) tools to help in early design decisions, such as which MCM technology to use and to verify that the design will work. The verification step requires simulators to verify the logic design, the electrical properties of the interconnection and package structures, the thermal design, and the test plan. Other verification tools check that the manufacturing design rules have been followed and that the design will have no yield or other manufacturing problems.

  All of these tools should be seamless in that the designer should not have to re-enter information that is described already in another tool. For example, the designer should be able to simulate an interconnection structure by "clicking" on it in the layout; he or she should not have to type in a simulation file.

- Computer-based libraries. These libraries should provide physical information, including die size and pad location, as well as information

needed to simulate the design, such as logic models of the circuits and package structures, thermal models of heat dissipation and package properties, test models of the chip, and the MCM design rules. Again, these libraries should be seamless. The designer should not need to type in or move data between programs in order to do the design. For example, clicking of the interconnection to be simulated should allow appropriate models to be pulled from the libraries automatically.

- Information and training. *This book is an element of the infrastructure!*

As of today (mid-1992), not all of this infrastructure is in place, particularly in the United States and Europe. (Japanese companies tend to be large and vertically integrated, or to have such close relationships with supplier companies that they are effectively vertically integrated.) This picture is changing very rapidly. Next we summarize the current infrastructure and how it is changing.

Though many MCM foundries exist, only a few can manufacture MCMs in high volume. Those that can often are using lines that were previously internal to vertically integrated companies. In the future, more of the smaller companies need to be able to provide volume manufacturing of MCMs once the need for such high volume exists. The work of standards committees to develop standard MCM sizes and second level packages hopefully will enable a designer to obtain the same MCM package from multiple sources. This activity also should enable equipment manufacturers to produce equipment that can handle and assemble these MCMs automatically.

Until very recently, guaranteed MCM-suitable die were available only at a high price premium over the equivalent packaged part. Several service companies are providing these parts, buying wafers from the chip manufacturers, and testing them. One chip manufacturer recently announced the availability of tested, guaranteed bare die, at the same prices as the equivalent packaged part [6]. Hopefully, as demand increases and the cost of at-speed bare die testing and burn-in decreases, more manufacturers will offer this service at a price *less than* the equivalent packaged part.

Currently, obtaining multiple sources of bare die with the same pad locations and in the same size is difficult. Manufacturers may need to collaborate. For TABed (or TABable) die to become available, for example, standard pad sizes and locations are needed, as well as standard TAB frame sizes (see Chapter 9). For solder bumped die to become pervasive, more chip companies will need to license or develop a solder bump technology. One helpful development would be for a foundry to add solder bumps to die in wafer form obtained from chip suppliers.

CAD and CAE vendors provide many good computer tools. However, seamless operation with each other and with libraries is not quite there. More

agreement between the tool vendors is needed. Part of this agreement could be in the form of common frameworks for information exchange between tools. A small number of frameworks are emerging that provide this commonality. Seamless libraries require that the CAE vendors and the library providers (the chip and MCM manufacturers) agree to common formats for this information.

Achievement of much of the above infrastructure requires agreement in a competitive environment. Most companies recognize that this agreement is necessary for their own commercial success. A number of forums exist for the required consensus building effort. These forums have been provided through professional and industry service organizations, such as the IEEE, ISHM, IEPS, IPC, EIA, JEDEC, SRC; by the government (particularly DARPA, DOD-Air Force, Army); and by Consortia (particularly MCC and MCNC).

MCM vendors may copy profitably the approach of vendors of ASICs (Application Specific Integrated Circuits). Such vendors provide standard packages, high level CAD descriptions of their gate arrays, and quick turnaround. MCM equivalents would include: industry standards for new MCM packages; high level CAD descriptions of microprocessors, logic and memory chips; CAD aids for analyzing propagation delay, reflections, crosstalk, and final noise margin; and CAD thermal design tools. Much of the engineering can be done in advance of specific customer requirements, not only to produce faster turnaround, but also to improve reliability. Increased volume relative to total custom products also will provide a cost advantage.

Last but not least, training and information is needed. This book fulfills part of that mission. Conferences and seminars also provide part of this information. Universities have been slow in providing interdisciplinary courses in packaging technologies. This book will help overcome this by serving as a possible course text. Training courses for faculty, with government and industry-provided support to attend such courses, have been successful in the past for other important emerging technologies. The chip design industry, in particular, has benefited from this activity in the past. Now it is the turn of the electronics packaging industry!

1.6 DECISION-MAKING AS A PROCESS

With the introduction of MCMs, the number of packaging alternatives available to the designer, and the number of decisions that must be made, have increased substantially. The case studies presented in Part C of this book provide unique examples of the decision-making process. The descriptions there of the decision-making process emphasize the decision to introduce an MCM technology and then designing into it rather than just describing the reported

results. In this section, we describe some general features of the decision-making process.

Engineering, managerial and marketing personnel together have to decide on the packaging alternative that best meets the need of their customer. An MCM technology provides a significant performance premium for the customer, but possibly at additional cost and schedule risk. Together with engineering staff, the manager needs to determine the impact of the different packaging technologies on performance and cost. Marketing and sales staff need to be provided with a clear understanding of what these new technologies are providing for their customers.

Knowing what packaging alternatives are available, we first investigate possible applications for MCM technologies by looking at the market.

1.6.1 Determining the Application: Possible MCM Markets

Though any such classification is somewhat arbitrary, it is possible to identify six categories of electronic systems:

1. **Consumer Products:** Included are consumer entertainment products, home appliances, and personal communications products, such as wireless (cellular) telephones
2. **Aerospace and Military Products:** Included are avionics, satellites, and military communications equipment
3. **Computers:** Classified broadly into the following subcategories according to applications and relative importance of performance and cost factors:
   - *Low-end computers*, such as PCs used for general office applications for example, word processing. Low-end computers can be defined as computers designed for users who wish to minimize cost.
   - *Mid-range computers*, such as workstations and servers used mainly for technical applications, for example, circuit simulation. Mid-range computers can be defined as computers intended for users who wish to maximize the ratio of performance to cost.
   - *High-end computers*, including supercomputers and mainframes used respectively for specialized scientific applications such as climate modeling and for applications requiring the rapid processing of large amounts of data such as airline reservation systems. High-end computers can be defined as computers intended for users who wish to maximize performance.

- *Portable computing products*, including notebooks
- *Peripherals* including input/output devices (scanners, printers, disks, screens)
- *Embedded computers*, such as machinery controllers and automobile computers

4. **Biomedical Systems:** Included are items such as office ultrasound machines, large CAT scanners and human-embedded devices
5. **Telecommunications:** Included are centrally provided equipment, such as switches, PBXs and their line cards, for example
6. **Instrumentation:** Included are oscilloscopes and test equipment

Each of these categories has somewhat different packaging needs.

The electronics parts usually found in consumer electronics do not have high pin counts (64 pins is a maximum typical count) and do not require high speed interconnection delays. Thus these systems usually use plastic single chip packages or, if small size creates a selling advantage, chip-on-board packages (the cheapest form of a bare chip mounted package). For example, most hand held calculators use a chip-on-board technology.

The majority of aerospace and military electronics systems are either signal processing or communications systems. Several examples are given in Chapter 15. In a signal processing system such as a radar processor, high circuit speeds are not usually required. Instead, additional system performance is achieved by having many chips working on the same signal at the same time. (However, there has been a recent trend to greater use of high speed chips in military electronics.) Though these chips may have only moderate I/O pin counts, the system size and weight can benefit enormously from MCM technology, and thus their use in this domain is common.

To obtain peak performance out of a computer, high I/O count parts must be connected with the shortest possible interconnection delay. (This is discussed in Chapter 3.) For example, the DEC 21064 RISC microprocessor, found in workstation products, is packaged currently in a 431-pin ceramic PGA and runs at 150 MHz. Even small computers tend to have high pin counts. For example, the Intel 386SL microprocessor, found in the current generation of notebook computers, is packaged currently as a 132-pin (LGA) and runs at 25 MHz. To pack these high pin count chips in a small space and to achieve small interconnection delays, most mid-range computer manufacturers are considering the use of MCM technology. Notebook computer manufacturers are seriously considering laminate (MCM-L) technology, as it provides considerable performance improvement, mainly through reduced size. Workstation manufacturers are considering both laminate and thin film (MCM-D)

technologies, and several have constructed prototypes. Very low-end computers, such as PCs costing under $1000 (1992 dollars), seek performance advantages but cost dominates and thus they use plastic single chip packaging.

High-end computer manufacturers have been using MCM technology, mainly ceramic (MCM-C) technology, for many years. As it is not currently possible to manufacture a high speed mainframe processor as a single chip, MCM technology enables high-end computer manufacturers to interconnect many chips and make a "virtual" large chip as an MCM. They require the highest performance out of MCM technology. Examples are given in Chapters 14 and 17.

Embedded computer applications, such as a washing machine controller, a printer controller, a fuel injection controller, or even an automobile navigation computer, tend to be low performance applications. As pin counts and clock speeds are not high, and space is not usually at a premium, advanced MCM technology has little to offer. However, ceramic hybrid circuits have been used for a long time in automobiles as a means to cope with the harsh environmental conditions. Plastic packages provide insufficient protection in this hot, hydrocarbon-filled environment, and hermetic hybrid packages provide a reasonable cost alternative.

Typical biomedical systems would be a computer aided tomography (CAT) scanner, or an implanted defibrillator. Much of the electronics in a CAT scanner is used for signal processing, similar to applications in military systems. However, since size is relatively unimportant, these systems do not need advanced MCM technology. Size is important in implanted systems, but the electronics parts in such systems have been neither high pin count nor high speed. Nevertheless, high pin count electronics parts are appearing in new implanted systems, and hybrid circuit packaging may no longer suffice.

Telecommunications equipment, such as large switches, tend to require both high speeds and large amounts of wiring. The telephone industry is looking very seriously at MCM technology for the provision of these functions.

Instrumentation such as oscilloscopes and test systems places unique demands on its electronics in that it must operate faster than the electronics in the system it is used to observe or test. Hybrid circuits often have been used in such systems and the use of newer MCM technologies is anticipated.The performance and cost considerations associated with these different systems are discussed also in Section 3.3.

1.6.2 Determining the MCM Technology: Business Decisions

Once a particular market application seems attractive for further consideration, many decisions must be made. Fundamental business issues include whether to

develop an internal capability or to use the contract services of another company, whether to try to change the technology with each new product, or to try to identify and develop a technology that will apply to several products.

Customer requirements for electrical performance, package size, unit cost and time-to-market must always be met. Such considerations dictate many of the choices in choosing an MCM technology. At the same time, there are always alternative choices for some aspects of every technology. It is important to recognize the cost and time-to-market advantages gained by exploiting any design or manufacturing infrastructure (and its accompanying expertise) that exists already, and that may be available within a company. For example, in a company with ready access to silicon IC design and fabrication resources, it probably will be cost effective to utilize an MCM-Si architecture. Similarly, assuming that the same desired performance specifications can be met, a company with skills in ceramics and thick film chemistry might initially pursue development of an MCM-C architecture.

On the other hand, if it is desired to do more than demonstrate the MCM concept, or to provide a limited number of application specific MCM prototypes, it is necessary to look at the longer range capabilities of a given MCM design to avoid being locked into an inflexible technology. It is important also to consider outside vertically integrated companies (IBM, DEC, Hughes, HP to name only some) that are willing and able to sell designs, components and functional subsystems. A readily accessible infrastructure greatly eases entry into the MCM business and provides a technology capable of meeting all the initial performance requirements. Such an infrastructure may be ill-suited for scaling up to large volume production or may be incapable of meeting expected future performance requirements. For example, a wire bond MCM-L architecture may represent a good route into the business, but an investment in flip chip MCM-D technology will have to be made eventually if exceptional high frequency performance is a long-range objective.

The importance of automated production using standard parts needs to be emphasized. As long as MCM technology development is focused on highly customized forms for small production runs, MCM costs will be high. Automation and standardization are necessary for cost-effective medium and large MCM product runs. This means the selection and refinement of MCM processes and designs appropriate for high speed automated batch processing, assembly and testing. As far as possible, these MCM technologies also must exploit the generic assembly and testing tools and standards that can be shared across a broad (industry wide) design and manufacturing base. In this case, even MCM-D may become a high volume cost effective alternative to VLSI integration and conventional packaging, and quickly claim its rightful share of the market!

1.6.3 Designing the Product: Multidisciplinary Engineering

With the growing need for aggressive packaging technologies, an interdisciplinary approach is needed for the engineering decision making process. Until recently, electronic package engineering was a discipline concerned mainly with manufacturing and reliability issues. Other engineers, separately, could take the package types offered by the package engineers and design products that met their required specifications. Today unfortunately, this strategy is no longer possible.

Key decisions in packaging involve detailed materials, manufacturing and reliability issues as well as electrical and thermal knowledge. Now design and systems engineers need to understand packaging technologies because package performance has become critical to their design function. Until recently, the choice of packaging technology was obvious once the chips were defined. Now this is not the case.

Even if a strategic direction in packaging technology has been selected, there are other subchoices and decisions still to make. Thermal design has become more intensive in nature. A different perspective is needed in electrical design. Managing the test process, for example, must be given a higher priority than previously. More effort must be spent on understanding materials and manufacturing issues as now their effect on cost, and their interaction with system function, is greater.

"Concurrent engineering" refers to cases where design and manufacturing decisions have to be made early and with the interaction of many different kinds of engineers. MCM product design clearly is one of these cases.

1.7 OVERALL PROSPECTS FOR MCMs

In this book, we consider not only various MCM alternatives, but also the other alternative: ***"None of the Above."*** Why MCMs at all? Two major perceived impediments to the widespread production of MCMs are:

- **Design Time**: Designing an MCM generally takes longer than designing the equivalent PWB. Then why bother with the new complications of MCMs if single chips will have the same performance and density by the time an MCM system is finally brought to market?
- **Cost**: Even if the design time can be reduced, will sufficient investment ever be made in U.S. production of MCMs to make their costs competitive?

With regard to design time considerations, a number of points should be made. First, as MCM technology becomes more pervasive, the additional design time overhead will decrease to the point where it is not a serious factor, particularly with proper application of concurrent engineering techniques. Second, many MCMs contain a mix of semiconductor technologies (such as digital, analog, memory, silicon and GaAs) and cannot be replaced by a single chip. Third, large MCMs contain so many transistors that a single chip equivalent will take a long time to develop. Fourth, it does not make sense to design a custom chip for a low volume application. An equivalent MCM will often make sense, however. Finally, design time is not an important factor in many applications where product lifetimes are long, for example, in military applications.

Even in today's commercial markets, however, relatively long life cycles are possible. Systems based on popular microprocessors sometimes fall into this category, and it is encouraging to see that Intel, for example, is beginning to offer bare die of its popular chips [6]. Secondly, even large computer systems are gravitating towards parallel processing based on microprocessors. The size advantage of MCMs is attractive here, and a single modular design might be used over and over to add on processing capability. Another possibility for MCMs lies in designing systems such that the MCMs can be replaced later with improved chips having equivalent performance and I/Os without affecting the rest of the system [8].

With regard to costs, there is serious concern that MCMs will never be commercially viable in the U.S. without the commitment of long term investment. The case of Group 3 Fax technology is cited [9], where investment in the U.S. was withdrawn prior to the development of a large volume market that ultimately drove the costs down. Suggested solutions to this problem include direct government support and management enthusiasm for an initial high volume capability [9], an improved government climate for long term investment and better marketing forecasts [10]. These solutions, however, are not under the control of the individual small or medium size manufacturer.

Not only are initial MCM costs high because the technology is new, but also because there are new design and testing interfaces between chip makers, MCM producers, and systems houses [11]. Long term working relationships need to be initiated within the industry to reduce costs associated with these interfaces [10]-[11]. Costs may be lower in the long run if systems people pick qualified suppliers and give them some confidence in a stable market while helping them develop the needed standards and interfaces. Trying to maintain the usual lowest bidder approach can be counterproductive, because then no supplier may wish to invest in the volume production capability that will drive the cost down.

Several chip makers (Intel, Motorola to name only a few) have taken the initiative, without waiting for support from systems houses. They have not only offered bare die of their popular chips, but they have started offering fully tested units ("known good die") [6]. Bare die testing eliminates an uncertainty leading to possible low yield of more expensive MCM units with several chips.

Ramp-up of MCM production may also occur fairly gradually. Since there are different possible systems and different MCM technologies, there is not the all-or-nothing quantum barrier of the Group 3 Fax technology cited above. MCM production may start out meeting market needs for "few chips packages" [12].

MCMs also offer the unique capability for optimized chip technology. No longer must different types of circuits be built on the same chip. Instead a single IC fabrication process can be used for an entire chip. For example, RAM processes can be used for RAMs, logic processes for CPUs, analog processes for CODECs and GaAs, if needed.

A promising niche for commercial MCMs in the short term is in systems where small size is absolutely essential, but the ultimate in performance is not [6]. One possible example is portable communication products [13]. The reduced interconnection complexity associated with MCMs also is attractive in these applications.

High performance systems where the speed is limited by the number of I/Os available on a single chip package are a longer term candidate for MCMs [14]. Reductions in the number of second level connections also should lead to higher reliability in these applications. MCMs have another unique advantage in their huge array contacting capability (see Chapter 18). Finally, MCMs can provide optimal functional performance, if signals only have to travel at high speed between chips within the same MCM package.

High performance alone, however, is not now a sufficient driving force for volume MCMs. Intel recently dropped its production of an advanced MCM for the reason cited at the beginning of this section: the next generation chip device came out with performance comparable to the MCM [6].

Many of these issues are discussed in more detail in Chapter 18. We hope that this cursory view sparks your interest!

1.8 SUMMARY

MCMs offer the potential for increased chip density leading to reduced size of electronic systems. Together with reduced size, MCMs offer a number of advantages. The speed performance is improved due to smaller chip spacings

and reduced parasitics. Reliability is improved due to the reduction of the number of second level connections.

The successful use of MCM technology requires careful application. The alternatives and the economic issues that affect its use must be considered. Currently, MCM components are more expensive than the equivalent collection of single chip components and PWBs. Sometimes, an advanced technology custom chip will make sense over a small MCM, particularly a high volume application. If that solution does not make sense, then MCM technology must be considered seriously in any performance-driven application. In any case, a large system built out of MCMs might be less expensive actually than the equivalent single chip package system due to substantial savings in total size.

If MCMs are to be used in an application, full consideration should be given also to the effects of infrastructure, standardization and automated assembly on the part to be used. Careful, concurrently engineered design is required.

The main challenge to keep in mind while reading this book is how to realize these potential advantages of MCMs for applications you may have. Technologies must be developed and chosen so that the MCMs are not hindered from reaching their potential. In particular, an MCM should maintain the performance of its component chips with minimal degradation. The material in Part B of this book will help in developing the required technology. The examples in Part C will help in making the right technology choices. Part D will help to verify whether you have made the right choices. ***We wish you success in an exciting adventure!***

Acknowledgments

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2

MCM PACKAGE SELECTION: A MATERIALS AND MANUFACTURING PERSPECTIVE

Allison Casey Dixon and Edward G. Myszka

2.1 INTRODUCTION

Multichip packaging is receiving increased attention as electronic equipment manufacturers drive toward smaller, faster and less expensive products. By connecting several chips together in a single package:

- Board size can be reduced by up to a factor of 10 or more
- Signal propagation between chips can be up to three times faster
- The number of solder connections in a system can be reduced

Even so, multichip modules (MCMs) will be utilized only where they are the least expensive method of meeting system requirements. The choice of MCM materials and manufacturing processes greatly influences the cost of a multichip module technology in terms of piece part cost, manufacturing yield, manufacturing cycle time and repairability. Materials choices are also dominant factors in the electrical and thermal performance of a module. There is no single "right" choice; rather, different choices are appropriate for different applications.

This chapter presents the technology choices available today for the various parts of an MCM described in Table 2-1 - signal interconnect, substrate base, MCM substrate, package body, chip mounting and module level connection.

Different combinations of these parts are used for different MCM technologies. Some of the typical combinations are sketched in Figure 2-1. Comparisons of manufacturing flows, materials properties, performance and cost are emphasized in this chapter, along with the concept that there are no "right" choices except in light of a specific application.

After the technology choices are described, global material and manufacturing related issues are discussed - cost, performance, thermal path, rework and manufacturability. The chapter concludes with some examples of modules designed for given applications.

Table 2-1 Multichip Module Parts.

PART	DESCRIPTION	EXAMPLES
Chip Mounting	Electrical and mechanical connection of chip to substrate.	Die attach/wire bond, TAB, flip chip
Package Body	Additional structural support, environmental protection and signal connection to outside world.	Ceramic packages
Substrate Base	Structural support for the signal interconnect. Signal interconnect may be deposited in the substrate base or the substrate base may be an integral part of the signal interconnect.	Silicon, ceramic, organic laminate, metal
Signal Interconnect	Metal and dielectric patterns forming the circuitry between chips.	Copper/polyimide, tungsten/alumina, aluminum/silicon dioxide.
MCM Substrate	Signal interconnect plus the substrate base, may require an additional package.	MCM-C, MCM-L, MCM-D, MCM-D/C, MCM-Si
Module Level Connection	Electrical and mechanical connection of module to motherboard. Integral part of either the MCM substrate or the package body.	PGA, PAC, gull wing lead

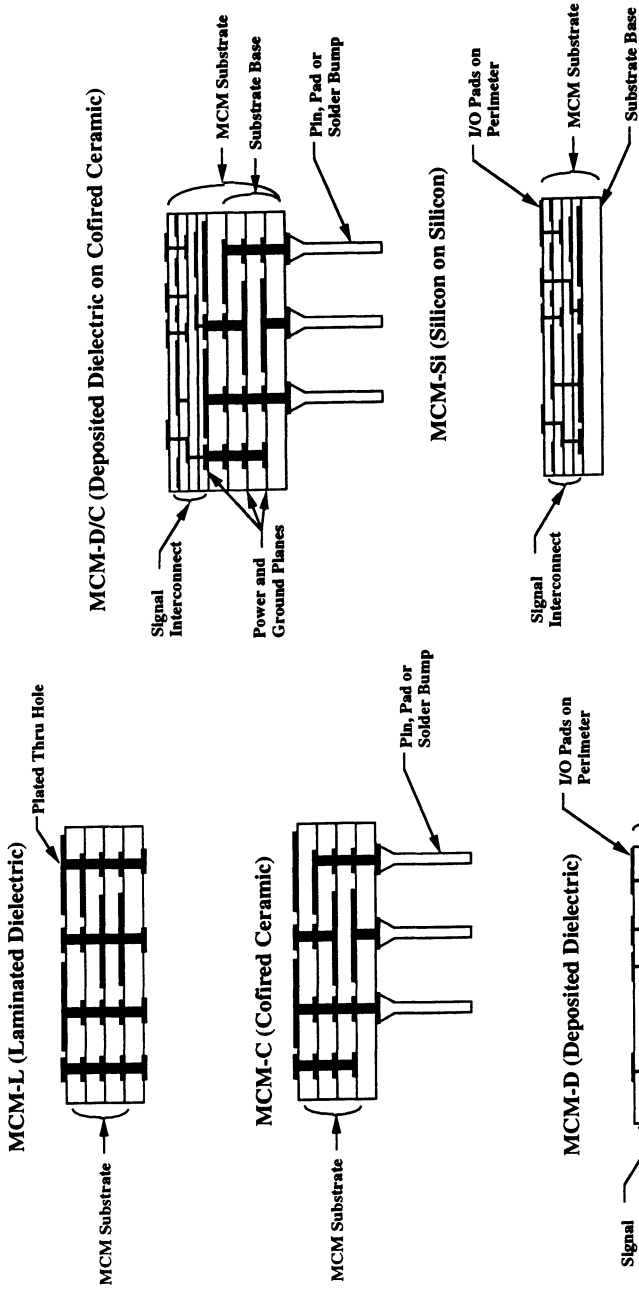


Figure 2-1 Typical MCM design configurations.

2.2 PACKAGE BODY AND SUBSTRATE BASE CHOICES

The package body and substrate base are the structurally robust piece parts that form mechanical support for the MCM. The package body is simply a housing for the module. Some module technologies require use of a package body, and others do not. In Figure 2-1, the MCM-D and MCM-Si modules will need a package body to house the fragile module and to provide electrical connection to the outside world. Typically, an MCM-D or MCM-Si module is wire bonded to a ceramic package body. The package body provides mechanical and environmental protection and a means to attach pins or leads to transfer electrical signals to the outside world. In some cases, a package body is not necessary because the substrate base, the structural support for the metal and dielectric patterns forming the circuitry between chips (signal interconnect), provides sufficient mechanical support and a means of electrically connecting the module to the outside world.

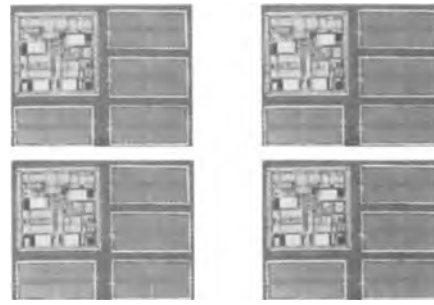
The various types of MCMs are sketched in Figure 2-1. Figures 2-2 shows photos of an assembled module and the MCMs packaged parts used to fabricate it. The MCM-L, MCM-C, and MCM-D/C modules make use of integrated MCM substrates that do not require use of a separate substrate base or package body. MCM-D and MCM-Si, on the other hand, utilize all three parts: substrate base, MCM substrate, and package body.

Three general classes of materials may be used for package bodies or substrate bases: ceramics, organic laminates and metals. Important characteristics of these materials are summarized in Table 2-2 and are discussed below [1].

2.2.1 Ceramics

Ceramics used in MCMs have several advantages. Foremost of these is that a properly designed ceramic piece part can serve as the module package body, the MCM substrate, and the module level connection — all in a single integrated part. Ceramics are electrically non-conductive, simplifying module design. They can form part of a hermetic package easily.

Alumina (also known as aluminum oxide or Al_2O_3) is the most common, inexpensive and widely used ceramic substrate material. Alumina may be used in an MCM as either an MCM substrate or as a stand alone package body for MCM-D or MCM-Si type modules. There are two general forms of alumina used – multilayer cofired alumina, which can contain conductive metal traces or planes, and single-layer pressed alumina. Multilayer cofired alumina is made from individual layers of unfired material (called "green tape") which can be patterned with conductive metal traces. Many layers (up to 50 or more) can be stacked together and fired at high temperatures to form a single unit. Further



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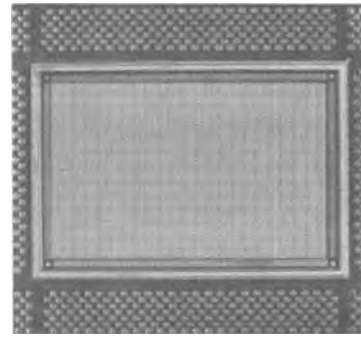

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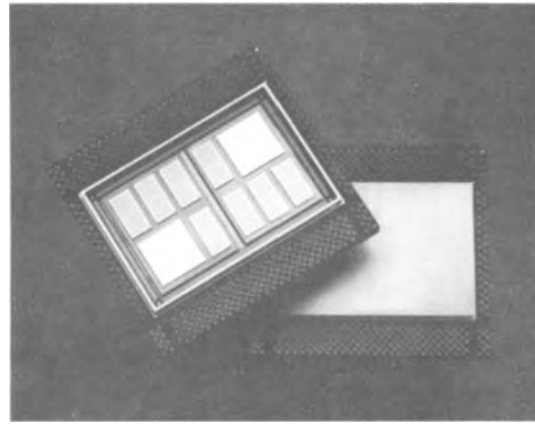

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Figure 2-2 MCM-Si package showing (a) chips on silicon substrate forming module, (b) ceramic package base and (c) assembled MCM package.

Table 2-2 Properties of Package Bodies/Substrate Bases.

	Formula	Cost	Availability	CTE (10^{-6}/°C)	Thermal Conductivity (W/m-K)
Pressed Alumina	Al_2O_3	X	Excellent	8.1	30
Aluminum Nitride	AlN	4X	Poor	4.3	260
Silicon Carbide	SiC	2X	Poor	3.7	270
Mullite	3 Al_2O_3/ 2 SiO_2	X	Poor	4.5	2-6
Glass Ceramic	Various	X	Fair	3.0-4.2	5
Organic Laminate	Various	0.5X	Excellent	12.0-17.0	0.2-0.3
Metals	Various	0.3X	Good	6.0-20.0	200-400

Note: Silicon, CTE = 3.5 x 10^{-6}/°C.

processing details are discussed in Section 2.3.1 of this chapter and in Chapter 6. Cofired alumina is a mature technology with highly automated factories in place. Its major disadvantages are shrinkage and warpage. These factors are controlled tightly in the manufacturing process and compensated for in the design process. Shrinkage and warpage limit the density of conductive metal traces on a cofired ceramic MCM due to the additive tolerance of each layer. Shrinkage and warpage also cause problems with mounting high lead count, tight pitch chips in cases where the planarity of connection points is critical. Figure 2-14b (discussed in Section 2.7.2) is an example of a prototype workstation module utilizing cofired ceramic as a substrate base.

Pressed alumina is a single sheet of ceramic material that is independently fired. Pressed alumina does not contain conductive traces or planes and serves strictly as a package body for MCM-D or MCM-Si modules or as a substrate base for MCM-D/C modules.

As shown in Table 2-2, alumina is a poor conductor of heat relative to other ceramics. It is, however, orders of magnitude better than organic laminates. Alumina has a coefficient of thermal expansion (CTE) more than twice that of

silicon. When silicon chips are mounted on alumina, thermal expansion mismatch creates stress that can cause material fatigue, leading to premature failure.

New ceramic materials aimed at improving CTE and thermal conductivity are currently in prototype production. Some of the most promising materials such as aluminum nitride, silicon carbide and mullite, are listed in Table 2-2 for comparison with standard alumina.

2.2.2 Organic Laminates

Organic laminates, commonly referred to as printed circuit board (PCB) or printed wiring board (PWB), are used in many different forms for electronics packaging. In MCMs, organic laminates are used most often as an integrated package body and MCM substrate. In general, sheets of polymer materials (polyimide, FR-4, BT resin plus glass reinforcement) are sandwiched between layers of metal (usually copper) traces. The stack up is then bonded by lamination in a hydraulic press or autoclave under heat and pressure (350°F and 325 psi for standard FR-4). Further processing details for laminate-based MCM technologies are described in Chapter 5.

Like ceramics, organic laminates have the advantage of combining package base and MCM substrate functions into a single piece part. Another advantage of organic laminates is the match of their CTE to the mother board. Any MCM will be mounted eventually on a PWB. The organic laminate-based technology typically has the lowest manufacturing cost of all module technologies because it is mature and employs both batch and parallel processes (see Section 2.3.2). The major disadvantages are very poor thermal conductivity, a CTE four to five times that of silicon, and warpage. Figure 2-3 is a photograph of an organic laminate MCM substrate, consisting of seven copper layers, BT resin dielectric and an embedded leadframe.

2.2.3 Metals

Metals also are used as package bodies for MCMs [2]. Often metals are chosen for high power MCMs because of their excellent thermal conductivity. Metals also provide a very rigid and flat surface for signal interconnect layers within the module. The major disadvantage of using metals as package bodies is that signal connections cannot be made directly through the metal to the outside world.

2.3 SIGNAL INTERCONNECT AND MCM SUBSTRATE CHOICES

Module signal interconnect refers to the pattern of metal and dielectric that forms the circuitry between chips and from the chips to the outside world. As

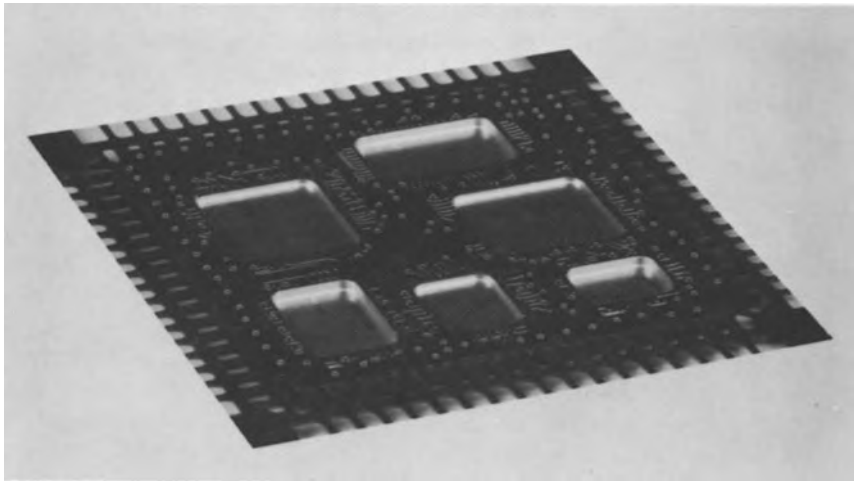

Figure 2-3 Organic laminate MCM.

discussed in Chapter 1, there are many MCM substrate types available. MCM-C, MCM-L, MCM-D, MCM-D/C and MCM-Si, as well as conventional thick film hybrids, are all available today. The MCM designer is faced with many choices for the fundamental technology, as well as in the selection of materials used within each of these technologies. The selection of the dielectric material, as well as the conductor material, also strongly influences the overall performance of the module. This is true especially for modules containing high speed digital and mixed analog/digital components with switching frequencies in excess of 50 MHz or switching rise times less than 2 ns. This section focuses on the description of the core MCM technologies and processes and the materials which are available to manufacture such MCMs.

There are many materials used as conductors for MCM applications. Copper (Cu) and aluminum (Al) are utilized as conductors for MCM-D, MCM-D/C and MCM-Si applications. Copper is preferred for its lower resistivity. Copper is being used also in experimental MCM-C modules fabricated at low cofiring processing temperatures. Gold (Au) is used occasionally for MCM-D and MCM-D/C, but its relatively high cost prohibits its use in most commercial applications. Refractory metals such as tungsten (W), molybdenum (Mo) and manganese (Mn) are used in high temperature cofired ceramic processing. These metals are selected for their high melting points rather than for their electrical properties. Metals such as W, Mo and Mn are electrical conductors able to withstand the

high (1500°C) firing temperatures required to sinter the ceramic layers together to form a monolithic multilayer MCM-C substrate.

2.3.1 MCM-C (Cofired Ceramics)

Multilayer ceramic structures have been designated as MCM-C. Further details on ceramic-based technologies are given in Chapter 6. This type of MCM can be categorized in two groups: those processed at high temperature (HTCC) and those at low temperature (LTCC). HTCC has been available for decades and is used most commonly [3]. Refractory metals such as W, Mo, and Mn are used as electrical conductors in HTCC processing. These metals are selected because of their inherent high melting point. These metals remain stable and do not decompose during the sintering process where temperature extremes can reach (1500°C). Low temperature cofiring, although fairly new to the industry, has generated a great deal of interest. The ability to use highly conductive noble metals such Ag, Au and, most recently, Cu as the conductor offers many advantages over HTCC modules [4]. Unfortunately, since this technology is quite young and its penetration into the market relatively small, the substrate cost can be as much as 70 – 100% higher than HTCC substrates. As the market penetration increases, this disparity is anticipated to decrease. In the cofire processing for both the high-and low-temperature technologies, a liquid slurry is formed from ceramic particles and organic binders and then cast into a solid sheet. This sheet is often referred to as the "green tape" because of its unfired state. Typical costs for moderate production volumes associated with green tape are $0.06 and $0.11 per square inch for HTCC and LTCC, respectively [5].

Next, holes for vias are generated in the green tape. The most commonly used via diameter sizes range from 0.015 – 0.008" with more aggressive designs reaching 0.004". Vias can be drilled, but are formed more commonly by a punching operation. Punching can be accomplished by a single punch head positioned sequentially at each site by computer numerical control (CNC). This often is referred to as "soft tooling." Alternatively, a custom die head that simultaneously punches all the vias on a single layer is referred to as "hard tooling."

Soft Tooling versus Hard Tooling

The nonrecurring engineering cost (NRE) for hard tooling is higher than soft tooling, but the unit price is typically lower. The decision on which type of tooling to be purchased is a function of the anticipated volume. For low volume runs, soft tooling NRE, which

can average $30,000 for an eight layer module, can be cost effective. Conversely, for high volume applications the cost of hard tooling, which can exceed $60,000, can easily be amortized over the life of the product to produce a cost effective solution. One disadvantage of soft tooling is that there typically is a maximum run rate associated with the tool. That is, there exists a maximum number of modules that are built and shipped each month. This is typically associated with the existing fabrication throughput capabilities.

After the green tape sheets are formed and via holes drilled or punched, a conductive ink (a refractory metal for HTCC MCM substrates or a noble metal for LTCC MCM substrates) is applied to each layer through a screen printing process (see Chapter 6). 10 mil lines are standard and 4 mil lines are readily fabricated using this process. Vacuum can be applied to the underside of the punched sheet to pull the ink into the hole to coat the side walls or, in many cases, to fill the via. Solid vias are advantageous for high density applications because they can be stacked directly on top of each other, otherwise the vias will be staggered and hence require additional area.

After patterns are screened on each layer, the layers are stacked and the assembly is fed into a furnace and fired at temperatures above 1400°C for the high temperature process and approximately 800°C for the low temperature process. The result is a monolithic structure containing all the interconnects.

During the firing process the organic binder decomposes, the ceramic densifies and, unfortunately, the structure reacts by shrinking. This shrinkage becomes a problem during the subsequent assembly of chips where precise positioning of the chip connections is required. This is true especially of high density tape automated bonding (TAB) and flip chip interconnects where the I/Os are fixed. If wire bonding is used as the chip connection method, an automatic wire bonder with look-ahead vision (an optical pattern recognition system that determines the precise location of bonding pads used to make small adjustments to accommodate substrate shrinkage) can be used. Another solution is to deposit a thin film layer of metal or copper/polyimide after firing the ceramic to facilitate chip connection of high I/O devices. This postfire processing can be provided only for the outermost surface of the module.

Thermal solutions in an MCM are accommodated typically by placing vias strategically under the chips (thermal vias) and/or by brazing a Cu/W heatsink to the ceramic structure. Figure 2-4 shows a single chip multitiered cofired ceramic package with an integral Cu/W heat spreader designed to dissipate up to 30 watts. These features can be implemented readily for multichip packaging, but they can come with both cost and electrical performance penalties.

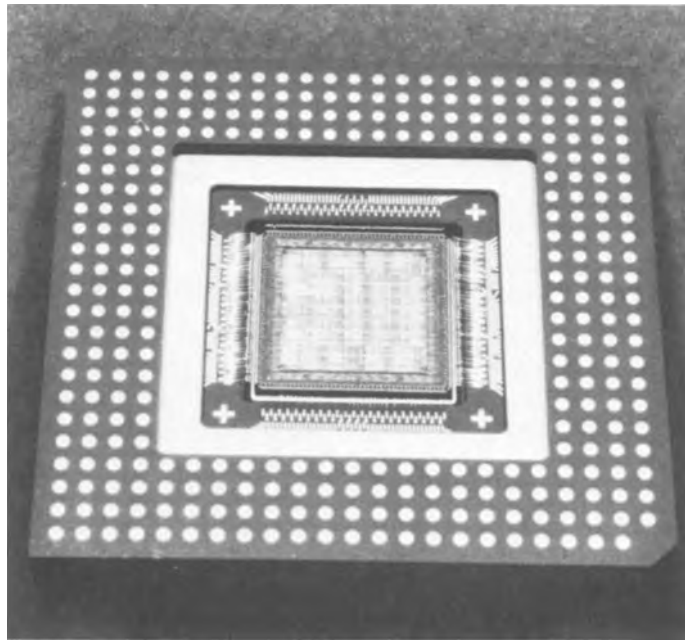

Figure 2-4 Single chip multitiered cofired ceramic pad array carrier (PAC) package.

One of the major disadvantages of cofired alumina is its relatively high dielectric constant (ε_r) which can limit the performance capability of MCMs (Section 2.6.2). Since the performance of a module is influenced heavily by design layout as well as by material selection, no rigid cut off exists for using cofired ceramic technology. Modules have been built and tested at clock frequencies in excess of 50 - 75 MHz. New ceramic materials with lower dielectric constants, such as glassy ceramics (Table 2-2), have been developed for modules operating in excess of this. The next section presents a brief description of several of these materials.

Low Dielectric and Glassy Ceramics

The most well known glassy ceramic was developed by IBM. These ceramics have low cofiring temperatures which make them co-sinterable with either Cu or Au conductors. Additionally, the materials have a low dielectric constant and mechanical properties which may be tailored for a particular application. Others are attempting to modify the material properties by introducing particles suspended in the ceramic matrix. Upon sintering, or through a post annealing

treatment, porosity is introduced to the matrix [6]. Since the dielectric constant of the gaseous material produced by the porosity is very low, the effective dielectric constant of the assembly is also low. Experimental data on research grade materials suggest that the effective dielectric constant can be reduced to approximately 2.5. These materials hold great promise but first must prove compatibility with metal films and the ability to withstand the environmental testing required to become a reliable substrate material.

High Thermal Conductivity Ceramics

Attention is being focused also on the development of ceramic materials with higher thermal conductivities than alumina. Besides alumina, beryllia (BeO) is the most widely used ceramic in the microelectronics industry, primarily because of its high thermal conductivity. Although cofired structures have not been developed for this material, it has been used extensively as a heatsink for semiconductor lasers and as a substrate base for high power RF applications. The greatest disadvantage of BeO is in its processing. BeO dust and particulates have been designated as carcinogens and, thus, extreme care must be taken when cutting or grinding this material. As a result, aluminum nitride (AlN) has been introduced as an alternative to BeO for MCMs (Table 2-2). AlN has 80% of the thermal conductivity of BeO and can be cofired in a multilayer structure [7]. With these beneficial properties, it is anticipated that AlN will become a cost effective alternative to BeO in the near future.

2.3.2 MCM-L (Organic Laminates)

The MCM-L structures can be regarded as a laminated PWB scaled to meet the requirements and dimensions of a MCM as discussed in Chapter 1. Fabrication methods vary among manufacturers, but, in practice, most techniques closely follow the infrastructure previously developed by the PWB industry. The following section is intended to provide the reader with a brief description of the most widely used fabrication methods, materials and their associated advantages and disadvantages.

Many organic laminate types are used to manufacture modules for various applications. Epoxy glass (such as FR-4) is most common. For applications where material stability is required at higher temperatures, materials such as Bismaleimide triazine (BT Resin) and polyimides with higher glass transition temperatures (T_g) can be used. Laminates can be double clad, single clad or not clad at all. Cladding is thin copper foil applied to the sheet of dielectric material. It is this foil that is patterned to make the conductors. Double clad and single clad refer to the number of sides of the dielectric material which are coated with copper foil. The clad sheets are called "laminates." Several clad

sheets stacked and bonded together are also called "laminates." Copper foil thickness is measured in ounces. For example, a one ounce copper clad laminate will measure 0.0014" thick. One ounce and one-half ounce copper are typical for the PWB industry and one half, one quarter and even less than one eighth ounce can be found in laminates for the MCM-L industry.

Laminate Sheet Types

Copper clad laminates are available in widths in excess of 24" and are fabricated most commonly by either of two methods. Adhesive laminates rely on the application of a copper foil to a sheet dielectric (bare laminate with no metal) with an adhesive layer (typically acrylic in nature). These materials are clad in a rolling press at very high volumes. Conversely, adhesiveless laminates are fabricated by applying the copper directly to the dielectric with no bonding agent. Adhesiveless laminates can be formed in one of two ways: liquid dielectric may be deposited to the foil and cured, or the metal may be electroplated or vacuum deposited to the fully cured laminate material.

Additive versus Subtractive Processing

Copper conductors are patterned using either a subtractive or an additive process. The subtractive process is used typically with thicker copper films. In the subtractive process the pattern is etched directly into the existing metal. Subtractive processing is used predominantly in the PWB industry. Minimum feature sizes typically are limited to 0.003" - 0.004" due to the isotropic nature of the conductor etching process and the dielectric surface roughness.

Alternatively, in the additive process, a photoresist coating is applied and patterned onto the existing thin metal foil. The actual conductor pattern is electroplated onto this foil, the photoresist is stripped and the thin foil is etched away revealing the electroplated conductor. Refer to Figures 7-12 and 7-13. Typical conductor patterns can range in size from 0.001" - 0.003". It is predicted that additive processing in conjunction with smoother laminate surfaces, will enable conductor features less than 0.001".

After the clad laminates are patterned, vias are drilled on a CNC machine. To increase process efficiency, many laminates are often stacked during the via drilling process on machines with multiple spindles. Currently, minimum via size is approximately 0.004" - 0.006" in diameter and is limited by the

availability of reliable drill bits. The copper layers can be patterned sequentially on a single clad laminate or two adjacent layers may be patterned in parallel on a free standing double clad film. The ability to pattern both sides of the laminate simultaneously is a major advantage of MCM-L because it effectively reduces the manufacturing cycle time.

After vias are formed and the Cu layers patterned, each layer can be inspected, an advantage of parallel processing. The inspection of layers prior to final lamination minimizes the possibility of the transfer of defects into the completed module. This early inspection for defects will increase the likelihood of receiving a functionally working substrate. The yielded copper layers are stacked with prepreg (partially cured laminate material) inserted between each layer. The stack is laminated in a press or autoclave with heat and pressure as mentioned previously.

The major disadvantages with organic laminate substrates used today are low routing density, poor thermal conductivity through the substrate and a high CTE, compared to silicon. New materials are being developed to alleviate many of these problems. These materials include advanced polyimides, aramids and fluoropolymers with homogeneous matrices and composite laminates. The electrical (dielectric constant) and mechanical (CTE) properties of many of these materials can be tailored for specific applications [8]-[9]. As the industry progresses to larger ICs with more demanding chip connection methods, such as flip chip, these materials will draw more attention.

For MCM-L applications one noticeable change in the fabrication of the laminate structure is the use of thinner dielectric films. These thin (25 - 50 μm) films allow controlled impedance, high density modules to be fabricated with transmission line design criteria. These fine line capabilities contribute also to the increase in routing density. However, large metallized pads on each layer are required to aid in the via drilling operation. To truly achieve high density modules novel approaches to via generation also will be required. Processes under consideration include wet chemistry etching, reactive plasma etching and laser ablation techniques. Each of these approaches to the fabrication of small vias is anticipated to break the current 0.004" barrier set by the mechanical drilling process and will increase significantly the routing density of MCM-L substrates. Unfortunately, many of the conventional laminates used today are not compatible with these advanced via processing techniques. For example, when using an excimer laser, since the ablation threshold of the glass weave used in conventional laminates is more than an order of magnitude greater than that for a polyimide matrix, processing of vias is complicated. The glass weave thermally decomposes at the high energy densities required to remove it. Similarly, the acrylic adhesives used to bond copper foils to dielectric sheets also have high ablation thresholds. Laminate suppliers have recognized the

limitations of conventional laminate materials and have begun to offer new, more advanced laminates specifically targeted for such applications. Many of these new laminates are adhesiveless and do not contain a glass fiber weave. Instead, these new materials are made up of the pure matrix material or contain small particulates dispersed within the matrix to control its properties and processability. As the industry progresses to more advanced via fabrication techniques, we predict increased use of new laminate materials.

In most cases, laminates are fabricated in a large panel. At the end of production, the layers are cut out of the panel. The ability to fabricate multiple modules in a large panel format is cost effective. However, as the panel size increases, the layer-to-layer registration becomes more difficult. Parallel processing offers the potential to integrate two distinctly different laminate patterning processes: conventional PWB for low density layers (power and ground planes), and advanced fabrication processing, such as laser ablation for high density (signal) layers. Since layer-to-layer registration is less of an issue with low density layers, large panel sizes can be processed. These large panels can be cut into smaller, more manageable panels and mated to panels containing the higher density layers during the lamination process. Additionally, recent advances in the lamination of the multilayer organic structures to leadframes has made it possible to produce leaded MCM-L substrates configured as quad flat packs (QFPs).

2.3.3 MCM-D (Deposited Dielectric)

MCM-Ds are fabricated by a sequential deposition of conductor, typically Cu or Al, and dielectric layers (typically polyimide) on a substrate base made of ceramic, silicon or metal. As the fabrication of MCM-L parallels the PWB industry, MCM-D most closely parallels the processing techniques of the semiconductor industry. Semiconductor type processing provides for very fine lines with high routing densities. However, the semiconductor processing equipment used to manufacture MCM-D substrates is expensive and low volume runs make it difficult to depreciate the high capital costs. MCM-D substrates are fabricated in 4", 5" or 6" round or square "wafers." Fabrication costs are associated primarily with the wafer and not with finished substrate size; that is, a single substrate on a wafer will cost about twice as much as a design where two substrates can be fit onto a single wafer. The cost driver is the number of substrates that can fit onto a given wafer size (number "up").

Another disadvantage of MCM-D technology is that it often requires the use of a separate package body to house the MCM substrate and to make electrical and mechanical connection to the mother board. This results in additional

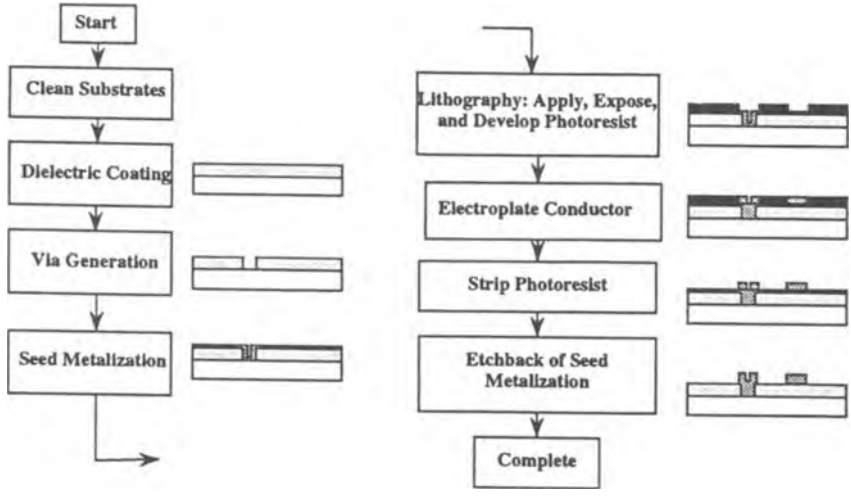

Figure 2-5 Process flow: MCM-D.

assembly operations and higher manufacturing costs. A more cost effective approach to MCM-D is its integration with cofired ceramic. These structures are detailed in Section 2.3.4 on MCM-D/C.

Although MCM-D fabrication processes differ from one manufacturer to another, a common method is presented to give an idea of the processing required to build such a module. Figure 2-5 is a flow chart of a typical process.

A liquid polymer (typically polyimide, but also benzocyclobutene (BCB) and other fluoropolymers) dielectric layer is deposited on the substrate base by a conventional spin coating process. The liquid dielectric material is dispensed onto the center of the substrate and spun until the material spreads uniformly to cover the substrate. Although this is an effective process in terms of uniformity, it is far from efficient. As much as 50 - 80% of the material is spun off and wasted. As typical costs for the polymers can range from $1.00 to $2.00 per gram, and up to 4 grams are required to form a 12.5 μm thick film layer on a 4" × 4" substrate, more efficient, alternative dispensing techniques are needed. Alternative deposition methods under investigation include spraying and extrusion. Dielectric thicknesses of 25 μm or less are typical, and multiple coats usually are required to obtain this thickness with good planarization.

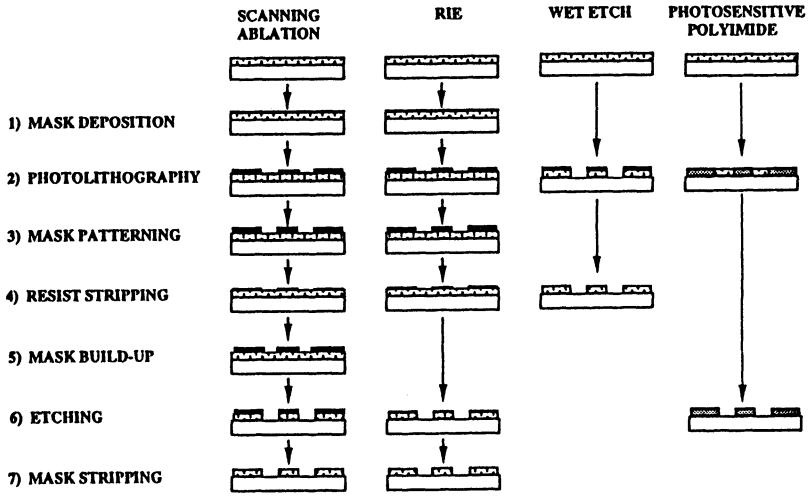

Figure 2-6 MCM-D via formation techniques.

Vias can be formed by scanning laser ablation, reactive ion etching or wet etching of the dielectric, as well as through the exposure of photosensitive polymers. Figure 2-6 shows the comparison of process steps required to form vias. No one method has been accepted as a standard in the industry [10]. Reactive ion etching of vias is commonly used in the U.S. and wet etching in Japan. These techniques are discussed further in Chapter 7.

After the dielectric layer is deposited and vias formed, metal conductors are formed using either additive or subtractive processing. In additive processing, a bus layer metallization for electroplating is first formed either by sputtering or by electroless copper plating. Photoresist is then spun on, the pattern imaged and the bulk pattern is electroplated. The photoresist then is stripped and the bus layer metallization etched away, leaving the electroplated conductor pattern behind. In subtractive processing, the full surface is coated with metal and the conductor pattern etched. The entire process is repeated for each layer. Both subtractive and additive processing are practiced today.

2.3.4 MCM-D/C (Deposited Dielectric on Cofired Ceramic)

Deposited dielectric on cofired ceramic, MCM-D/C, can cost effectively combine the advantages of MCM-C and MCM-D. This technology utilizes deposited

dielectric layers on top of a multilayer cofired ceramic substrate base to produce MCM substrates with all of the high density and high frequency attributes of MCM-D coupled with the flexible physical attributes of MCM-C. This combination provides a single substrate that functions as the signal interconnect, substrate base, package body and module level I/O connection. Vias may be brought out the bottom of the substrate, the package I/Os may be terminated in a pad array carrier (PAC) format or mated with pins to simulate a standard, single chip pin grid array (PGA) package. The cofired substrate is part of the package body, eliminating the cost associated with repackaging of the MCM substrate. The photo in Figure 2-14b is an example of a module that uses a MCM-D/C substrate. In this module there are four layers of polyimide dielectric and thin film copper deposited on a standard 299 pin cofired ceramic substrate.

Another advantage of MCM-D/C technology is that signal lines can be embedded in the low dielectric constant deposited layers to minimize crosstalk, while power and ground planes can be contained in the higher dielectric constant ceramic layers. With the development of high dielectric constant ceramic materials ($\varepsilon_r > 200$), it may be possible to incorporate much (if not all) of the decoupling capacitance within the substrate and eliminate the secondary assembly operation required to mount external bypass capacitors.

2.3.5 MCM-Si (Inorganic Thin Film)

Yet another solution to multichip packaging utilizes semiconductor fabrication techniques directly. This technology, often referred to as silicon-on-silicon (MCM-Si), is processed in a similar fashion to conventional silicon ICs. As discussed in Chapter 16, a silicon wafer is used as the substrate base, Al or Cu as the conductor, and silicon dioxide as the inorganic dielectric media. Several microns of the metal conductor and the subsequent silicon dioxide dielectric layers are deposited by a vacuum deposition technique (such as evaporation or sputtering). Layer thicknesses are controlled quite uniformly over areas as large as 6" - 8" diameters. Photoresist is applied and patterned with the support of a wafer spinner and mask aligner, respectively. The metal is etched away by either wet etching or, more typically, by dry etching techniques. Because the silicon wafer substrates are extremely smooth and flat, very fine feature sizes are possible. Although submicron interconnects are possible, typical features of 15 μm are adequate for MCM interconnects.

MCM-Si offers the advantages of the highest signal interconnect density, excellent CTE match to the silicon die and the utilization of existing semiconductor fabrication infrastructure. The equipment used is readily available and the processes have been established and well characterized by the semiconductor manufacturing community. The utilization of this infrastructure

has contributed to a reduction in fabrication cycle time (and learning curve) for many entering the MCM field along with the security of the predictable reliability of conventional ICs. Additionally, the inherent low density of silicon makes it ideal for applications in which light weight is critical, such as in the aerospace and military industries.

However, MCM-Si technology also has some significant disadvantages. Foremost among these are that silicon substrates are not a suitable MCM package base. In some cases, the high resistivity of the aluminum conductor precludes its use in high frequency applications. In addition, as with MCM-D, the equipment costs are high. Batch sputtering systems can range from $150,000 to $350,000 and in-line systems from $1,500,000. In combination with low volume manufacturing, typical module costs will be high. Silicon-based technologies are discussed further in Chapter 16.

Other Inorganic MCM Materials

The majority of the industry has focused on the development of organic dielectric materials (MCM-D and MCM-D/C). For the short term these will be the materials of choice. However, in the long term, some inorganics may offer performance benefits that surpass that of today's organics. Research workers have focused attention on synthetic diamond and diamond-like coatings [11]. Although the development of cost effective deposition methods requires additional work, the superior properties of the diamond-like films warrant investigation as dielectric layers for high density interconnect structures. These materials typically combine desirable properties such as a low dielectric constant, extremely high thermal conductivity (more than four times that of copper) and a low CTE. These properties are desired for high frequency, high power and low residual stress applications, respectively.

2.3.6 Thick Film Hybrid MCM

Ceramics have been used in the microelectronics field for many decades. Various ceramic materials exist, but alumina (aluminum oxide) is most widely used as a substrate for the hybrid microelectronics industry. Some argue that the development of thick film hybrids was the origin of the first MCM-type interconnect. In this type of interconnect system, a flat sheet of alumina is typically used as the substrate material. Each layer is applied sequentially by screen printing, as described in Chapter 6. Although this is not a complicated process, one disadvantage with any sequentially fabricated module is layer-to-layer inspection. Since these layers can only be inspected once they have been applied to the module, there exists a potential for a defect in the final layer causing the entire module to be defective. This is unlike parallel processing (for

MCM-L, MCM-C) where all the layers can be fabricated independently and inspected. Many new processes under development either use parallel processing guidelines or minimize the total number of layers.

The substrate is then placed into a furnace where the ink is dried and fired. Conductor geometries are typically limited by the fabrication of the screens used for the printing process to 0.005" lines and spaces.

The dielectric layer is applied in a similar fashion. No dielectric material is applied in regions where vias lead to the above layers. When the subsequent conductor layer is printed, the ink flows into the openings of the dielectric and make contact to the conductor below. The balance of the module is completed by repeating this process.

Thick film hybrid is a mature technology with good infrastructure. A major advantage of this technology is that a large supply of resistive inks are available that can be screened onto the module to integrate resistors. Additionally, there exists an abundant supply of surface termination inks with metallurgies that facilitate wire bonding, soldering or component attachment through conductive epoxies.

Thick film hybrid technology used for MCMs has some serious disadvantages in the areas of performance and routing density. The dielectric constant of most dielectric inks is as high as 8. While high dielectric constant is not in itself a disadvantage, it can make a desired substrate characteristic impedance difficult or impossible to attain. Thick film hybrids are very limited in routing density - typically 0.005" - 0.010" lines and spaces and via sizes of approximately 0.008". From a module yield point of view, it is advantageous to minimize the number of layers. One way would be to increase the routing density so that all signal interconnects could be made on a minimum number of layers. Recent research and development efforts in transfer printing have claimed results of 0.001" feature sizes. Although this process has yet to be implemented in a production environment, it holds promise for the future.

2.4 CHIP MOUNTING CHOICES

The purpose of any chip mounting technique is to provide a suitable path for electrical signals from chip to MCM substrate and to provide a means of mechanically attaching the chips to the substrate. All chip mounting techniques also provide a path for heat generated in the chip to dissipate. The common of chip mounting choices are wire bond/die attach, TAB, flip TAB, and flip chip. Further details of these chip mounting or chip connecting techniques are presented in Chapter 9.

The method of connecting chips to a substrate is probably the most critical choice in module physical design. This choice largely defines the technical

Table 2-3 Chip Mounting Choices.

	Die Attach Wire Bond	TAB	Flip TAB	Flip Chip
Cost	X	> 2X	> 2X	0.8X
Chip Availability	Excellent	Fair	Fair	Poor
Reworkability	Poor	Fair/Poor	Fair	Good
Probe Test	DC	AC	AC	AC
Lead Inductance (nH)	2.0 - 3.5	4.0 - 5.0	4.0 - 5.0	< 1.0
Footprint (Chip +)	20 - 100 mil	80 - 600 mil	80 - 600 mil	Clearance
Peripheral Bond Pitch	4 - 7 mil	3 - 4 mil	3 - 4 mil	10 mil
Area Array Bond Pitch	N/A	N/A	N/A	≥ 10 mil
Max I/O Count	300 - 500	500 - 700	500 - 700	> 1,000

Notes:

- Cost based on high volume production of a nine chip module with over 2000 chip-to-substrate connections
- Wire bond lead inductance for 1.0 mil Al wire with pad-to-pad spacing from 2.0 - 4.0 mm.
- Wire bond footprint depends on cavity or no cavity.
- TAB footprint depends on OLB pitch.
- Chip availability may be poor for high performance devices such as DSP, microprocessor and ASIC.

capabilities and product characteristics of the module. The chip mounting technique dictates what thermal path must be provided for the heat generated in the chip and, in many cases, dictates the type of substrate to be used. The chip mounting or chip connection choice also has heavy implications on module cost, chip availability, chip testability, module reworkability, module size and module performance. These issues, compared in Table 2-3, will be discussed for each of the major chip mounting choices.

2.4.1 Die Attach/Wire Bond

Die attach/wire bond chip mounting of semiconductor chips has been used for over 20 years. The chip is attached mechanically to the substrate by a variety of means including organic adhesives (silver filled epoxy is common) and metal eutectics (gold/silicon and various solders are common). The die attach material can be thermally and/or electrically conductive depending on the material selected. Then the chip is connected electrically, wire bonded, to the substrate by gold or aluminum wires. Figure 2-7a shows chips wire bonded in an MCM. Over years of process development, this technique has been thoroughly characterized and refined to its present production limit of about 4.8 mil pitch (a "mil" being a milli-inch and "pitch" referring to the center-to-center spacing of the wires). Figure 2-7b shows a portion of a chip wire bonded with 464 wires on a 4.8 mil pitch using 1.25 mil aluminum wire - a good example of state of the art production.

The die attach/wire bond technique minimizes MCM risk. High volume precision equipment is readily available in existing semiconductor assembly lines and experienced personnel are available. Yields (number of good wire bonds per number of wire bonds attempted), and thus costs, are predictable. All of this adds up to known variables and low risk.

Another unique advantage of die attach/wire bond is availability of ready to use chips. Bare silicon chips with wire bondable aluminum bond pads have been sold for years by semiconductor manufacturers to hybrid manufacturers. Techniques, specifications and applications information for electrical test, visual inspection, packing, shipping and assembling exist in a somewhat established infrastructure. It is important to note, however, that while many thousands of devices are routinely available in chip form, many state of the art devices such as microprocessors, digital signal processors and application specific integrated circuits (ASICs) are not. These devices are fully tested and sold typically in single chip package form - an important issue for MCM manufacturers.

In addition to pitch limitation, the die attach/wire bond technique has two major disadvantages for MCMs. The first is that die attaching a chip to a substrate complicates thermal management within the module. As shown in Figure 2-7a, heat generated by the chip must be conducted through the die attach material to the MCM substrate, to the package body and, finally, to the outside of the package. But most MCM substrates and package bodies are poor conductors of heat. They also may have CTE (the material property defining the of expansion or contraction at different temperatures, usually expressed in ppm/°C) sufficiently different from that of the silicon chip to create mechanical stress problems.

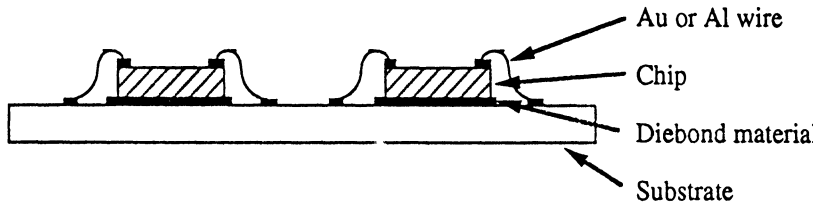

Figure 2-7a Die attach/wire bond.

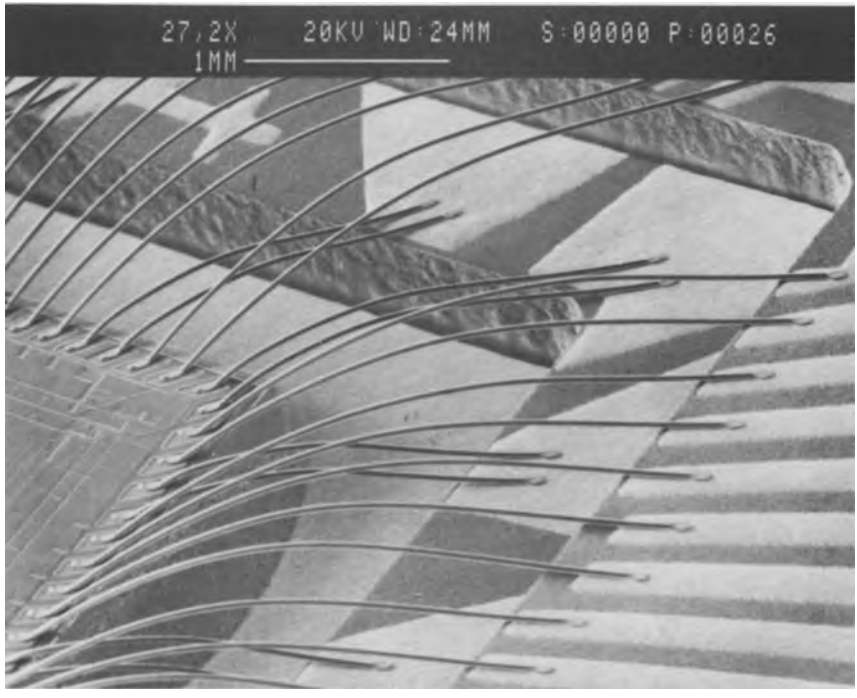

Figure 2-7b State of the art wire bonding (1.25 mil Al wire, 465 I/O, 4.8 mil pitch).

The second major disadvantage of using the die attach/wire bond technique for MCMs is that bare silicon chips cannot today be tested at-speed (normal operating AC frequency) because the large inductance of probe needles masks the test results. At-speed testing is normally done by the semiconductor manufacturer after chips are packaged. From a MCM manufacturing perspective, the scenario is grim: partially tested chips are assembled together in a module and then the entire module is tested at operating frequency. Any one chip that is not "up to speed" causes the entire module to fail test. Module yield is affected dramatically by the number of chips in the module. Even if the module design and test techniques are clever enough to locate a bad chip, the problem is compounded by the fact that die attach/wire bonded chips are difficult to remove and replace. Thus, the MCM manufacturer is faced with poor yields and little chance of rework. In addition, technology is not commonly available today to burn-in bare silicon chips; burn-in must be done at the module level (see Chapter 13).

The die attach/wire bond technique is often cited for its low cost - about $0.25 for die attach and approximately $0.01 per wire bond. But as we have seen, the total module manufacturing costs could be quite high due to low yields. This technique is suited best for modules consisting of a few, low power, inexpensive chips and an inexpensive substrate. Wire bond techniques are discussed in Section 9.3.

2.4.2 TAB

Tape automated bonding (TAB) is a method of electrically and mechanically connecting a chip to the substrate that has many possible advantages over conventional die attach/wire bond techniques for MCMs. The tape is an etched-out piece of metal consisting of tiny beam leads. The end of the leads connecting to the chip are typically on a small pitch and are fanned out to a larger pitch at the end that connects to the substrate. Chips are first bonded to the tape (inner lead bond or ILB) with each chip pad connected up to a beam lead by thermocompression (heat and pressure) bonding. The ILB unit is then excised from the tape and die attached to the substrate using conventional means described in Chapter 9. As a last step, the other end of the beam leads are bonded, using heat and pressure, to the substrate (outer lead bond or OLB). There are many techniques and metallization schemes for accomplishing inner and outer lead bonding. From a manufacturing point of view, the two main types are gang bonding and single point bonding. In gang bonding, all leads are connected at the same time by means of a hot bar thermode. The process is fast and uniform, but lead planarity is a difficult issue. In single point bonding, each

lead is connected individually by means of a hot point or laser bonder. Figure 2-8a shows a schematic diagram of chips TAB bonded in a MCM.

TAB has been developed in the United States primarily to handle more chip connections at tighter pitches than wire bonding. TAB works well for high lead count, small pitch chips where wire bond yields become unpredictable and costly. Production TAB ILB bonding is done today at 4 mil pitch and has been demonstrated in the laboratory at 3 mil pitch and less. Figure 2-8b is a photograph of a 385 mil square chip with 360 pads TAB inner lead bonded at a 4 mil pitch. The beam leads are fanned out for outer lead bonding at a pitch of 8 mil. The large fanout is required for two reasons. First, tight pitch bonding requires leads to be very precisely coplanar and this is less likely to be the case by the time the unit reaches the OLB process step. And second, the substrate or board technology limits the pitch capability of pads on the substrate. If an advanced substrate is used, then non-fanout TAB (where the OLB pitch is the same as the ILB pitch) can be used.

TAB offers several advantages when used to bond chips to substrates in MCMs. Foremost is that ILB units can be tested at ac operating speeds. This means that bad chips can be culled and only known good chips need be assembled into the module, thus dramatically increasing module yields. The value in testing chips before module assembly increases with the number of chips in the module. In addition, the type of chip in a module can increase or decrease the need to test them prior to assembly. For example, ASIC chips typically are not speed sorted at final test; they are designed to fall within a range of specified performance. A module containing all ASIC devices can be expected to perform properly even without at-speed testing of the chips prior to assembly. On the other hand, high speed memory components are speed sorted at final test and graded for sale. A module containing these devices could not be expected to yield well at final test unless the chips had been at-speed tested prior to assembly.

A related advantage of TAB is that inner lead bonded chips can actually be burned-in (operated at-speed and sometimes at elevated temperatures for a period of time to cull out bad units) prior to module assembly. Such practice would probably eliminate the need for burn-in at the module level, reducing the cost of scrapping or reworking finished modules.

Although TAB offers the advantages of assembling only known good chips and the capability of bonding large complex chips, the disadvantages of using TAB in MCMs are numerous. Foremost among these is cost. Two factors can make TAB expensive: cost of the TAB tape and the number of difficult manufacturing process steps. Complex double metal layer (one metal layer acts as the ground plane to reduce lead inductance) tape can run as high as $30 in a 35 mm format. Single metal layer tape is significantly cheaper - approximately

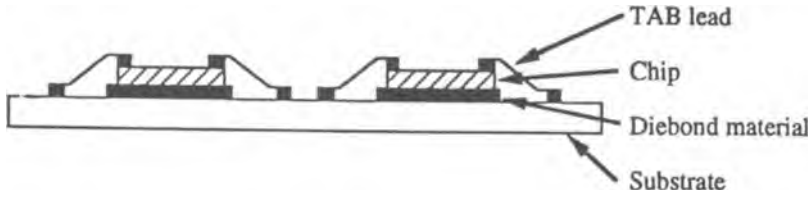

Figure 2-8a TAB.

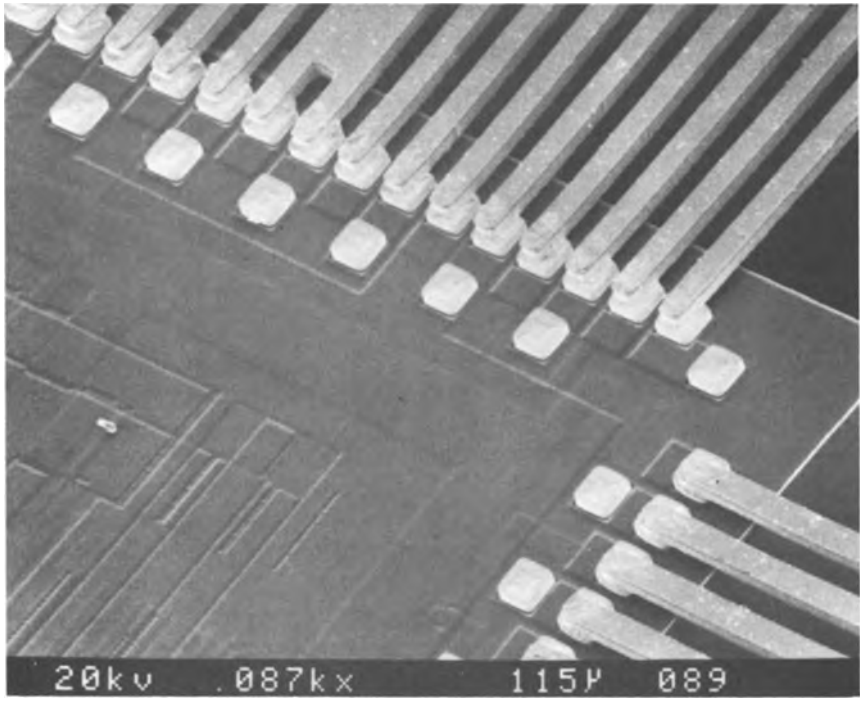

Figure 2-8b State of the art TAB (360 I/O, 4 mil pitch).

$4 in a 35 mm format. Once the chip is inner lead bonded, it cannot be reworked or the tape salvaged. A typical TAB manufacturing flow consists of multiple difficult processes: inner lead bonding, testing, burn-in, testing, die attaching and outer lead bonding. Each of these processes can be low yielding on complex components, and together, they can add up to unacceptably low yields and high cost.

Another disadvantage of TAB is that die attaching a chip to a substrate complicates thermal management within the module. The problem here is identical to that discussed in Section 2.4.1.

Finally, TAB technology often means long leads and large component footprints. Even moderate OLB pitch can easily mean long beam leads, with corresponding high inductance. A very long beam lead may require an integrated ground plane to reduce lead inductance. At this level, TAB tape becomes very difficult and expensive to manufacture. Another disadvantage of TAB is that OLB at reasonable pitches can mean very large device footprints. In one case, a 15 mil OLB drove TAB lead length to over 880 mils. Large footprints mean the electrical signal must travel greater distances, something MCMs are designed to avoid.

In general, TAB technology is best suited for large MCMs containing complex and expensive chips and substrates. For this type of application, the advantages of testability and burn-in at the ILB stage probably outweigh the disadvantages.

2.4.3 Flip TAB

Flip TAB, sketched in Figure 2-9a, is a variation on TAB where ILB bonded units are mounted face down on the substrate for OLB. Flip TAB has all the characteristics, positive and negative, of regular TAB, with two major differences. First, in flip TAB, heat generated by the chips can be removed from the backside of the chip to a module lid, thus simplifying substrate design. And second, flip TAB is easier to repair than regular TAB since no die attaching is done. Instead the inner lead bonded chip simply rests on a spacer material and is held in place by the OLBs as shown in Figure 2-9b. The mainframe computer module shown in Figure 2-13 is another good example of non-fanout flip TAB.

2.4.4 Flip Chip

Flip chip mounting offers the best possible electrical connection between chip and substrate because it eliminates leads altogether. As sketched in Figure 2-10, solder bumps are placed in an array pattern across the chip. The chips are

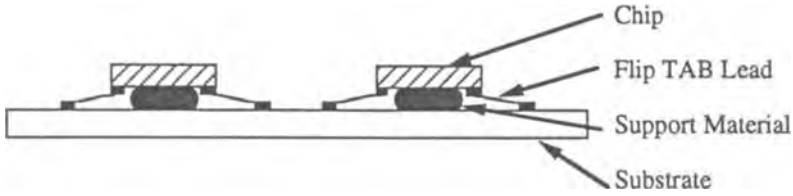

Figure 2-9a Flip TAB chip mounting.

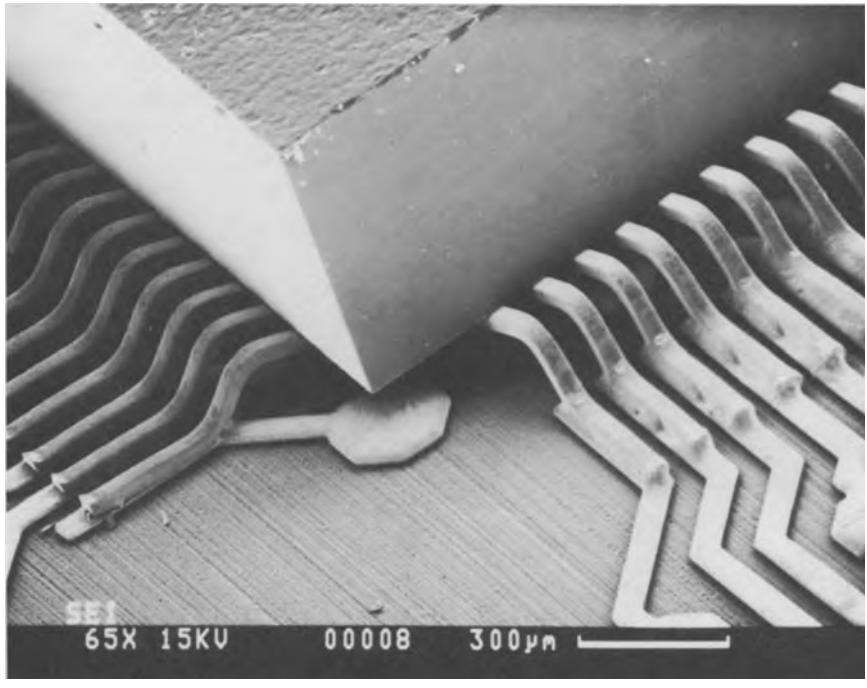

Figure 2-9b State-of-the-art flip TAB.

mounted face down on the substrate and the solder is reflowed (heated to the melting point and then cooled) to form the connection. The chips can be placed as close together as 10 mils with no additional space needed for connections. The technique offers the best performance and smallest footprint at potentially the lowest manufacturing cost.

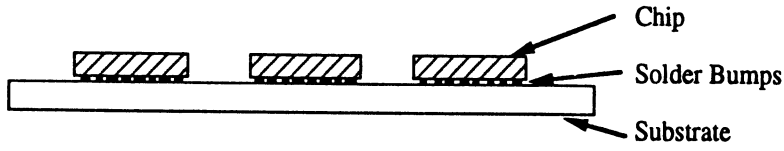

Figure 2-10 Flip chip mounting.

Flip chip electrical performance is superior to the other techniques because the interconnect length is extremely short - usually only about 50 - 100 μm, thus, the inductance is extremely low, as shown in Table 2-3. This can be a significant factor if designing a module for high speed applications.

Small chip footprint is also a performance plus for the flip chip technique. Small footprints mean shorter distances between chips on the module and shorter signal propagation delay. (Propagation delay is the time it takes a signal to leave the output buffer of one chip, travel across the substrate and enter the input buffer of another chip). Product miniaturization is one of the market drivers for MCMs. Obviously, small footprints also mean smaller modules.

From a manufacturing point of view, flip chip has several advantages. There are few process steps and those steps are batch rather than individual. Additionally, because the solder bumps can be placed in an array pattern across the entire surface of the chip, the pitch of these bumps need not be extremely small. As the number of signal connections increases on complex chips, wire bond and TAB techniques must continually strive for smaller and smaller pitches. Once developed, the flip chip technique should be the highest yielding and lowest cost of all.

Finally, flip chip, like TAB, offers the ability to probe test chips at-speed prior to mounting in the module. This means that bad chips can be culled and only known good chips need be assembled into the module, dramatically increasing module yields. The value in testing chips before module assembly increases with the number of chips in the module. In addition, the type of chip in a module can increase or decrease the need to test prior to assembly.

Also, like TAB, a flip chip mounted IC can be removed from the module and replaced should a defect be identified. This repair process is accomplished by locally heating the faulty die to reflow the solder and remove the die. The site is then refreshed by either reflowing or removing the existing solder.

Flip chip has been developed and utilized almost exclusively by IBM for over 10 years. The basic technology is well characterized and production

qualified within IBM, and almost universally not characterized or qualified outside of IBM. This fact gives rise to a host of infrastructure issues for the non-IBM module designer selecting flip chip technology. First and foremost is the lack of chips available with solder bump array connections. Basically, they do not exist outside IBM. The outside module designer is faced with procuring standard wire bond compatible chips or wafers and somehow converting them to flip chip compatibility. The problem is compounded by the fact that these chips will have peripheral connection locations, possibly at a very tight pitch. Conversion to a large pitch array pattern of connections, and then bumping them, is a formidable task. Simply asking semiconductor manufacturers to provide flip chip compatible chips may not work. Infrastructure is lacking at this level also. Semiconductor manufacturers do not have computer aided design (CAD) tools or rules for designing flip chips. They lack bumping processes and equipment, probe-test equipment, trained personnel, etc.

The disadvantages of flip chip clearly are related to infrastructure and economics rather than technical. Current efforts at IBM to disseminate the technology to the general industry may eventually alleviate these issues and flip chip could become the preferred interconnect for a wide range of MCMs. For today, the MCM designer must carefully weigh the risks and benefits of using flip chip for a specific application.

2.5 MODULE LEVEL CONNECTION CHOICES

Numerous choices exist for the connection of the MCM to the mother board, but, unlike the vast standards implemented for single chip packages, none presently exist for MCMs. Without industry collaboration, the recent broad activity in MCMs will result in many different package sizes and formats. Fortunately, a cooperative venture has been initiated for the standardization of MCM packaging sizes. A task force operating under the auspices of the IEEE Computer Packaging Committee recently proposed a series of standard MCM package sizes to the EIC/JEDEC Committee [12]. Until this is reconciled, many module sizes will continue to be fabricated. Some of them will adopt the existing single chip packaging formats and benefit from the existing standards implemented by such organizations as JEDEC. The following section provides the basis to better understand the different options that exist and the performance penalties imposed.

2.5.1 Peripheral I/O

Peripheral I/Os are the most commonly used single chip package connection arrangement. The appearance of many MCM designs have been styled to

resemble these single chip packages. By doing so the assembly and testing infrastructure can be utilized with little or no tooling modifications. The user does not know whether the package contains multiple chips or a single IC without dissecting the package. These packages can be implemented with virtually all of the MCM substrate types stated in Section 2.3, but are most prevalent in MCM-L where leadframes can be easily laminated to the module or plated through-holes can be used as castillation joints to form leaded and leadless modules, respectively. If leaded, the leads can protrude from one or all four sides. For most applications, the most efficient way to distribute the I/O warrants the use of all four sides. The leads are trimmed and formed to QFP specifications. If no leads are required, metallization is placed on the underside of the module body to facilitate direct soldering. Although this style of package utilizes less space because the solder joints are on the underside of the package perimeter, inspection of the solder joints by conventional means is difficult. Conversely, the lead adds inductance and contributes to the propagation delay of the package. For high frequency applications, leadless modules are preferred.

In both cases, as the number of I/Os terminating from the module increases, either the lead pitch decreases or the module size increases. As the lead pitch decreases, the ability to reliably solder the module to a circuit board becomes progressively more difficult. As this pitch is reduced, soldering defects, such as bridging (solder flows between adjacent I/O and forms an electrical short), also increases. In contrast, if the package body is increased, more space of the mother board will be required for the attachment process. Thus, the use of perimeter I/Os is self limiting. Typical I/O pitches found are 0.050", 0.025" and 0.020", and I/O counts can reach several hundred. For increased interconnection density, one must consider the use of array I/O connections.

2.5.2 Pin Grid Array

Pin grid arrays (PGAs) can be utilized as a solution to overcome the geometrical constraints imposed by the peripherally terminated modules. By distributing the leads on the full area of the underside of the package, the module is more efficiently used. Figure 2-11 demonstrates the module I/O plot versus the area of the package. For the same pitch, significantly more I/Os exist in the PGA format. One hundred mil, 70 mil staggered and 50 mil pitches are commonly used. Package lead counts from several hundred to over 1000 have been fabricated. These pins can be press fit and soldered onto the MCM, as with plastic packages, or brazed in place, as with ceramic. The approximate cost of adding pins ranges from $0.01 to $0.02 per I/O. The PGAs can be through-hole mounted, placed into sockets or the pins may be surface mounted and soldered directly to the board. In many high performance applications, surface mounting

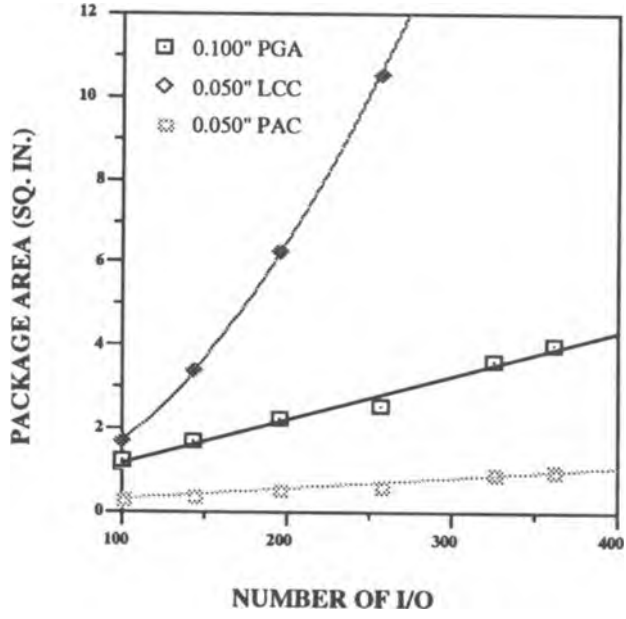

Figure 2-11 Array package efficiency.

will be required. In these cases, as with any leaded module, the inductance of the lead must be taken into consideration. For applications where this inductance is too great, area array formats such as pad array carriers should be considered.

2.5.3 Pad Array Carrier (PAC)

Pad array carriers (PACs) are often referred to as area array packages, land grid arrays (LGAs) or surface mount arrays (SMA). They are similar to PGAs with the exception that the pins are replaced by metallized pads. This package offers all of the efficient I/O termination benefits of the PGA without the negative attributes associated with lead inductance. Additionally, costs are typically less than PGAs since no leads are required. Attachment to the motherboard is through a socket or by a direct soldering process known as C5 (Controlled Collapse Chip Carrier Connection). In this process, solder bumps are deposited onto the metallized pads on the underside of the module and on the mating pads

on the motherboard. The PAC then is placed onto the board and reflowed. As with most surface mount applications, small misalignments in component placements are remedied during the reflow cycle by the natural wetting characteristics and surface tension of the solder. This phenomena contributes to a high yielding process.

2.6 GLOBAL MATERIALS AND MANUFACTURING CONSIDERATIONS

2.6.1 Cost

The choice of materials and manufacturing processes greatly influences the final module cost and its suitability for a particular application. Because many MCM technologies are new (such as thin film substrates, flip chip connections and TAB), capital equipment start-up costs can be very high. The immaturity of these technologies also means low initial yields. Although capital costs and initial low yields can easily undermine a start up MCM development effort, this chapter is concerned with cost comparisons based on a full-scale production situation.

The largest contributions to cost for MCM production are module final test yield, substrate cost, and chip cost. Module final test yield is based on the expected yield of the individual components (chips plus substrate) plus an estimate of the damage done by the assembly process. Expected yield of the chip components is a tricky subject, depending heavily on the type of testing done at probe (in wafer form) and at final test for a particular device. For example, a RAM (random access memory) chip is normally tested only for basic functionality at probe. Then the RAM is packaged and sorted at final test for speed and temperature performance. As a last step, the packaged RAM is burned in to cull early life failures. Unless the die is speed and temperature sorted at probe and burned in at wafer level, which is not the normal practice today, the speed, temperature, and burn-in fallout occur at module final test and module burn-in.

If the circuit does not contain redundancy, the module can be considered a "series system" [13]. The expected yield of a series system is the product of the individual expected yields of the components. For example, consider a module containing three different semiconductor chips with expected yields of 95%, 90%, and 97%. The substrate expected yield is 95% and the assembly related yield is estimated at 99%. The expected module final test yield is then:

$$.95 \times .90 \times .97 \times .95 \times .99 = 78\%.$$

It is easy to see that the module yield quickly deteriorates as a function of the number of components and the expected yield of each of those components. Yield can be greatly improved and module costs dramatically reduced by testing module components - chips and substrate - prior to assembly.

For a given chip set, module yield will dominate total costs for small plastic MCM-L type modules where substrate costs are low and module repair may be difficult or impossible. If a repairable technology is used along with an inexpensive substrate, the silicon cost is the major contributor to total cost. At the other end of the spectrum, substrate cost may be the largest contributor to total cost for large, high end, high power ceramic or MCM-D/C modules where module repair is practiced [14].

Substrate cost is driven by three major factors: capital equipment required to fabricate the substrate, the number of module substrates that can be obtained from a single process unit (such as a ceramic wafer) and substrate yield. More mature technologies such as thick film hybrid and wire bond will have the lowest capital equipment costs and the highest substrate yield. Larger process units (such as 12" × 18" PWB panels) will lead to lowest individual substrate costs. Substrate yield is substantially influenced by basic manufacturing approaches, such as parallel versus sequential processing. In parallel processing (most commonly used for PWB and cofired ceramic type substrates), substrate layers are individually fabricated, inspected and yielded. The layers are then stacked to form a single substrate.

2.6.2 Electrical Performance[1]

Electrical performance can be affected significantly by choices made in the areas of signal interconnect and chip, MCM substrate and module level connections. Thermal performance of a package can also affect electrical performance, most likely through degraded performance at excessive junction temperatures. Other than thermal issues, the chief performance factors to be considered during package selection are:

1. Material properties of insulator layers and interconnect conductors
2. Transmission line parameters such as impedance and crosstalk
3. Package parasitics (such as pad capacitance and lead inductance)

Ideally, in any electronic system, the signal leaving the output of some transmitter should arrive, with no changes, at the input of some receiver. However, signals experience attenuation (loss of amplitude) and distortion (noise)

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[1] Contributed by Eugene Heimbecher.

as they travel through a packaging system. Loss is caused by material properties and noise is caused by numerous factors broadly broken into transmission line concerns and package parasitics. Noise control considerations generally lead to package designs which are large, difficult to manufacture, and expensive. Manufacturing and cost factors, as well as size and weight considerations, usually lead to package designs with poor electrical performance. Balancing these factors against one another is essential for successful MCM system design.

Insulator and Conductor Material Properties

Insulator layers effect electrical performance through two parameters. These are dielectric constant (ε_r or K) and loss tangent (tan δ), also known as dissipation factor (DF). Dielectric constant, ε_r, is a key factor in determining most transmission line parameters; both ε_r and tan δ contribute to what is called dielectric loss in insulator layers. Dielectric loss, like conductor loss (below), results in signal attenuation. Generally, for MCMs with short line length and frequency content below 1 GHz, dielectric loss is not of concern. For these cases, loss due to resistivity of interconnect metal almost always masks dielectric loss. At frequencies much higher than 1 GHz, certain materials must be avoided because of their high dielectric loss. At microwave frequencies, preferred materials are ceramic or teflon; fiberglass epoxy (FR-4) is to be avoided.

The high dielectric constant of a material in and of itself is not necessarily a problem. It is not an automatic limitation to high frequency usage. There are usually undesirable consequences to using high dielectric constant materials for signal interconnect structures. These are primarily: increased signal propagation delay and increased physical size (for identical transmission line parameters and performance).

Interconnect material (such as copper) affects electrical performance primarily through internal resistance resulting in signal losses. (Voltage drop due to these losses is usually negligible in signal interconnect, but may be significant in power and ground lines. This is one reason for use of wide planes to distribute power and ground). Resistance is generally broken down into two categories. These are standard DC resistance and high frequency AC resistance due to skin effect. Skin effect occurs because alternating currents do not flow evenly throughout the cross section of a conductor, but tend to flow only near the outer surfaces. For example, it is a good approximation to say that, for pure copper, a current with a frequency of 300 MHz only flows in the outer 0.15 mil of the conductor cross section [15].

DC resistance is calculated using standard equations; AC resistance is calculated by a ratio of full cross section to skin effect area [16]. Line resistance is not always important. For example, MCM-L conductors are on the order of 3 - 4 mils wide and about 1 mil thick and both DC and AC losses are usually

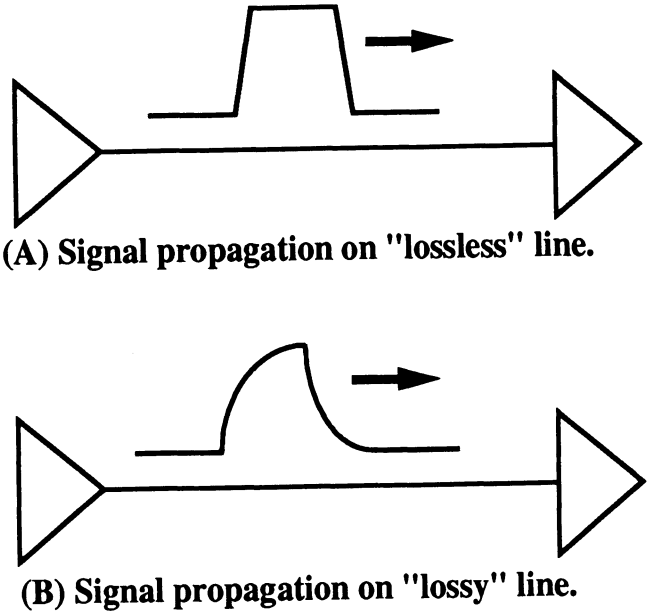

Figure 2-12 Effect of line loss.

negligible. On the other hand, MCM-D conductors may be on the order of 0.4 × 0.15 mil and losses need to be carefully assessed. Measured data (Motorola) of some typical MCM-D substrates show DC resistance on the order of 3 - 5 Ω/cm for copper interconnect and 15 Ω/cm for aluminum.

Large line resistance causes a low pass filter (RC) type roll off on signal edges (Figure 2-12). This roll off is small near the sending end of the line and becomes progressively more pronounced as the signal propagates down the line. The edge degradation is beneficial to noise generation, but can be a significant problem on long lines with critical timing requirements, for example clock distribution lines. Also, the signal rise and fall times may be slowed down so much that CMOS devices become subject to spurious oscillations. The MCM system designer must consider these issues carefully.

Transmission Line Parameters

The understanding of transmission line theory and its application to MCM design is a text in itself [16]. However, it may be sufficient to say that at higher

frequencies and faster edge speeds it always is necessary to maintain the best possible controlled impedance environment for both signal lines and power and ground distribution. For optimum performance in high speed, high frequency systems, signal interconnect always needs to be done in a transmission line manner (such as stripline, with good AC ground and reference planes both above and below the signal). Additionally, voltage distribution should always use full planes well coupled to ground references. A near ideal approach is available in the MCM-D/C. Signal lines can be embedded in low dielectric constant deposited stripline layers with optimized signal performance while power and ground return planes can be contained in a high ε_r, very thin (and hence highly capacitive) layer in the ceramic base. With sufficient power plane capacitance, it would not be necessary to use discrete decoupling capacitors.

Dielectric constant is important in two ways. It affects both transmission line impedance and speed of signal propagation. As an example, for a given stripline geometry, if the impedance is 50 Ω and the delay is 2.03 ns/foot (ε_r = 4.0), doubling the dielectric constant without changing any other factor results in impedance decreasing to 35 Ω) while delay increases to 2.87 ns/foot. (Note the square root of two relationship.) The situation is not as clean for microstrip lines or other multimedia line geometries, but the general trend of decreased impedance and increased delay (as ε_r increases) always holds.

For several reasons it is desirable to have transmission line characteristic impedance (Z_o) fall into the general range of 50 - 150 Ω. Line impedance is generally a complex function of several parameters, but it can be increased (from 35 - 50 Ω) by a combination of making line width smaller and/or making the vertical distance between the signal lines and ground planes larger. When dielectric constants are large, as for ceramic, designs must use either thinner line widths or thicker insulator layers than for designs with smaller dielectric constants, such as polyimide. There are two problems with trying to use thinner lines. First is the fact of running into the manufacturing process limit, as discussed in previous sections. Second is a parameter tolerance issue: a line width of 10 mils ±1 is easier to make consistently than a line width of 2 mils ±1. Thus, the usual strategy is to increase the thickness of the insulator.

The chief physical parameters for controlling impedance are: dielectric constant and line width and vertical distance between signal line and ground plane. It is recommended that a full dimensional analysis of all parameters of all layers in a substrate stack up be performed to identify the worst case maximum and minimum impedances to guarantee acceptable electrical performance. Also, it is often desirable to separate or isolate certain signals from other signals. This can result in the need for additional routing layers as compared with a design with no routing restrictions. These extra layers are undesirable from a manufacturing and cost point of view, but are necessary to obtain required electrical performance.

Crosstalk is the remaining transmission line parameter to be discussed. Crosstalk is the unwanted coupling of energy from an active (signals occurring) section of some circuit or system to some other unconnected and nominally quiet (no signals) section. This can result in a receiver seeing an input signal that is, in fact, only noise. Crosstalk can arise form a number of sources:

- Electro-magnetic interference (EMI)
- Power and ground plane noise
- Capacitive affects when signal lines cross over each other
- Mutual coupling when signal lines run parallel to each other

Generally, this last mechanism is considered the most significant source of crosstalk in well designed systems. (But crossover affects can be significant if several or more occur along the length of the victim line.)

For stripline, maximum crosstalk is not affected by the dielectric constant of the insulator material. If ε_r is doubled, all other factors being unchanged, there will be no change in crosstalk. However, if the dielectric thickness is increased (to increase line impedance from 35 - 50 Ω), then crosstalk will increase due to the reason discussed below. Therefore, with higher ε_r materials, to obtain comparable electrical performance, the line separations must be larger and the overall physical size of the design will probably increase.

There are a number of strategies for reducing crosstalk, but the most useful is simply to keep things far apart. Microstrip transmission lines are more prone to crosstalk problems and should be avoided in noise sensitive designs. When microstrip is used, separating two lines by a distance equal to 8H (where H is the vertical distance between the bottom of the signal lines and the top of the ground plane) reduces crosstalk to about zero. Stripline is a more effective approach for lines in a noise sensitive application.

As an example, consider an MCM-D/C design, as mentioned above. If the distance between ground planes is about 40 μm (1.6 mils), striplines separated by only 80 μm would have no crosstalk. In practice, it is found that even a separation of 40 μm is enough to achieve close to zero crosstalk. On the other hand, for an MCM-L design using microstrip, the situation can be much worse. For example, to guarantee no crosstalk in a structure with a dielectric thickness of 4 mils, signal lines would have to be separated by over 30 mils. Thus, there is a 10 to 1 routing density advantage in MCM-D (stripline) as opposed to current MCM-L (microstrip) for identical levels of crosstalk.

Crosstalk does not occur only in MCM substrates. A potential problem in flip chip MCM design is redistribution of I/O pads. Most ICs are not designed for flip chip. Hence, the typical procedure is to take a standard chip, with I/O

pads on the periphery, and use an extra metal layer to redistribute the I/O pads over the surface of the chip. This must be done with some care. It is possible to route a very noisy output over the top of some very sensitive input. This is an issue that is not well understood currently.

Crosstalk is an issue to be considered in package selection as well. Three primary factors to reduce chip connection and packaging crosstalk are: to keep leads as far apart as possible, to keep parallel leads as short as possible and to use as many ground leads as possible (mixed in with signal leads) to reduce coupling between signal leads.

2.6.3 Thermal Path

Heat produced within semiconductor chips will dissipate through the MCM package and out to ambient air and to the board on which the module is mounted. If heat is not dissipated efficiently, the chip junction temperature (T_j) rises beyond the reliable operating range and operating life is decreased significantly.

Like single chip electronic packages, module thermal performance is measured in terms of the difference in temperature between the chip junction and ambient air per watt of power produced by the chips:

$$\theta_{ja} = (T_j - T_a) / W.$$

The module must provide thermal pathways that conducts heat expected from the chips mounted in the module. Heat is conducted through a combination of four general paths: chip to substrate to ambient, chip to lid to ambient, chip to leadframe to ambient or chip to substrate to heatsink to ambient. The chip to substrate to ambient path is most common in electronic packaging, but for MCMs this path can be complicated by a substrate with mediocre thermal conductivity and very dense circuitry. Designing structures to improve substrate conductivity, such as thermal vias and metal heat spreaders, usually reduces the routing channels available in the substrate. The designer is faced with a difficult tradeoff between routing density and thermal conductivity. The chip to lid to ambient path has been demonstrated on several high power MCM designs, but is workable only when the backside of the chip faces the module lid - flip chip or flip TAB mounting. Many low cost, single chip packages use the chip to leadframe to ambient approach. This path has limited thermal capability (35°C/W in still air) and may complicate the routing of signal interconnect on the module.

2.6.4 Rework

The choice of materials and manufacturing processes determines whether a module can or should be reworked; that is, a faulty chip removed from the substrate and replaced with a new chip. Rework is both a technical and business issue. The cost of the rework process must be less than the cost of a finished module, otherwise rework does not make economic sense. When considering the cost of rework, one must consider costs associated with designing fault location circuitry, isolating a fault, performing the repair, retesting the part and, perhaps, cycling through another rework iteration.

Module level rework begins with fault detection by either visual or electrical tests. Next, the faulty chip is accessed. The chip is demounted, normally by applying heat to the chip connection points. The substrate connection points are then prepared for a new chip, the new chip is mounted, the module encasement is restored and the module is retested. Materials and manufacturing choices are obviously critical at every step of rework. For example, visual detection may be difficult or impossible with flip chip or flip TAB type chip mounting. Electrical detection is successful only if the module circuitry is designed for such testing, using JTAG boundary scan, for example, as discussed in Chapter 13. Chip accessibility can be difficult or impossible in modules with plastic mold encasement or with certain lid attach schemes. Chip demounting is difficult or impossible in modules where a die attach is employed. Substrate connection point preparation is difficult in modules that contain tight pitch chip connection pads, or in those that rely on solder pads on the substrate.

2.7 MODULE DESIGN EXAMPLES

MCM materials and manufacturing choices should be optimized for a given application. In this section, we describe some real examples of MCMs employing various combinations of technologies to suit specific product requirements.

2.7.1 Mainframe Computer Module

Figure 2-13 is a photograph of an MCM designed and built by Siemens-Nixdorf Information Systems for a high speed mainframe computer. It is 4" on a side and contains bipolar ASIC and memory components. The MCM substrate is a multilayer organic laminate (MCM-L). Substrate manufacturing is additive and sequential. Each layer is visually inspected and repaired as it is fabricated [17]. Chip mounting is flip TAB using thermode gang bonding. An elastic spacer on

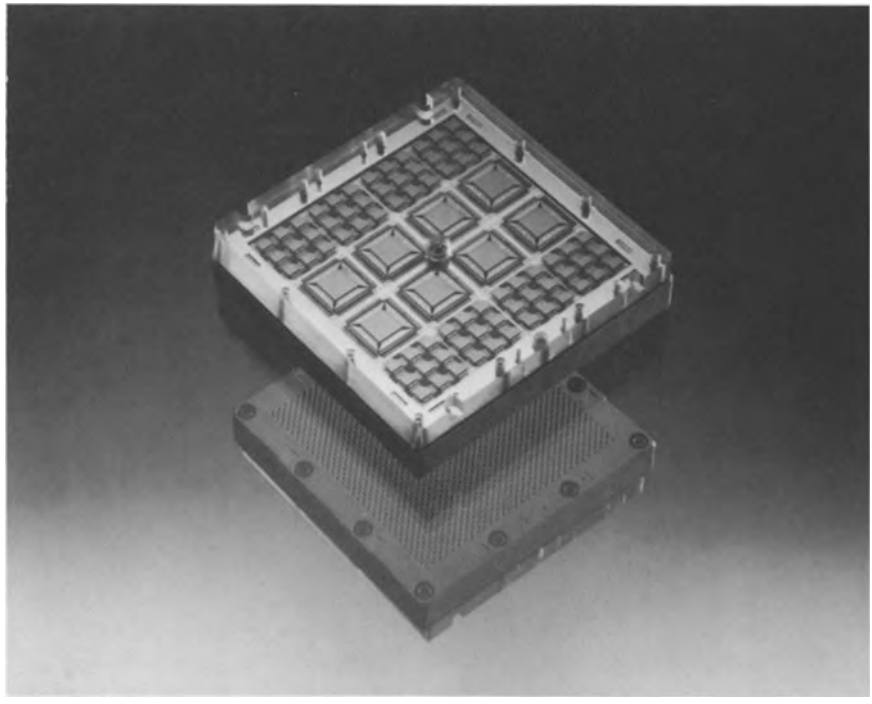

Figure 2-13 Mainframe computer module.

the front or active side of the chip presses the back of the chip directly against an anodized aluminum module lid forming an excellent path for heat transfer. The module can handle more than 500 watts of power. The substrate is mounted in a plastic housing that contains the unique module level I/O, with over 1,000 signals connecting to the mother board. The module I/O is an array of holes in the plastic housing with bifurcated springs designed to accept a matching array of pins mounted on the mother board. The entire module is repairable.

This MCM design is optimal for its intended application of packaging a large number of high speed, high power, expensive bipolar chips. High cost can limit the use of this technology for the general market.

2.7.2 Workstation Module

The MCM sketched in Figure 2-14a is aimed at the performance and density driven CMOS/BiCMOS marketplace, particularly, the departmental computer,

communications, peripherals, workstation and PC segments. It is a cost effective, high density MCM developed to accommodate high speed complex ASIC logic devices, microprocessors and memories.

The package body and MCM substrate are combined in a single substrate made of a ceramic base with deposited thin film copper/polyimide interconnect layers (MCM-D/C) [18]. The substrate provides very high density routing with 20 μm lines and 30 μm spaces on two layers. The chip mounting is flip chip, with a thermal gel material providing the heat conduction path between the backside of the chips and the thermally conductive lid. The module I/O is a JEDEC standard 299 pin grid array or a space optimized 50 mil pad array carrier [19] as pictured in Figure 2-14b.

This module is well suited for its intended application. It is capable of connecting 15 to 20 complex chips in a very small area. The power handling capability of 20 - 30 watts is matched to the expected power dissipation of CMOS components. The module offers optimum electrical performance at a cost that serves the market for performance oriented systems.

2.7.3 Low Cost Module

A very inexpensive module commercially available today is pictured in Figure 2-15a. The module, which offers advantages in system miniaturization and system performance, is a direct extension of a single chip QFP package. It utilizes a multilayer PWB substrate (package body and MCM substrate are integrated (MCM-L) with an embedded leadframe that forms the module level peripheral connection (Figure 2-15b). The chips are mounted using standard die attach/wire bond techniques, and the entire assembly is overmolded with plastic.

The major limitations of the module are thermal dissipation and routing density. Heat is primarily conducted from the chip to the copper leadframe The package can dissipate up to 4 watts under forced convection at 500 feet per minute airflow. Routing density is limited primarily by very large vias - 0.8 mm on the internal layers and 0.5 mm on the outer layers.

The technology offers low cost and low risk because it uses a minimum number of inexpensive piece parts and mature processing technologies. It is generally applicable to consumer and communications products where small size and low cost are important.

2.7.4 Data Communications Module

The module shown in Figure 2-16 is a prototype developed for a data communication application. The module consists of two host microprocessors

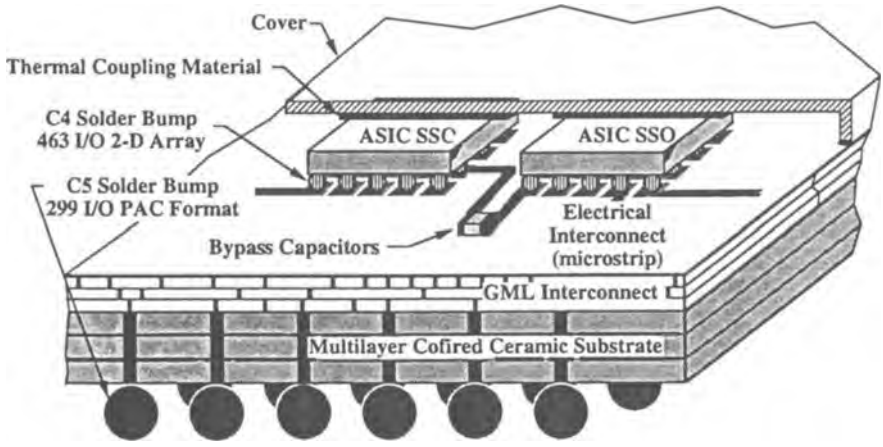

Figure 2-14a Schematic of workstation module.

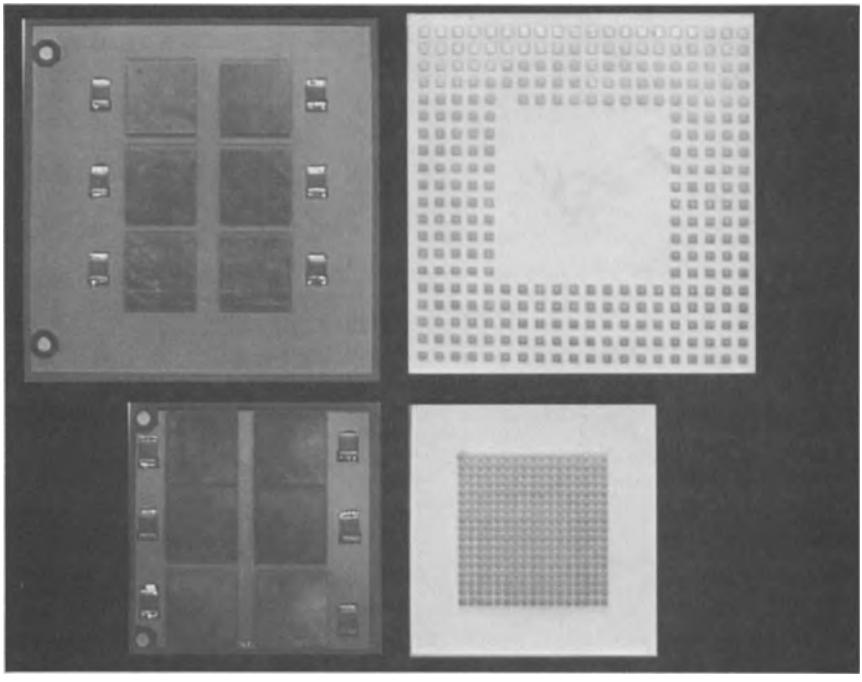

Figure 2-14b Two versions of a six chip C4/C5 workstation module: thin film copper/polyimide on multilayer cofired ceramic pad array carrier (PAC) substrate. Each chip has 463 I/O flip chip connections.

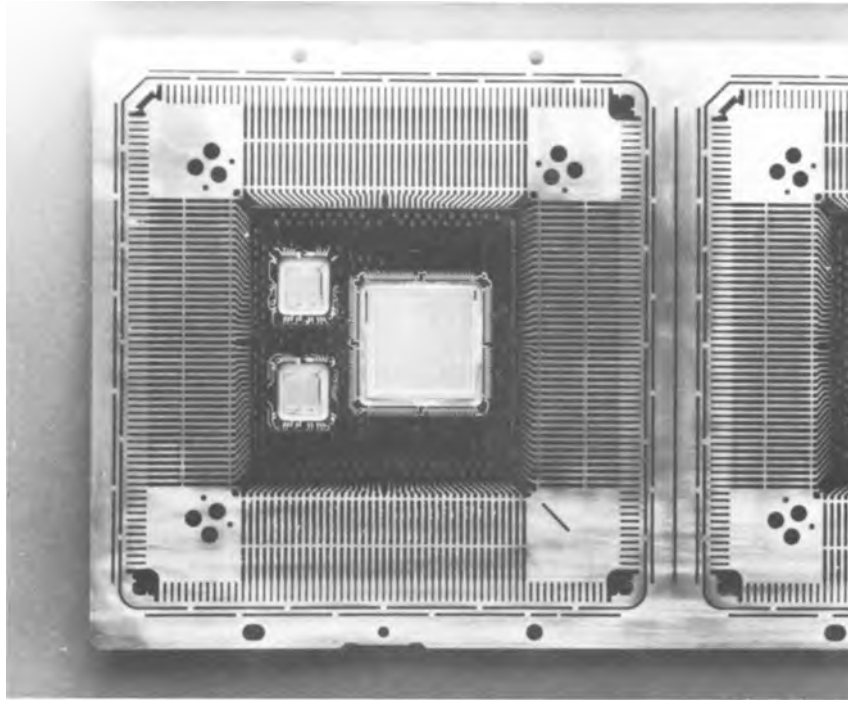

Figure 2-15a Low cost module.

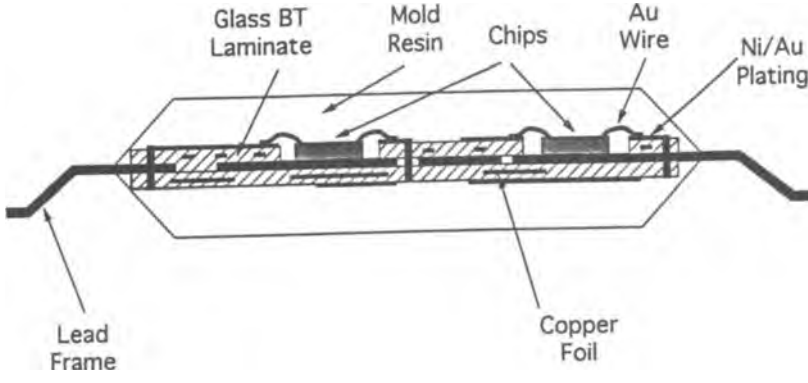

Figure 2-15b Schematic of low cost MCM with integral leadframe.

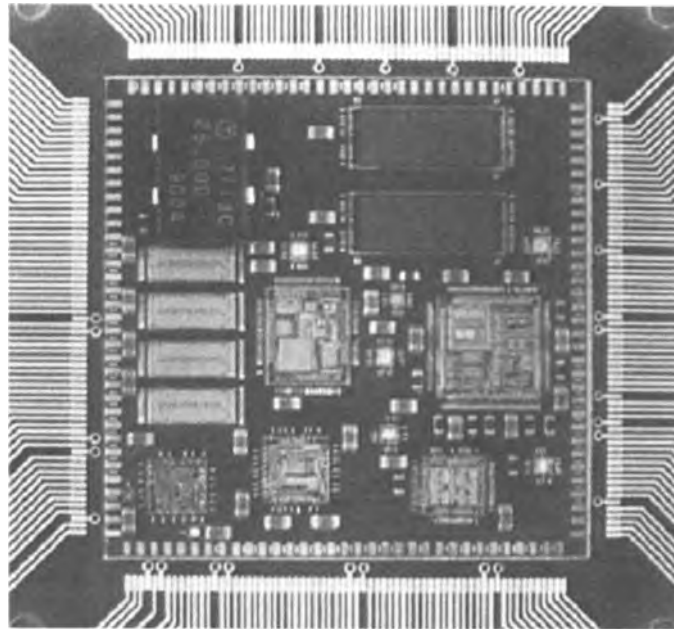

Figure 2-16 Data communications module.

with associated memory, a proprietary chip set and various passive devices. A total of 18 ICs and approximately 45 passive devices are assembled to a 1.8" × 1.8" four layer MCM-D substrate incorporating 75 μm lines and 30 μm vias. Die and wire bond assembly techniques are utilized for chip mounting. In this application MCM processing has made it possible to reduce the size from the original 30.0 square inch PWB to 3.24 square inch.

2.8 FUTURE TRENDS IN MCM MATERIALS MANUFACTURING

MCMs are a solution to the size, parasitic and path length effects of semiconductor packages and their interconnect. The multichip module (MCM) interconnection technology has been maturing as a packaging technology since the first articles were published in the early 80s. The first applications using MCMs used multilayer cofired ceramic substrate technology (HTCC). Low dielectric constant polymers with thin film conductor technology applied to

silicon, metal, alumina and cofired multilayer ceramic came later as more package and or chip I/Os were needed.

During this same period plastic quad flat package (PQFP) technology improved significantly with 0.3 mm pitch and up to 500 I/Os being planned for manufacture by 1993. PWB technology and MCM-L are also improving with 4 mil line and space and 6 mil via technology currently available and manufacturers talking about 2 mil line and space PWBs with 4 mil vias by the mid 90s.

With the exception of the very high end computer and military applications and the very low end consumer market, the use of MCM has been relatively modest. Most of the successful commercial users of MCMs have been vertically integrated mainframe computer companies. The successes have come from products derived from a system viewpoint, where the company has control of the subsystem and the components to achieve performance of the product at an acceptable cost.

If MCM technology is to approach the degree of acceptance in the marketplace to that of surface mount technology (SMT) today, issues relating to die availability, low cost substrate technology and the testing of bare chips and modules must be addressed.

An abundant supply and variety of good bare die must become available at an acceptable cost. Off chip performance will determine whether wire bond, TAB or C4 die configurations are suitable for use. As chip clock frequencies rise, the thrust will be to C4 die attach.

2.8.1 Substrates

Today, typical high density MCM-D substrates can cost anywhere from $50 to $100 per square inch, meaning that the substrate cost alone will deter many product designers from considering this packaging approach. A low cost MCM technology must evolve within the next several years if MCMs are to have a major impact across a broad spectrum of products. A high density MCM substrate cost below $5 per square inch must be achieved. A hybrid version of current MCM-L and MCM-D processing is a potential solution. For example, high density signal layers containing small vias fabricated by advanced processing such as laser ablation can be laminated to low density power and ground planes fabricated by conventional PWB processing. Since there is a cost premium for using the high density layers, utilization should be confined to a minimum of signal layers or for the redistribution from high I/O chips to the circuit board. The cost of such a module is expected to approach that of conventional PWB and current MCM-L technologies.

2.8.2 Optical Multichip Modules (MCM-O)

MCM prototypes intended for use at system clock rates in excess of 3 GHz have been fabricated by conventional copper/polyimide processing. Design guidelines for these high frequency modules have been proposed [20]. A potential next step in the evolution of MCMs that could overcome many of the difficulties associated with high frequency, hard wired MCMs is the use of optics for chip-to-chip interconnection. Optical transmission media exhibit terahertz bandwidth, immunity to electromagnetic interference and optical noninteraction. It has been demonstrated that properly designed thin film optical waveguides, physically intersecting with each other and transmitting optical signals, exhibit negligible crosstalk [21]. Therefore, chip-to-chip optical interconnect technology may not require a multilayer system as is required when using conventional, hardwired interconnections. The need for crossovers is eliminated or minimized. However, in practice, it is likely that hardwired and an optical layer will be used together, with the total number of layers significantly reduced from using hardwired alone.

Preliminary results have shown that high speed chip to chip optical interconnects, compatible with conventional MCM substrate processing, are feasible [21]. A semiconductor laser was coupled to a flip chip photodetector through a photolithographically defined polymer optical waveguide (Figure 2-17a). An infrared photograph of the interconnect taken during operation is shown in Figure 2-17b. Optical propagation is from left to right across a 2" ceramic MCM-D substrate. The resulting optoelectronic module is referred to as an optical MCM (MCM-O).

2.8.3 Test

Test methodology and technology to supply functional bare die and assembled MCMs must be developed to a point where testing is not perceived as an impediment to utilizing MCM technology. To assist in this area, standard MCM sizes and footprints (either perimeter or area array) need to be established. In addition, test and burn-in sockets need to be available.

2.8.4 Thermal Control

Thermal solutions for modules which provide for reliable thermal control at reasonable cost need to be developed. For high power applications, C4 die or flip TAB can offer the lowest thermal resistance path (back of die is exposed for heatsinking) without complicating the substrate layout, quite possibly making it the most viable packaging alternative for high power applications [23]. (See Figures 2.9 and 2.14).

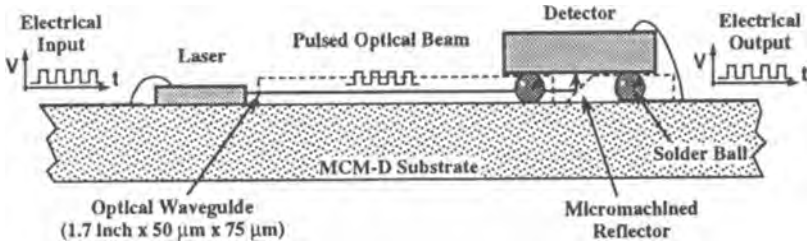

Figure 2-17a Schematic of a chip to chip optical interconnect.

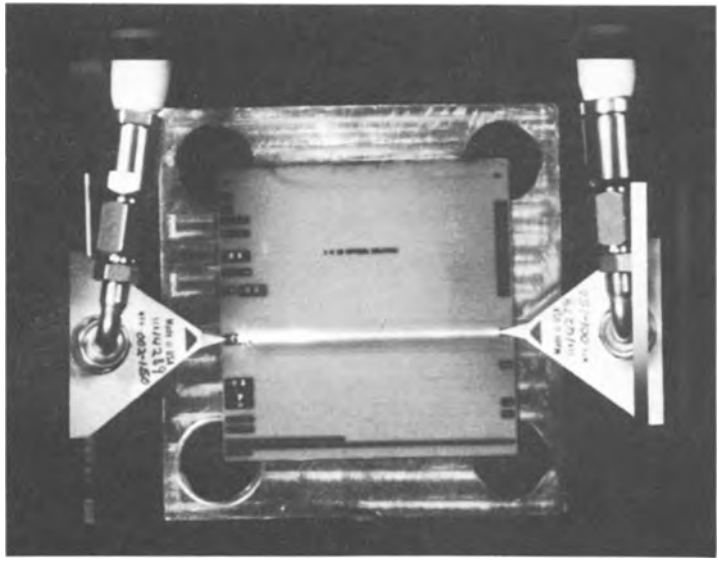

Figure 2-17b MCM-O operating at 1 Gbit/s NRZ.

2.8.5 Environmental Concerns

Finally, more environmentally sound processes need to be developed. The elimination of many toxic solvents and heavy metals from the fabrication of laminate materials and subsequent assembly processes is becoming an issue. The

move to eliminate solvents, such as methylene dianaline (MDA) from the manufacture of organic laminates [24] and chlorofluorocarbon (CFC) containing materials, has already begun. In addition, federal legislation is pending that limits or eliminates the use of lead from electronic assemblies [25]. OEMs soon may be responsible for recycling all lead containing products from inception to retirement - cradle to grave. As a result the industry needs to focus on developing non-lead bearing solders and conductive z-axis adhesives and cements.

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3

MCM PACKAGE SELECTION: A SYSTEMS NEED PERSPECTIVE

Paul D. Franzon

3.1 INTRODUCTION

There are a large number of packaging alternatives available to the design engineer today. This range is not likely to narrow in the near future. The object of this chapter is to provide a framework of understanding for making packaging decisions with the perspective of how best to satisfy the needs of an electronic system.

The design decisions made in any engineering venture are driven by cost and performance. Fundamentally, packaging acts to limit performance and to increase cost. Recent trends in integrated circuit technology suggest that system performance is being limited increasingly by the package. This has resulted in heightened attention to new, more highly customized forms of packaging used to improve system performance. Multichip modules (MCMs) represent a class of packages used to obtain significant improvements in system performance compared with conventional forms of packaging. Highly customized advanced packages are expensive when compared with off the shelf mass produced single chip packages. It is important to realize when advanced packaging is appropriate and when it is not. A primary aim of this chapter is to identify the nature of the tradeoffs involved and to suggest a decision-making process. The aim is not, however, to provide the reader with complete models for that decision-making. Many of the later chapters provide these models.

Fundamentally, there are three types of silicon found in a digital system. First, we find the very large scale integrated (VLSI) logic chips with over 100,000 transistors. Such chips range from general purpose microprocessors to special purpose application specific integrated circuits (ASICs). ASIC styles range from full custom and semi-custom designs to chips whose function is programmed in the manufacturing line. Second, we find the so called "glue chips," the off the shelf chips that provide functions not integrated into the VLSI chips. Today, more and more of the glue logic is being collected into and thus, is being replaced by ASICs. Typically, the only glue chips found are the drivers required to drive large loads and long lines and the receivers and latches that often are at the other end. Finally, we find the memory chips, which are often the most numerous [1].

The need for advanced packaging is driven by the trends in the design and use of these three types of chips. Today's leading CMOS microprocessor chips often contain over 1,000,000 transistors and are clocked at frequencies in excess of 150 MHz. The transistor count and clock speed are expected to continue to grow at a rapid rate, as shown in Figure 3-1. Leading edge VLSI chips create tremendous demands on the package. These chips have high I/O counts with 500+ I/Os being typical for 1992 RISC microprocessors. As the on-chip circuits become faster, the inter-chip package delay, not speeded up by using faster circuit technology, becomes dominant. One of the requirements for reducing this delay is that the chips be placed closer together. The increasingly fast signals produce lots of electrical noise in the package unless the package is carefully designed. The large number of fast circuits also produces lots of heat that must be removed from the system. For example, the DEC Alpha CPU chip dissipates over 30 W when running at a clock speed of 200 MHz.

The purpose of this chapter is to present a framework for making packaging decisions as part of the system design process. The next two sections set the stage for this by describing the system design process and defining the concept of the packaging hierarchy. Following that, the factors through which packaging decisions affect system performance and cost are presented and discussed. A process is then described showing how these performance and cost factors are used to make packaging decisions. An example is given of this decision process.

3.2 SYSTEM DESIGN PROCESS

The phases that make up the design process are summarized in Figure 3-2. In the system specification phase, the system requirements and goals are determined. How this is done is discussed toward the end of the chapter. Most of this chapter is concerned with the high level design phase, in which the

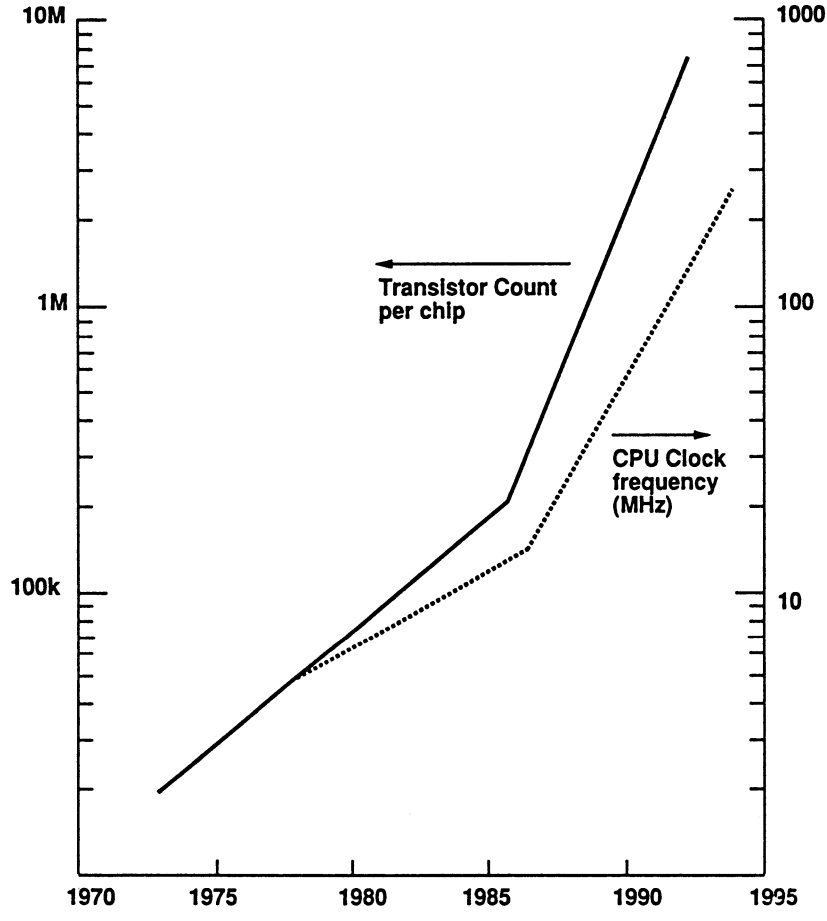

Figure 3-1 Microprocessor clock speed and the number of transistors per die are both growing at an increasing rate. (Adapted from [16].)

organization of the system, and the technologies to be used, are decided. This is described further in Section 3.6. In the low level design phase, the actual circuits are designed schematically. These are turned into layouts of the chips and packages during the prefabrication stage. A layout describes exactly where each transistor and part is placed and where each wire is run. Aspects of these phases are discussed in **Part B - The Basics.**

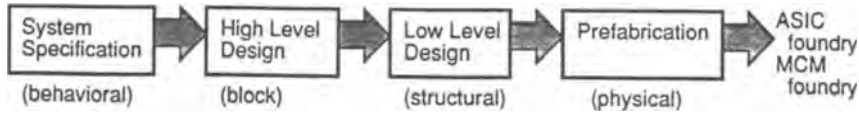

Figure 3-2 The system design process. (Adapted from a chart prepared by Ken Drake of MCC.)

3.3 THE PACKAGING HIERARCHY

Obviously not all systems fit onto one VLSI chip, one MCM or one printed wiring board (PWB). Thus, multiple levels of packaging are needed so that multiple chip packages can be interconnected. This is referred to as a packaging hierarchy, an example of which is given in Figure 3-3. At the lowest level of the hierarchy, the chips are mounted in single chip packages or MCMs. The next level of the hierarchy usually consists of PWBs (sometimes referred to as cards). The PWBs in Figure 3-3 are then connected together via a backplane (also referred to as a back panel, or sometimes board if the PWB was called a card). Backplane to backplane connections are made via a rack, and the racks then might be connected by some means, and so on. This is a very common hierarchy for larger systems though it is by no means the only one available.

Gate to gate interconnections (nets) might not go through this packaging hierarchy (for example, an on-chip interconnection) or might have to go through one or more levels of packaging. As any one net spans more levels of the hierarchy, the length of that net, and also the signal delay, increases substantially. Ideally, the interconnections and connections provided by the packaging hierarchy would be matched to the interconnection needs of the system. For example, Figure 3-4 shows how an electronic system could be considered as a set of interconnected functional blocks. In this case, the interconnection requirements of the system map naturally onto the packaging hierarchy shown previously in Figure 3-3. The nets that need to be short and fast are kept to the low levels of the hierarchy while nets that can be long span all of the levels of the hierarchy.

This ideal situation is rarely met. Most systems require more short nets than usually is provided by the packaging. The physical limitations of the packaging hierarchy (primarily determined by the desire to keep the sizes of individual packages and connectors down to control cost) force a number of these nets to go through more than one level of packaging. Unfortunately, the number of connections that go between package levels is limited by the capacity of the

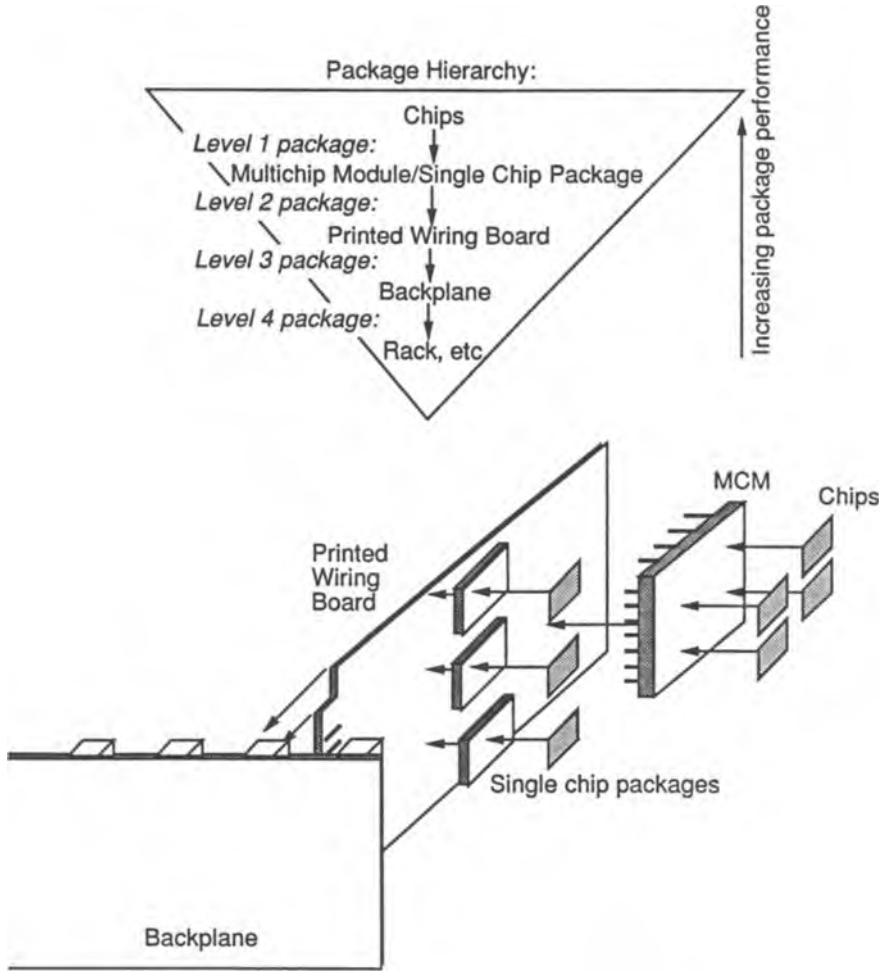

Figure 3-3 The packaging hierarchy.

connectors between levels (and high capacity connectors are expensive). If there are not enough paths available through these connectors then it might be necessary for several nets to share the same path (a bus or multiplexed path).

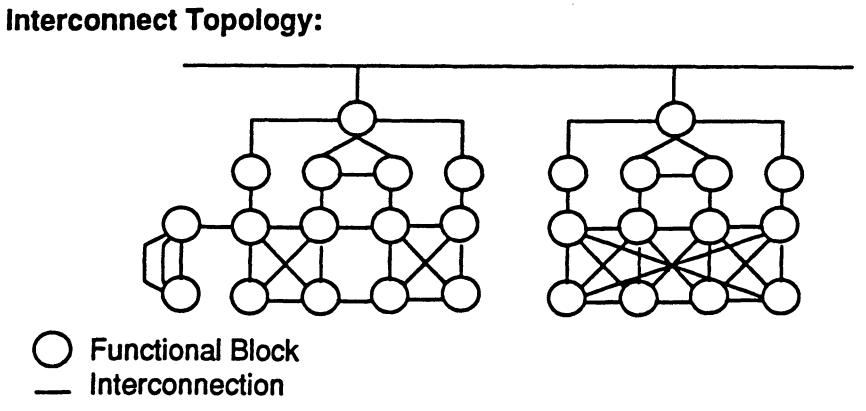

Figure 3-4 The interconnection needs between functional modules in a system often vary across a system. The packaging hierarchy should be structured so as to match these needs as closely as possible.

Thus, in many systems, a large number of nets take a double hit - they must span multiple levels of package and they must share a path with other nets. The job of the designer is to select the package technologies to minimize the number of nets that must run through the high levels of the package, and then to select

those nets carefully. A tremendous advantage of MCMs over conventional packaging is that they allow more of the nets to be concentrated in the first two levels of the hierarchy, thus improving the system performance.

There are several alternatives to the hierarchy style illustrated in the bottom of Figure 3-3. For example, sometimes the backplane might be bypassed with dedicated cable connections coming from the other side of the board. This can be extended even further to the situation where most of the interboard connections are dedicated wires. For example, this is done in Cray computers. A slight variation on the hierarchy shown in the bottom of Figure 3-3 is to have a relatively large motherboard with smaller daughterboards mounted on it. This is a common hierarchy in desktop and portable computer systems. It also is used to package the IBM 3081 computer central processing unit. In this case, the main board is 60 cm × 70 cm in size and the daughterboards are MCMs, each containing 100 chip sites [2]. Another hierarchy under active investigation is the use of connections in the third dimension to stack MCMs.

3.4 PACKAGING PERFORMANCE FACTORS

This section describes the factors that relate performance to packaging technology choices. Usually, each performance factor is broken down into the elements that determine it. In some cases, figures of merit used to differentiate package choices are discussed. A figure of merit is a number that attempts to summarize the packaging factor. The usefulness of a figure of merit depends on the accuracy needed to make a decision. Often a full model or evaluation is needed to make a decision.

3.4.1 Size and Weight

Size and weight are often specified as performance goals in many portable and aerospace systems. In the latter this is a primary driving force towards the application of MCMs (see Chapter 15).

A size restriction leading to the use of advanced packaging also might arise artificially. In any system, the size and possibly the weight of each subsystem only is estimated early in the design process. Errors might be made or system goals might change later while detailed design is in progress. In this case it might become necessary to use advanced packaging in a sub-system in order to avoid a complete redesign.

A size limitation might be an area or volume limitation or some mix of the two. For example, in a notebook computer, the height of the computer is limited by the height of the disk drive. Disk drive manufacturers are driven to package

the electronics portion of the drive in as small a height as possible, sometimes just a fraction of an inch. On the other hand, a few millimeters of height on the main computer board is not as important as the total area of the board.

If a size limitation is expressed as an area limitation, then a suitable figure of merit for evaluating different packaging approaches is the substrate efficiency. This is defined as the percentage of the substrate covered by silicon [3]. For example, if a 6 cm × 6 cm MCM has 10 0.8 cm^2 die placed on it, the substrate efficiency is given as 10 × 0.8 / (6 × 6) = 22%. Another useful metric is the number of gates per unit of substrate area. These figures sometimes are evaluated on a volumetric, rather than an area, basis.

Particular attention also must be given to the size and weight of the power supply (battery) and the mechanical structures used to remove heat. This might involve a compromise between the desire to use a small system to house the electronics and the need for a large heat removal structure required by a small system with a high heat density.

By replacing multiple single chip packages with an MCM, substantial size and weight reductions are achieved. The closest comparable single chip package solution would be to use ASICs in surface mount packages on a PWB. The magnitude of the reduction possible with an MCM solution depends, in part, on the interconnection capacity needed.

3.4.2 Interconnection Capacity Within Each Level

Interconnection capacity refers to the total amount of wiring provided within a level of the packaging hierarchy. This wiring is provided by layers within the package devoted to signal interconnections. The physical layout of the wires is determined by a routing Computer Aided Design (CAD) tool. Additional layers are usually used for distributing power and ground. Once the details of the parts to be interconnected are known, the package interconnection (or routing) capacity requirement is expressed in the following form [4]:

$$\text{Required Interconnection Capacity} \approx RN_{net}P/E \qquad (3\text{-}1)$$

with the result expressed in units of length. In this equation, E is the efficiency with which the available interconnect capacity can be used (often called routing efficiency and typically takes a value of around 50% [4]), R is the average length of each net (interconnection) in terms of chip pitch, N_{net}, is the number of nets and P is the average chip pitch, the average distance between chip centers.

The available interconnection capacity is given by:

$$\text{Available Interconnection Capacity} \approx \frac{\left(\sqrt{N_{chip}} - 1\right)^2 P^2 \times \text{Number of signal layers}}{\text{Average wire pitch}} \quad (3\text{-}2)$$

plus any capacity around the periphery of the board. Here N_{chip} is the number of chips.

A figure of merit often used to compare different packaging technologies is the interconnection density:

$$\text{Average Interconnection Density} = \frac{\text{Number of signal layers}}{\text{Average wire pitch}} \quad (3\text{-}3)$$

Figure 3-5 shows how interconnection density is calculated for a single layer. Figure 3-6 gives a plot of interconnection density and cost per unit area for different interconnection technologies. Wiring capacity is then given by:

$$\text{Available Interconnection Capacity} \approx \left(\sqrt{N_{chip}} - 1\right)^2 P^2 \times \text{Average Interconnection Density.} \quad (3\text{-}4)$$

If the available capacity is less than the required capacity then, short of redoing the high level design, there are six choices:

1. Share (multiplex) signals onto the same interconnections, for examples, reduce N_{net}. This is often done on backplane busses. If it is likely that several functional modules need the same physical line at the same time then performance degrades.

2. Increase the number of signal layers thus increasing weight, size and cost. Typically, the total number of layers increases at a rate almost one and a half times the rate of increase of the number of signal layers. In a high speed system each signal layer has to be next to a power or ground layer (see Section 3.4.4 and Chapter 11). If through-hole components are used on a PWB, the maximum number of layers is limited to 10 or 12 (usually equivalent to a maximum of 8 signal layers).

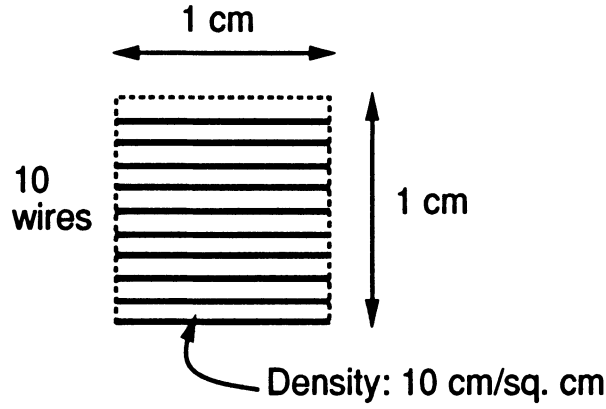

Figure 3-5 How interconnection density is measured.

3. Increase the chip pitch, P, and the size of the board or substrate. This then increases weight, size, cost and delay.

4. Spend additional design time to try to increase the routing efficiency, E, by manually, rather than automatically, routing the nets.

5. Reduce the number of chips by using an ASIC.

6. If the via size is larger than the wire width, thus consuming area that could have been used for wires (see Figure 3-7), then reducing the via size will allow an increase in interconnection density. This is common in PWBs and laminate MCMs.

In general, the finer the average wire pitch and the greater the total interconnection density, the less likely that these undesirable steps are required. In particular, thin film MCMs rarely have insufficient interconnection capacity. The average wire pitch is not always the same as the minimum wire pitch, typical values for which are given in Table 3-1. There are two reasons for this. First, in high speed systems, wires need to be pitched further apart to control crosstalk noise. This is discussed in Chapter 11. Second, via size and style can have a dramatic impact on average interconnect density.

If there are insufficient via sites on the board or MCM, it might be difficult for a router to find a via where it needs one. This is referred to as via

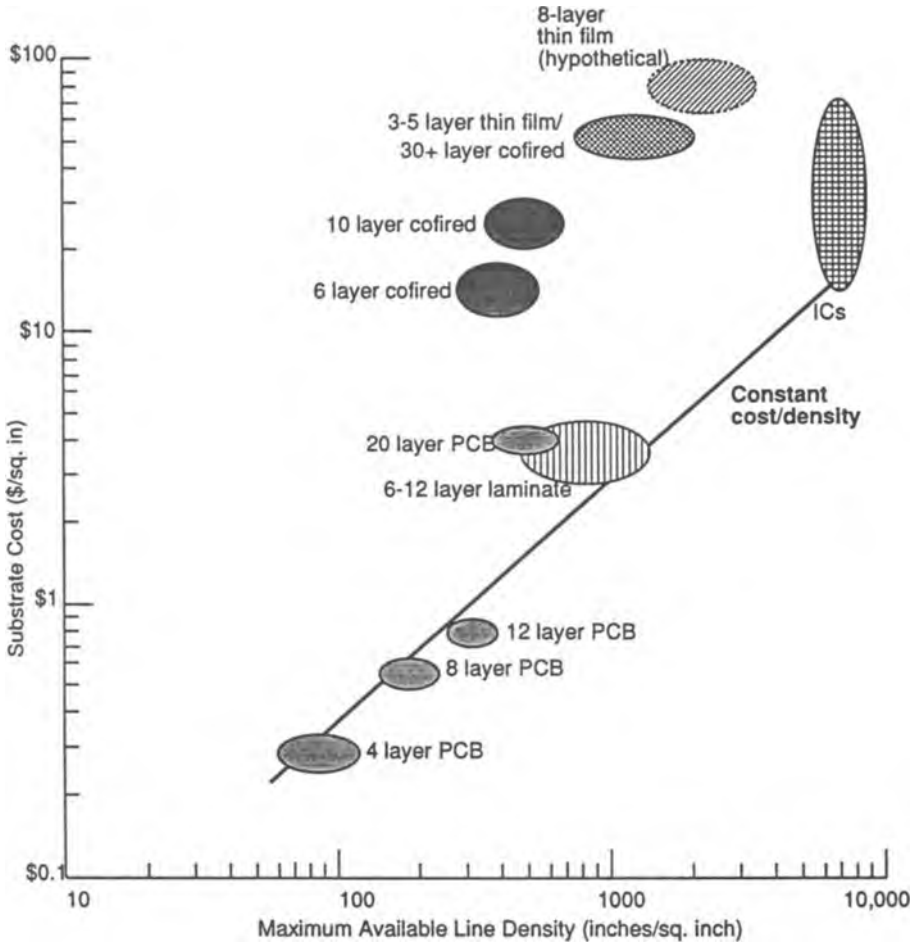

Figure 3-6 Substrate cost (1992) versus interconnection density. (Adapted from [18] with updated prices based on typical 1992 vendor costs.)

starvation. As a rule of thumb, if there are fewer than 1.5 to 2 via sites per signal pin, then the router efficiency, E, decreases [4]. This is particularly a problem with the through hole vias commonly used in PWBs since the number of via sites does not increase as the number of signal layers increases. With high layer count boards and laminate MCMs, buried vias are required to compensate for this. The use of large PWB and laminate MCM vias also can result in via

Table 3-1 Typical Minimum Line Pitches.

TECHNOLOGY	MINIMUM WIRE PITCH	MINIMUM VIA PITCH
Cofired Ceramic MCM	150 μm - 250 μm	250 μm
Thin Film MCM	20 μm - 40 μm	20 μm - 200 μm
Laminate MCM	100 μm - 250 μm	1000 μm - 2500 μm
PWB	250 μm - 300 μm	1000 μm - 2500 μm

starvation. Referring again to Figure 3-7, it can be seen that between every row of vias there are several wires (two or three are typical). This low ratio of wires to vias might also make it difficult for a wire always to find a via where it needs one. In thin film and ceramic technologies the via size can be the same as the conductor size. Buried vias are the norm. Thus, the effects of vias on interconnection properties in these technologies are usually minimal.

Interconnection properties interact with the choice of connection techniques used between levels of the packaging hierarchy. For example, if an edge style of connection is used (such as wire bonding or TAB for the first level connection) then the pads on the chip might have a center to center pitch as small as 75 μm (though 150 μm or more is typical). If the pitch of the wires on the substrate (Table 3-1) is larger, then the chip connect function must include fanout for pitch matching, as shown in Figure 3-8. Making room for this fanout increases the minimum possible chip pitch, P. This is one important reason why conventional packaging tends to have poor substrate efficiencies. Providing this fanout to match a 0.35 - 0.5 mm PWB surface pad pitch makes high pin count surface mount packages large (while a small pin count package, such as a memory, is small). Providing fanout often is necessary even on laminate and cofired ceramic MCMs. It is not necessary on a thin film MCM.

On the other hand, with area connection (such as flip chip solder bump), the pad or pin distance on the chip must be equal to or larger than the minimum via spacing in the package. Providing this fanout to match a 0.1" PWB via pitch makes high pin count pin grid arrays (PGAs) large. The signal layers underneath the chip then are used to bring these signals out from underneath (escape) to be routed to other chips at the required pitch. This consumes some of the interconnection resources underneath the chips. It is important to ensure that sufficient interconnection resources remain underneath the chip for normal interconnections. This is often a problem underneath high pin count PGAs. IBM solves this problem on their flip chip MCMs by assigning special layers (redistribution layers) for the escape function in the Thermal Conduction Module. These layers also perform test and rework functions. Again, the impact is minimized if thin film layers are used.

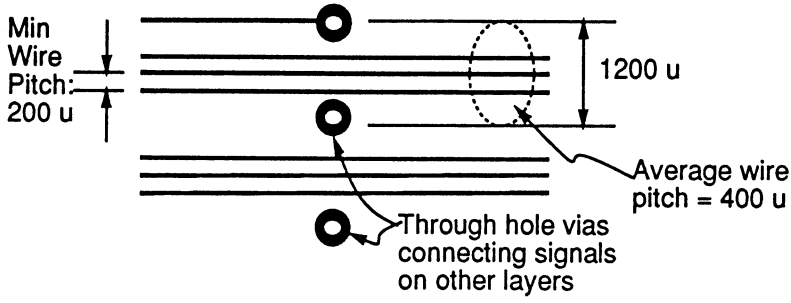

Figure 3-7 One effect of via size on wire pitch.

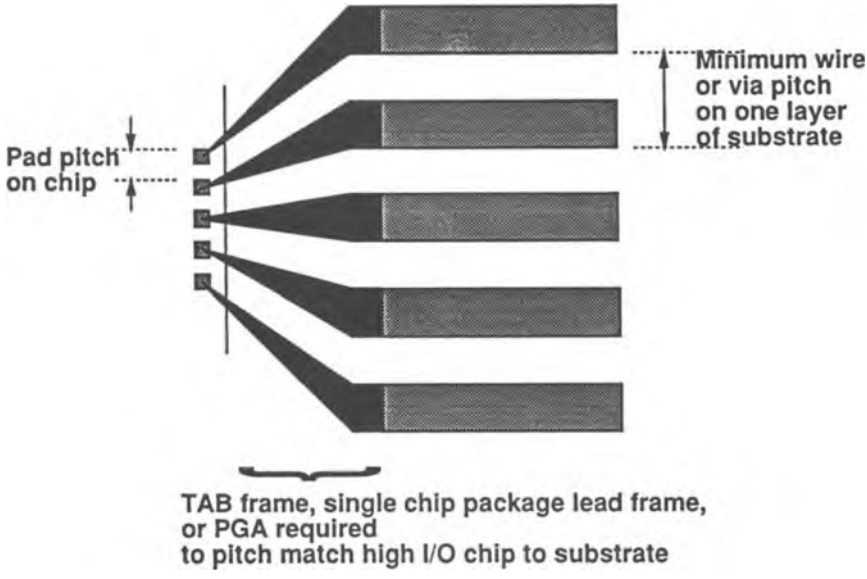

Figure 3-8 Fanout often is required to pitch match the chip pads and the package pads.

3.4.3 Connection Capacity Between Packaging Levels

The connection capacity between packaging levels is much smaller than the interconnection capacity within a level. For example, consider an MCM connected to a PWB. The pin pitch of the connector that goes between the two package levels typically is limited to either the wire pitch of the PWB on one layer only, or to the through-hole via pitch of the PWB, usually the latter. The capacity implied by either of these pitches is much less than the capacity, over a similar cross section, of either the PWB wiring or the MCM wiring. Furthermore, the cost of large high pin count connectors can be very high. (See Chapter 10 for a discussion on MCM to PWB connectors generally and Chapter 18 for a discussion on cost.) This is why richly interconnected systems tend to use large MCMs and large PWBs to minimize the use of connectors and backplanes. By flattening the packaging hierarchy in this way, the bottleneck created by the low capacities of the higher levels of hierarchy and the connectors to them is minimized. For example, the IBM 3081 main CPU board contains nine 9 cm × 9 cm MCMs placed on a 70 cm × 60 cm PWB. However, a large MCM is more expensive to produce than a collection of smaller MCMs. There is a tradeoff between substrate size and connector capacity.

Performance often is compromised to reduce connector capacity requirements between different levels of the hierarchy. For example, the only significant difference between the Intel 386DX microprocessor and the Intel 386SX microprocessor is that the latter provides fewer pins on the single chip package for the memory interface. This reduces the effective performance of the latter but does make it less expensive.

An important factor determining the connection capacity between levels is whether an edge or area connector is used. For example, Figure 3-9 plots the total number of pads versus pad pitch for both area and edge connectors for the IC to MCM interface. With area connection, more connections are made with reduced manufacturing tolerance than with edge connections. This is a major advantage for flip chip with solder bump technology. It is also a major advantage for PGAs and other area array single chip and multichip packages in comparison to peripheral pinned packages such as surface mount. The subject is discussed in more detail in Chapters 10 and 18.

The above discussion assumes the required connection capacity between levels is known. However, often it is not known and must be estimated. A good estimation of the required signal pin capacity, N, for the signals leaving any level of packaging is given empirically by Rent's rule:

$$N = KM^{p} \tag{3-5}$$

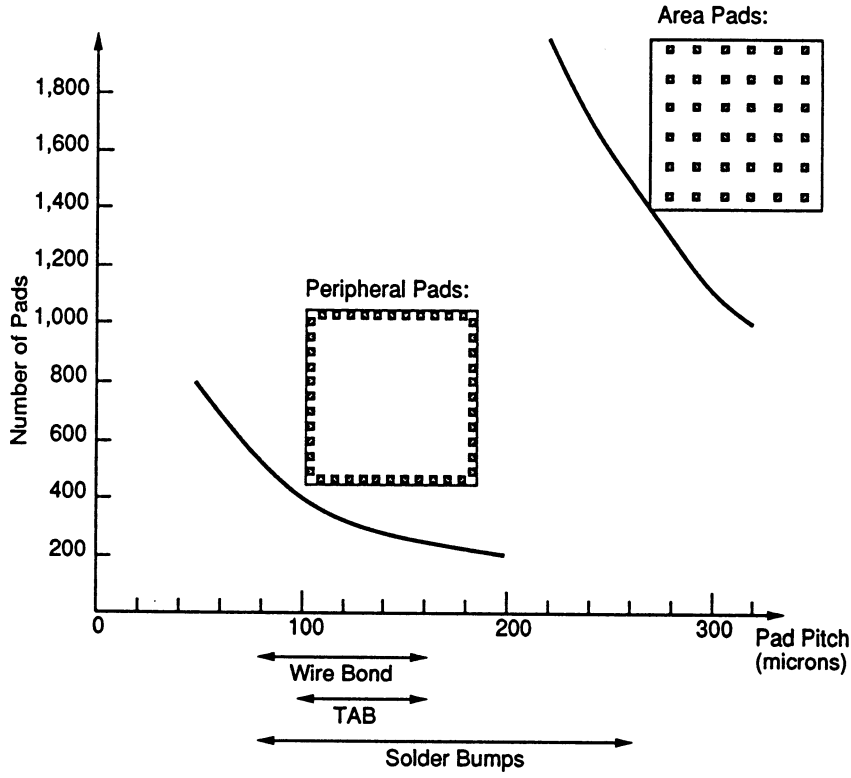

Figure 3-9 Number of I/O pads for a 1 cm^2 chip with peripheral and edge arrangements.

where K is a constant of proportionality, typically about 2.5, M is the number of circuits contained within the lower level of the hierarchy, and p is Rent's constant (typically $0.5 < p < 0.7$). However, it should be noted that K, M and p are determined empirically. Rent's constant tends to decrease with large increases in the number of circuits. (Consider the number of signal pins leaving a personal computer box versus the number leaving a CPU chip; they are roughly comparable indicating a sharp decrease of p with M.) It should be remembered that N does not include the power and ground pins. In high performance systems there can be almost as many power and ground pins as signal pins to control electrical noise.

For modest increases in the number of circuits, M, contained within a package, the number of pins required, N, usually increases. Thus, as further transistor miniaturization occurs, there is an increased requirement for interlevel connectivity. Interlevel connections become an important technological constraint on the package performance, as discussed in Chapter 18.

3.4.4 Delay and Electrical Noise

Delay refers to the time required for a signal to travel between the functional circuit blocks in a system. To a first order approximation, packaging-related delay is broken up into the following contributions (Figure 3-10):

$$t_{delay} = t_{buffer} + t_{flight} + t_{rise\text{-}time\text{-}degradation} + t_{noise\text{-}settle} \quad (3\text{-}6)$$

where t_{buffer} is the delay incurred within the buffer-amplifier, t_{flight} is the time taken for the signal to travel (fly) along the wire at nearly the speed of light, $t_{rise\text{-}time\text{-}degradation}$ is the extra delay incurred because of an increase in rise time of the signal (the time for the signal to transition between the two different logic voltage levels) on the rise time as compared to the signal at the input of the buffer. $t_{noise\text{-}settle}$ is the extra delay that must be incurred while waiting for electrical noise to settle.

If the buffer is small and weak, then t_{buffer} is small but $t_{rise\text{-}time\text{-}degradation}$ is large. The delay $t_{rise\text{-}time\text{-}degradation}$, is determined mainly by the ability of the buffer output to charge and discharge the capacitances associated with the interconnection. Part of this capacitance comes from the chip attach leads and $t_{rise\text{-}time\text{-}degradation}$ improves as the chip attach leads get smaller. Thus smaller buffers are sometimes used in chips intended solely for MCM use. If the line is lossy (resistive), then $t_{rise\text{-}time\text{-}degradation}$ is increased further. Thus it is desirable to have low loss lines.

The minimum time for the signal to travel down the line, the time of flight, is given by:

$$t_{flight} = \frac{l}{c/\sqrt{\varepsilon_r}} \quad (3\text{-}7)$$

where l is the length of the interconnect, c is the velocity of light in a vacuum and ε_r is the relative dielectric constant of the insulator. Typical values for

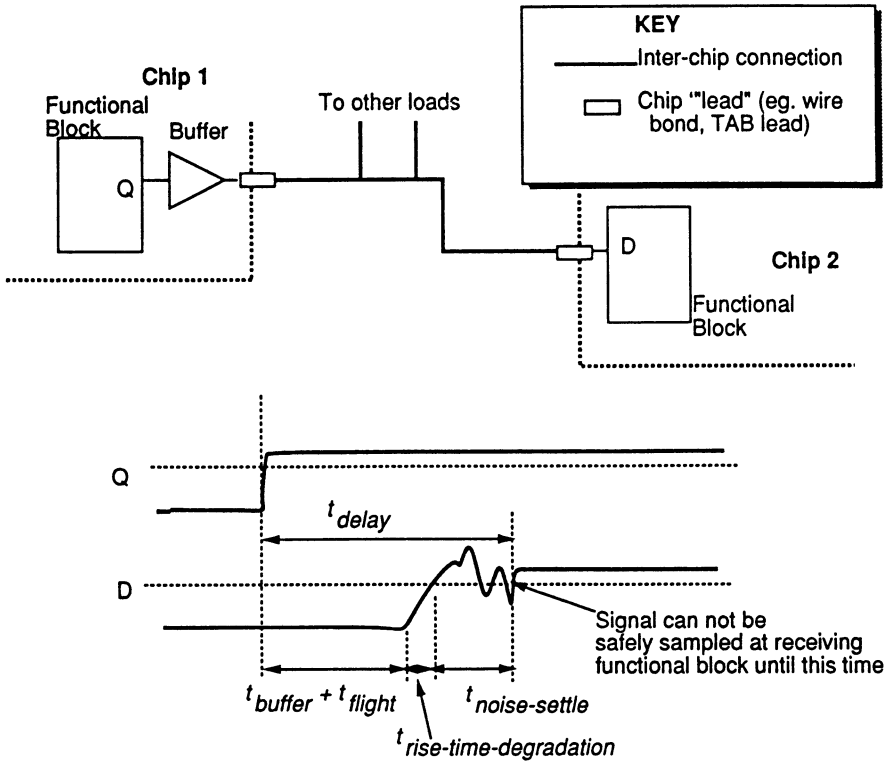

Figure 3-10 Electrical delay.

dielectric constant are given in Chapter 2. In a high speed system, total delay time is limited primarily by the time of flight. This is a driving force behind using packaging types that allow parts to be more closely spaced (reduce *l*) and for using dielectric materials with lower values for dielectric constant, such as glass-ceramic for cofired ceramic MCMs, polyimide for thin film MCMs and cyanite ester or polyimide for laminate MCMs and PWBs, as discussed in Chapter 1.

Whenever transitions occur on digital signals (0→1 or 1→0), electrical noise is introduced both on the wire (connection or interconnection) carrying the signal and on the wires around it. This noise contributes to the package parasitics

defined in Chapter 1. In digital systems, noise considerations indirectly affect system performance. For example, Figure 3-10 shows how increased noise is equivalent to an increase in delay on data lines for digital systems. For clock signals and analog signals, excessive noise will directly compromise correct system function. This is discussed further in Chapter 11.

There are three major sources of noise within a digital system: reflection noise, crosstalk noise and simultaneous switching noise. The system also produces noise that affects the operation of systems around it (and itself is susceptible to such noise produced by other systems). This is referred to as electromagnetic interference (EMI) noise. The magnitude of all of these noise sources depends on the rise time, t_{rise}, of the signal. The faster the rise time, the worse the noise.

Reflection noise is a potential problem if the time of flight becomes comparable with the rise time

$$t_{flight} > t_{rise}/5 \rightarrow t_{rise}/3. \tag{3-8}$$

When this is the case, the signal edge needs to see a constant impedance as it travels along the line. Whenever the impedance changes, part of the signal is reflected just as part of a light signal is reflected when it encounters a sheet of glass.

The characteristic impedance, Z_o of a wire is given by:

$$Z_o = \sqrt{L/C} \tag{3-9}$$

where L is the inductance per unit length of the line and C is the capacitance per unit length. Maintaining a constant (termed controlled) characteristic impedance requires that L and C remain constant along the length of the line. Doing this requires that the signal line maintain a constant cross sectional geometric relationship with a reference line or plane, either ground or power. Examples of controlled impedance lines are given in Figure 3-11. The most common approach is to use microstrips and striplines, creating the need for reference planes. Typically, offset striplines are used instead of striplines wherein there are two signal layers between each pair of reference planes. Thus in most digital systems there are typically about half as many reference planes as signal planes (reference layers can be shared by signal layers).

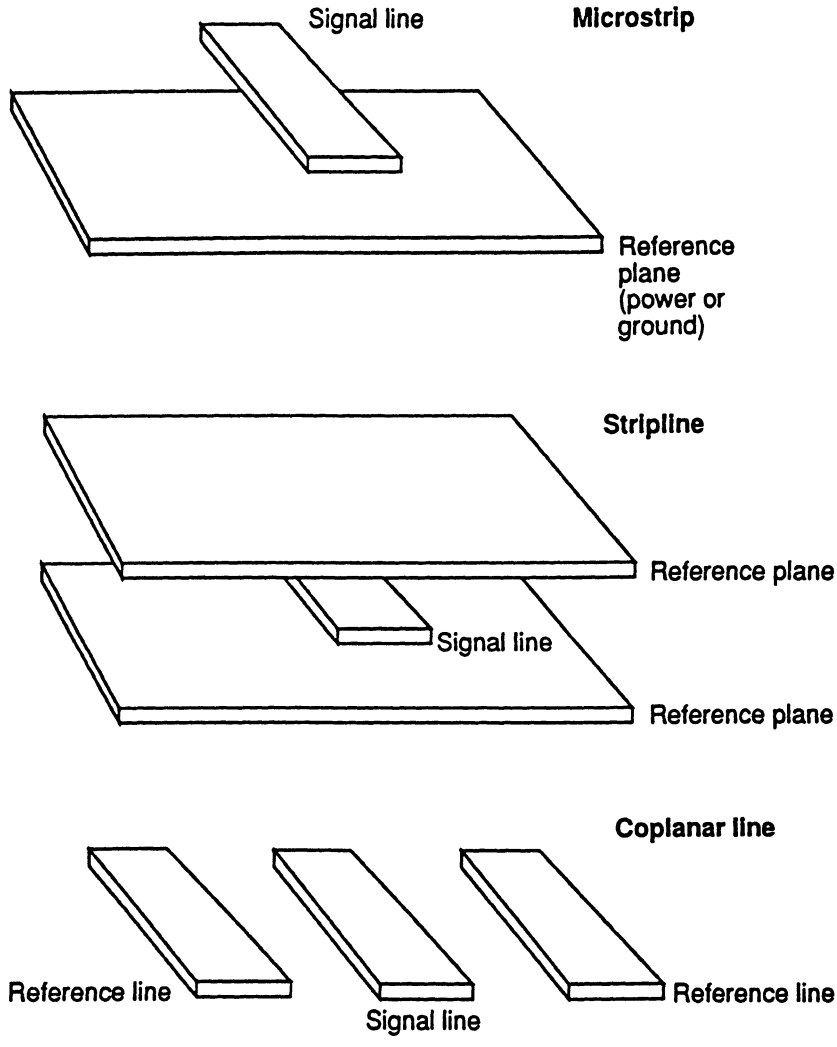

Figure 3-11 Examples of controlled impedance lines.

Also, if a matching terminating resistance, $R = Z_o$ is not placed at one end of the line, then part of the signal is reflected there. This reflection travels up and down the line, interpreted by the receiver as noise. Without a matching

termination, reflection noise can be controlled by keeping the line short (see Chapter 11):

$$t_{flight} < t_{rise}/4. \tag{3-10}$$

Crosstalk noise arises whenever signal lines or chip connect leads run parallel to each other. The signal on the active line couples onto the quiet line as noise. The faster the rise time, the greater the coupled noise. Crosstalk noise is controlled by placing the lines further apart than the minimum line spacing and, sometimes, by limiting the coupled length. Thus, the greater the potential impact of crosstalk noise, the lower the interconnection density is. Chapter 11 discusses how crosstalk noise considerations also lead to the use of reference planes and allow lines to be more closely spaced when the dielectric constant is reduced. One advantage of cofired PGA packages over most plastic packages is the provision for these reference planes within the package.

Simultaneous switching noise occurs whenever a large number of off-chip or on-chip drivers switch at the same time, as shown in Figure 3-12. This switching activity causes a large current spike to flow through the ground and V_{CC} connections. When this current spike flows through the inductance associated with the ground and power circuits a noise voltage will appear on the chip's internal power and ground lines. The magnitude of this noise is given approximately as:

$$V_{SSN-noise} = L_{eff} N \frac{dI}{dt} \tag{3-11}$$

where L_{eff} is the effective inductance of chip ground or V_{CC} connection, N is the number of switching drivers, and dI/dt is the current transient produced by each buffer. The effective inductance, L_{eff}, also can be substantially reduced through the use of shorter chip attach leads and by placing ground planes beneath the leads. As a rule dI/dt increases with decreasing rise time. This noise causes false switching inside the chip, appears as noise on the output leads of any quiet buffers connected to the ground or power rail and increases delay in the switching drivers. One major advantage of MCM technology is that the effective inductance is greatly reduced in comparison to single chip packages. This is particularly true for solder bump and multimetal TAB attachments (TAB with a ground plane).

For the same set of chips, all of these sources of internal noise are usually smaller in an MCM package in comparison to PWB packages. In particular, the shorter connection distances reduce reflection noise as well as the accumulation of crosstalk noise, while the smaller chip connection inductances reduce the amount of simultaneous switching noise. Noise is easier to control in MCMs and its impact on delay is smaller. However, noise usually can be adequately managed in single chip packages. Many packages, particularly ceramic PGAs, provide internal reference planes or ground and power planes for the purposes of controlling noise. Though few plastic packages currently have these planes, some are starting to make limited use of them.

EMI is produced by the package circuits whenever current flows within them. The connections act as antennas producing radiated noise. Meeting required standards for EMI noise can be difficult and often requires the use of metallic screens in the box. One advantage of MCM technology is that it reduces the size of many of these antennas and, potentially, the need for screening.

It is important to note, however, that as transistor speed increases, rise time decreases and noise control becomes more difficult. The subject of electrical delay and noise control is discussed further in Chapter 11.

3.4.5 Power Consumption

Power consumption usually impacts system performance through its indirect impact on size and weight. For example, in a notebook computer, weight considerations dictate the battery size and energy. Thus, to make a computer that lasts four hours on one battery means carefully controlling the power consumption. Similarly, in aerospace systems, increasing power also means increasing the weight of the power supply. In telecommunications systems, power consumption must be controlled so that the batteries required to power the system in the event of a power failure are not too large. Controlling power consumption also reduces power dissipation (the two have the same value), thus reducing the need for complex and large heat removal structures.

Whenever a 0-1-0 transition occurs on an interconnection, the amount of energy consumed in charging and discharging the interconnection capacitance is given by:

$$\text{Energy} = CV^2 \tag{3-12}$$

where C is the total capacitance of the interconnection and V is the voltage swing. The power consumed is this energy per transition times the number of

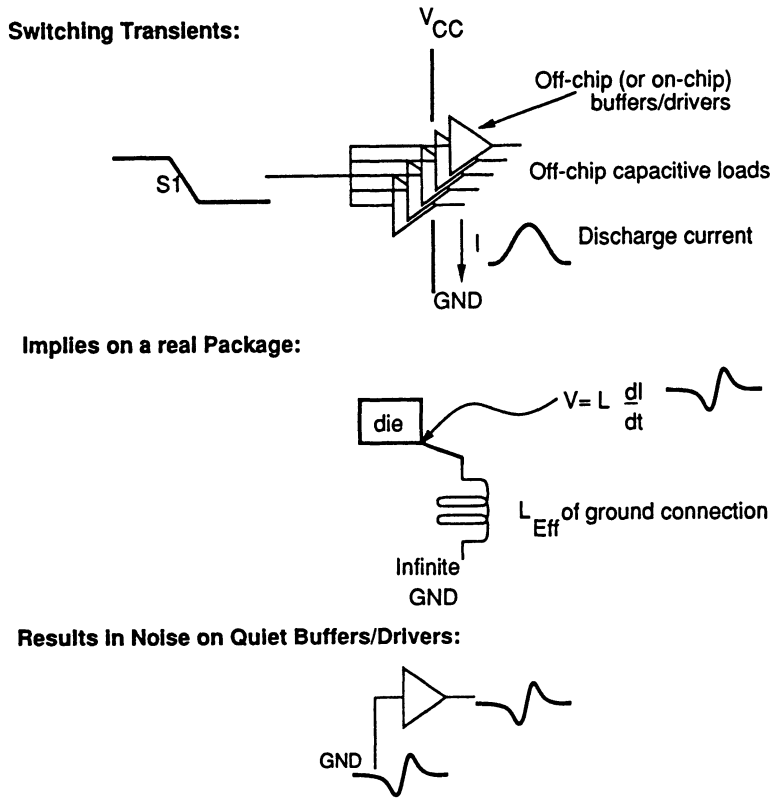

Figure 3-12 Simultaneous switching noise in digital systems.

transitions per second. Therefore, in any CMOS circuit where capacitive energy is the main form of power consumption, the power consumption increase is directly proportional to frequency of operation.

As the capacitance, C, is proportional to the length of the interconnection and the size of the chip attach, one advantage of MCM technology is reduced power consumption. For example, let us say that 10% of the system power consumption is due to the interconnect when mounted on a PWB and that migration of the product to an MCM reduces the power consumption due to the interconnect by a factor of five. Then the MCM product either would consume

8% less power than the PWB-based product or could be allowed to run at a faster rate of transitions per second (frequency) with no increase in power consumption.

3.4.6 Heat Dissipation

Consumed power is converted directly to dissipated heat. As the clock frequency and the number of transistors per chip increase, the heat produced by the chip increases. This heat causes the temperature of the chips to rise. With CMOS chips, higher temperatures affect system performance directly by slowing the transistors. In any system, high temperatures decrease the reliability. To maintain reliability, other performance factors might need to be compromised to improve heat removal. The structures used to remove heat might add considerably to the manufacturing cost. Thus, thermal issues are very important in MCM design because the heat density is much higher than in single chip packages, making cooling more difficult.

Heat is removed mainly by conducting it away from the chips and allowing it to convect into a circulating coolant. There are generally two choices for the heat conduction path: through-the-substrate or directly off the back of the chip. Also there are generally two choices for the coolant: air, often forced by a fan(s), or water (or another other liquid such as a fluorocarbon), often forced by a pump. Some possible combinations are shown in Figure 3-13. Unfortunately all of these alternatives involve some compromise in either another performance or cost factor.

Generally it is considered that through-the-substrate forced air cooling is the cheapest alternative. (Hence its very aggressive use by DEC, as described in Chapter 17.) An air cooled system has a number of advantages over a water cooled system. It reduces the need for expensive plumbing and seals. An air cooled system also is more likely to survive a fan failure than a water cooled system would a pump failure. By making the parts more accessible, maintenance and field repair costs are reduced. Through-the-substrate cooling tends to require less precise mechanical engineering than chip backside cooling and further helps in making the parts more accessible for repair.

The use of through-the-substrate forced air cooling might require some performance compromises. First, its use requires a highly conductive thermal path through the substrate. Unfortunately, the materials with the lowest dielectric constant such as glass-ceramic or polyimide tend also to have the lowest thermal conductivity (Tables 7.1 and 12.1, for example). This can be overcome by using either copper slugs, commonly called thermal vias, beneath the chip or sinking the chip into the substrate (Figure 3-14). This substantially reduces the capacity beneath the chip, particularly for laminate MCMs where the slug consumes all

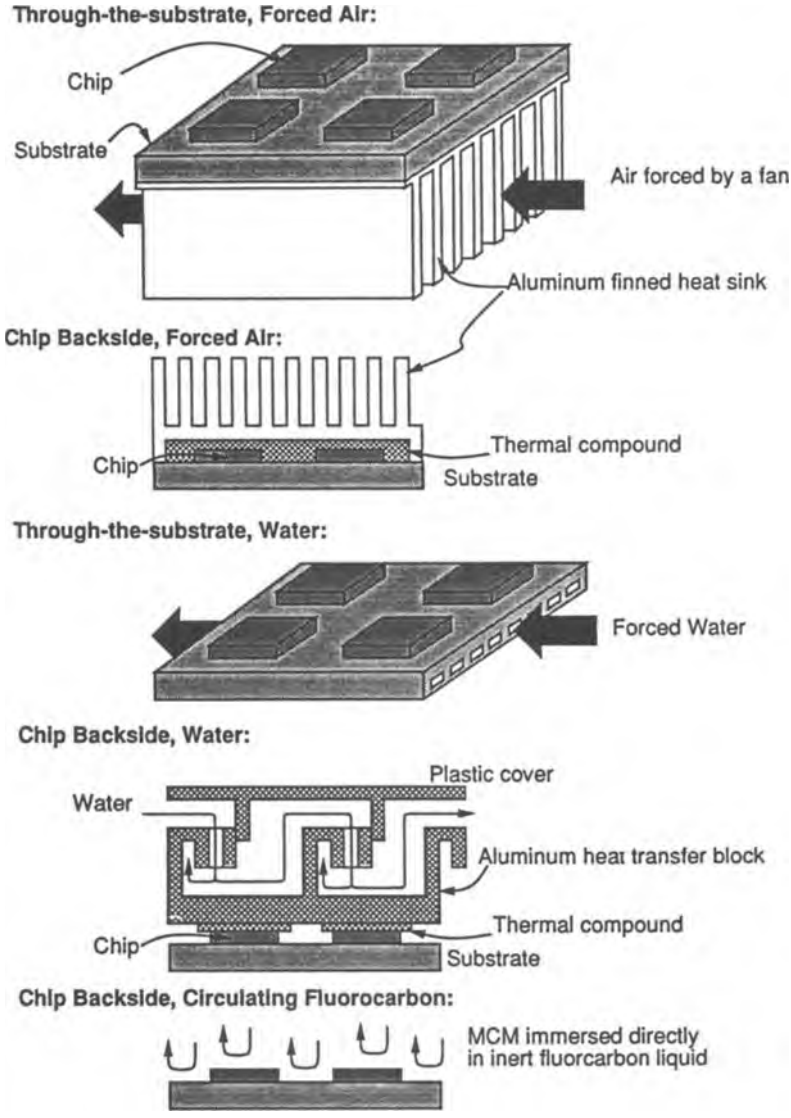

Figure 3-13 Some of the alternatives that can be used to cool an MCM.

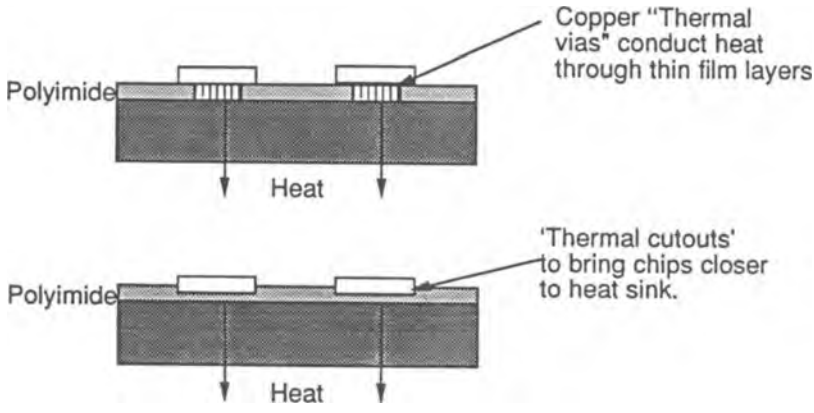

Figure 3-14 Thermal vias and thermal cutouts.

of the area beneath the chip. (Alternatively, an array of through-hole vias can be used, but their efficiency is limited.) The resulting lack of interconnect capacity might force an increase in chip pitch, P, and thus MCM size. Second, use of through-the-substrate cooling usually means that only edge connectors can be used to the next level of packaging, potentially reducing connection capacity. Third, even with the use of thermal vias, the heat density might be too high for the desired cooling mechanism. It is then necessary either to reduce heat density by forcing the chips further apart or to consider a more aggressive cooling approach.

When individually packaged, high power chips generally must be housed in ceramic or metal packages, or in plastic packages with direct ceramic or metal heat paths to the heatsink. The thermal tradeoffs between single chip and multichip packaging can not be easily summarized. While heat density is higher in the latter, one (larger) heatsink can be shared by multiple chips. The advantages of the multichip packaging relative to single chip packaging depends on the details.

3.4.7 Performance Tradeoffs

A number of performance to performance tradeoffs have been identified above. Increased interconnection density is the main driver to increased system

performance. Increased density allows the chips to be spaced closer together, thus decreasing size, weight and delay. It also allows more chips to be placed in the same area, avoiding the bottleneck posed by the board to backplane connectors. The increased density offered by MCMs primarily benefits systems containing chips with hundreds of I/Os. It is erroneous to think that the main advantage of MCMs is only that they eliminate single chip packages. Repackaging a system with high I/O count chips as bare die on the same PWB results only in a small size reduction due to interconnection density considerations.

Sometimes it is necessary to sacrifice wiring density to satisfy thermal requirements if thermal vias become necessary. This should be weighed against the alternatives of using backside cooling or spreading the chips apart.

3.5 PACKAGING COST FACTORS

In this section, the different factors that contribute to system cost are described and explained. Details about how to model cost are provided in Chapter 4. In this section the intent is to explore their relationship to system level decision making by describing some of the more important cost performance tradeoffs. It must be noted that the unpackaged chip costs also must be included in the production cost. For any one board or module, the chip costs often exceeds the package cost if large, leading edge chips are used. The opposite is true if simple chips are used. When a multiple board system is considered, total packaging cost often exceeds total chip cost (see Chapter 18).

3.5.1 Production Cost

Production cost is the cost involved in getting the product out the factory door to the purchaser. It has two elements, manufacturing cost and the manufacturability cost.

Manufacturing Cost

The manufacturing cost is the cost of materials and process steps associated with the production of each part in the system and their assembly. This includes the chips, packages, connectors, heat removal mechanisms, power distribution features and the final packaging (casing, etc.). It includes the recurrent engineering (RE) cost elements (a cost that recurs for every part made) such as the purchase of the required materials and the labor and energy required to produce each part. It also includes the cost of purchasing the manufacturing equipment, a nonrecurrent engineering (NRE) cost element (a cost that is spread over a number of parts). A technical cost model for these elements is described in Chapter 4.

Table 3-2 Manufacturing Costs for Packaging and Interconnection Elements.

PACKAGE TYPE	TYPICAL COST
Plastic package	5¢ - $5.00
Ceramic PGA < 144 pins	$5,000 NRE + 10¢ per pin ($14 or more for 144 pins)
Ceramic PGA > 144 pins	$25,000 NRE = 10¢ per pin ($50 or more for 500 pins)
Cofired ceramic MCM	$3 per sq. inch per layer ($30 per sq. inch for 10 layers)
Thin film MCM	$60 per sq. inch (expected to decrease to ~ $20)
Laminate MCM	$3 - $5 per sq. inch
PWB	< $1 per sq. inch
CMOS chip wafers	$25 - $150 per sq. inch

High volume production allows the cost of purchasing the manufacturing equipment to be distributed over a greater sales volume, minimizing the NRE cost apportioned to each part. The required manufacturing and assembly steps should be as simple as possible and should lend themselves to automation through the use of standard looking parts. For example, the fact that small MCMs often can be mounted in conventional packages (QFPs, PGAs, etc.) gives them an additional cost advantage over large MCMs that tend to require custom packages unusable by standard automatic assembly equipment [5].

Typical vendor prices for some lower level interconnect structures are listed in Table 3-2. It can be seen that high pin count PGAs, high layer count ceramic MCMs and thin film MCMs command a substantial price premium over plastic packages, PWBs and laminate MCMs. Not shown are the cost of connectors. High pin count connectors tend to be costly (see Chapter 18). The higher cost of using high density MCMs at the lower levels of the packaging hierarchy might be compensated for if the need for high pin count connectors at higher levels of the hierarchy were reduced.

Manufacturability Cost

Not all of the parts manufactured function correctly. Parts must be tested, repaired if possible, and retested after repair. The cost of test and repair and the impact of failures is referred to herein as manufacturability cost because they depend, in part, on how well the part was designed for manufacturability.

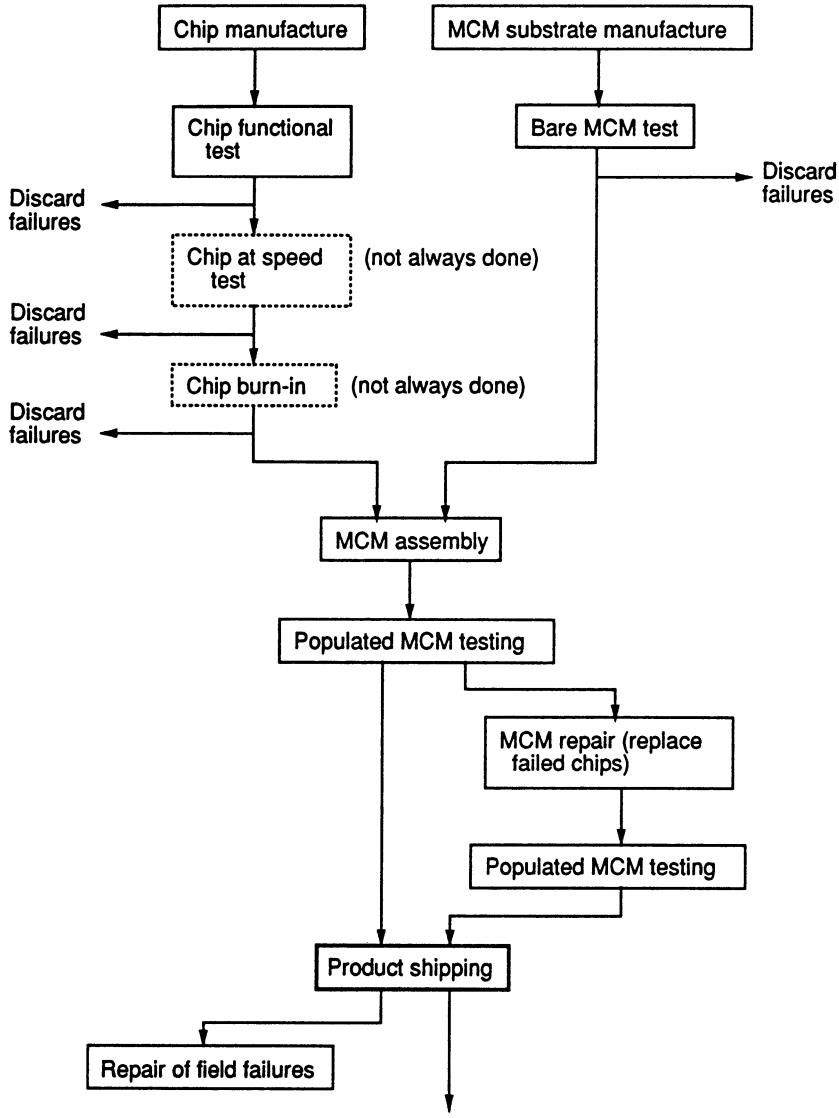

Figure 3-15 A simplified view of the MCM manufacturing process.

Assuming that this test and repair step is done only once in the manufacturing process (as shown in Figure 3-15), the final unit cost becomes:

$$\begin{aligned}\text{Final unit cost} = (&\text{Manufacturing cost per part} + \text{Test cost per part} + \\ &(1 - \text{Initial yield}) \times (\text{Repair cost per part} + \\ &\text{Cost of retest per part})) / \text{Final yield}\end{aligned}$$

where each cost component is averaged over all parts, good, bad or repaired.

Yield is defined as that percentage of parts that pass a test phase. Final yield is greater than initial yield if some of the failed parts can be repaired. For a chip, MCM or PWB, yield decreases with size. Thus, the cost premium of increasing a part size by a factor of two might be factor of eight if doubling the size doubles the manufacturing cost and quarters the yield. However, the greater effective interconnection capacity of the larger MCM often compensates for the poorer yield.

For example, consider die yield. The number of dies (chips) manufactured per wafer is given by:

$$\text{dies per wafer} \approx \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}} - \#\text{ die sites used for process control} \tag{3-13}$$

and the die yield is given by:

$$\text{die yield} = \text{wafer yield} \frac{1}{(1 + \text{defect density} \times \text{die area}/\alpha)^{\alpha}} \tag{3-14}$$

where wafer yield is the percentage of wafers not containing a gross fault affecting every chip on them, and α is the defect clustering parameter, which tends to take on a value between 1 and 3 [6]. The defect density might run anywhere between 0.5 - 2 per cm^2. Defect density improves with process maturity. For a fixed wafer manufacturing cost (typically \$500 to \$2000), the die cost increases rapidly with chip area. If a large complex chip has a yield of only 10%, then its final cost is at least ten times its manufacturing cost. This is one reason why large chips are not always the best alternative to a small MCM. The presence of defects effectively limits the maximum size of chip that is manufacturable without some method of tolerating the faults produced. As chips usually cannot be repaired, initial yield and final yield are the same.

Testing and rework costs have been identified as critical MCM related cost issues. Many sources attribute one-quarter to one-half the cost of the final MCM to these subcosts. In the normal manufacturing flow (Figure 3-15) individual parts are tested before assembly and the assembled MCM also is tested. If the assembled board fails, then it is necessary to either scrap the board or rework it, that is find and replace the part that failed. Since most MCMs contain at least one high value chip reworking usually is preferred. However, the cost of reworking an MCM is generally high. The best way to minimize rework is to ensure that chips are fully tested before being mounted on the MCM. Currently, this requires that the die be TAB mounted for reasons explained below. TAB mounting itself is expensive and also consumes area on the MCM.

Thus a balance must be struck that optimizes the combined cost of test and the likelihood of rework. This balance is determined by the minimum of the total out the door cost. A simplified expression for this cost (based on the manufacturing process in Figure 3-15) is:

$$\text{Final cost} = \frac{\text{MC} + \text{TC} + (\text{P(TE)} + \text{P(AF)}) \times (\text{RC} + \text{ATC})}{\text{Final yield}} \quad (3\text{-}15)$$

where MC is the total IC and MCM manufacturing cost, TC is the total IC and bare and populated MCM test cost, P(TE) is the test escape probability, P(AF) is the probability of an assembly fault, RC is the rework cost and ATC is the cost of retesting the assembled substrate.

Test escape refers to an IC that passes its initial test but fails after assembly. This is a potentially significant problem for MCMs. The hardware used to probe the very small chip pads uses long non-controlled impedance leads, making it difficult to pass noise free, fast edge signals to the chip. Good design for test techniques, as discussed in Chapter 13, are needed. At the moment, the easiest way to test a chip at full speed is to mount it first in a package such as a PGA, QFP or TAB. If the chip is not tested at full speed, the test escape probability can be as high as 30% if the IC is a leading edge CMOS chip, but also can be very small if the IC is from a mature line. It also is higher for CMOS parts than for bipolar parts. This is discussed further in Chapters 13 and 18. Depending on the details of this combined cost, there are a number of options that can be considered:

- If the MCM contains no high value parts or has only one high value part likely to fail, then there is no need to fully test the ICs before assembly since the MCM can be scrapped at little expense, if it fails.

- If the MCM has only one high value part, that part can be placed by itself on the MCM where it is easier to test than in bare die form. If the part passes, then the MCM assembly is complete. If the part fails, then the MCM can be scrapped or the single die replaced. This approach reduces the risk that other parts are damaged during rework.

- If the MCM contains a number of high value dies (chips) likely to have high test escape probabilities, then full consideration should be given to properly testing the dies before assembly, perhaps by using TAB chip attach and testing the tape form.

- Sometimes parts can only be tested properly after assembly. For example, a complex microprocessor may be easier to test completely when attached to its memories rather than as a single IC. In that case, the process should be optimized toward inexpensive and easy rework such as flip attach techniques.

3.5.2 Post Production Costs

Post production costs are incurred once the system is in use. They include maintenance, field upgrades and the repair and replacement of failed parts. The sum of production and post production costs is referred to often as the life cycle cost. The goal of a designer is to minimize life cycle cost, of which production cost might only be a fraction.

Reliability depends on the elimination of possible failure mechanisms and the operation of the parts at a sufficiently low temperature. This is discussed throughout the chapters in **Part B — The Basics.**

Repairability relates, in part, to the size of the field replaceable unit. For example, if an MCM is soldered onto a board, the field replaceable unit is the board. If the MCM is socketed, and the field diagnostics located the failed MCM, then the MCM is the field replaceable unit. If that MCM is sealed in epoxy, it must be scrapped. However, if the MCM has a resealable lid, it might be repairable and have further value as a used part. A life cycle cost analysis points at the correct solution (though MCMs are considered to be so reliable that repair is not usually needed).

The down time required to locate the fault and replace the unit also often is important. For example, in military systems, the ability of a system to survive a mission and to be quickly and easily checked and repaired are very important. If liquid cooling is used, then replacing a failed unit takes much longer than when air cooling is used. Also, the greater compactness of an MCM system might make fault location more difficult if the design is not carefully thought out. It is difficult to probe a signal on an MCM in the field.

Later chapters pay particular attention to reliability exposures that come about through the use of specific MCM technologies and reliability results from actual MCM use (see Chapter 17). Particular attention should be given to establishing a quality engineering process so that reliability can be maximized.

3.5.3 Design and Prototyping Costs

Design and prototyping costs include engineer training, engineer time spent in design, purchase of CAE and CAD tools to help in the design, construction and testing of the prototype, followed by design changes that arise from testing. Particularly for small to medium production runs, design and prototyping costs can be a significant part of the final system cost. The following should be considered when estimating the impact of this factor:

- The cost of building and diagnosing faults in an MCM prototype is higher than for a PWB prototype. (In the PWB prototyping, signal lines can be probed easily to test the prototype.) Extra emphasis needs to be placed on using a design approach that results in first pass success of the prototype. This requires extra investment in computer design tools and engineer training. Note, however, this investment is not that much different than the investment required for achieving first pass success for PWB designs operating at similar speeds and power dissipation. Consideration should also be given to using rapid prototyping technology [7].

- Effort should be spent on learning the technology. One technique is to go through the entire design and prototyping cycle with a non-production part. One reason that laminates are currently a popular form of MCM is because of their similarity to the already familiar PWB technology.

- Existing designs and hardware should be reused as much as possible and reasonable. This involves using off the shelf parts (if available and suitable), using programmable or semi-custom logic (if suitable) and reusing portions of existing designs, if applicable, rather than creating new designs. This is very important for low volume commercial parts.

- The decision making process described in this chapter requires that models be built, data obtained and evaluations conducted. This is a design activity. The investment required to carry out this activity

should be balanced against the likelihood that more detailed models, data, etc. lead to better decisions being made.

One possible impact of using existing designs is that, for low volume parts, it might be preferable to gain a performance improvement through repackaging a set of chips as an MCM, rather than redesigning them on one VLSI chip. (In any case, the one chip alternative is not a viable option if the chip set contains a mix of technologies.)

3.5.4 Time-to-Market

Reducing time-to-market often is more important than controlling design, prototype and production costs. One survey showed that being six months late to market resulted in an average 33% profit loss for that product, while a 9% production cost overrun resulted in a 21% loss, and a 50% design development cost overrun resulted in only a 3% profit loss. In a recent survey, engineering managers stated that they would rather have a 100% overrun in design and prototyping costs than be just three months late to market with a product. There are a number of reasons for this. If your competitors beat you to the market with a comparable product, they gain considerable market share and brand name recognition. This is difficult to quantify. One example is the stronger market presence of the Nintendo games over the other newer electronic games simply because it was introduced first. An earlier market entry has more opportunity to improve yield, thereby improving profits. Also, the technology is usually locked into place early in the design process. The design and production must be completed quickly from this point to prevent competitors from introducing a similar or more advanced product at the same time. Finally, design and prototyping costs are an up front investment that must produce a return. The longer investors must wait for their return, the higher that total return must be. (Who would you invest in? The company that could double your investment in two years or the one that would take one year?)

There are many reasons why time-to-market might be longer than necessary. One reason products might be late to market could be organizational, that is, excessive delay in making key decisions and an over reliance on complex design methods. Another possible reason is inexperience. Learning a new technology introduces delays into the design and manufacturing cycles. Remember that you are also inexperienced in pushing the older technology to new limits. It is very difficult to get a conventional 250 pin QFP to run reliably at 150 MHz.

Another potential reason for a long time-to-market, particularly critical for some MCM technologies right now, is the lack of infrastructure, as discussed in

Chapter 1. For example, you might need a source of tested, qualified solder bumped die and access to a high volume thin film MCM manufacturing line for success of your product. If both of these are difficult to obtain at the time of manufacture, product release must be delayed while you wait for their availability.

3.5.5 Cost Tradeoffs

The relative weight given to production cost, post production cost, design and prototyping cost and the impact of time-to-market depend on the details of the type of part being produced. For example, a part being produced in high volumes for use in applications where reliability is not critical, emphasizes production cost.

3.6 PACKAGING DECISIONS AND THE SYSTEM DESIGN PROCESS

During the system design process, the design engineering team needs to determine the organization of the system, the packaging hierarchy to be used, the packaging mixture to be used within each level of the hierarchy and the partitioning of the system functions between the chips and packages that comprise the system. The term "organization" means the block diagram for the system - what functional blocks make up the system and how they are connected. The term "packaging style" refers to the details of the package selected, including the type of package (QFP or thin film MCM), the size and layer count. It also includes the details of the connectors used between the packaging levels. The term "partitioning" refers to what functions are assigned to which chips and how the chips are assigned to different packages within the system. As part of the partitioning process, it might be necessary to determine a floor plan describing the approximate placement of components, chips or packages, with respect to each other.

Packaging and partitioning decisions are made by evaluating a set of alternatives. The performance and cost of each alternative is estimated and compared against the requirements and goals of the system. To do this, the requirements and goals of the system must be expressed in terms of the performance and cost factors described above and summarized in Table 3-3. If the performance and cost of each alternative is similarly expressed, then the alternative that best matches the goals of the system is the preferred option. This