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USEFUL ARTS IP
MICHAEL J. URE
10518 PHIL PLACE
CUPERTINO, CA 95014

EXAMINER	
JOY, JEREMY J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/26/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-12,17-22,26 and 35-99* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-12, 17-22, 26, and 35-99* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *07/17/2013, 10/18/2013, 10/18/2013, 10/18/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 09/26/2013, with respect to the rejections of the claims have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-12, 17-22, 26, and 35-89** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bertin et al.* (**U.S. Patent No. 5,202,754**, from hereinafter "*Bertin*") in view of *Kato et al.* (**U.S. Patent No. 4.939.568**, from hereinafter "*Kato*") in view of *Leedy* (**U.S. Patent No. 5,354,695**).

Regarding Claim 1, *Bertin* teaches a first circuit layer comprising a first substrate, a first surface having interconnect contacts, and a second surface opposite the first surface (Fig. 3, circuit layer 50, substrate 52, first/second surfaces 56/58 (not necessarily respectively), interconnect contacts 68/82) and a second circuit layer

comprising a second substrate and a first surface and a second surface each having interconnect contacts, wherein the second surface is opposite the first surface (Fig. 3, circuit layer 50, substrate 52, first/second surfaces 56/58 (not necessarily respectively); interconnect contacts 68/82); wherein at least one of the first and second circuit layers comprises a substrate thereof that is a substantially flexible semiconductor substrate made from a semiconductor wafer thinned by at least one of abrasion, etching and parting (Fig. 2, y to y' in which substrate is thinned to 5-20µm and thinning specifically shown in Fig. 3f-3g), and wherein the at least one of the first and second circuit layers comprising at least one vertical interconnect extending from a the first surface thereof to an the second surface thereof and formed within a via etched into the semiconductor substrate to accommodate the vertical interconnect, the vertical interconnect comprising a conductive center portion and an insulating portion surrounding the conductive center portion and adjoining sides of the via (Fig 3, vertical interconnects 66, insulated by silicon oxide), a third circuit layer comprising a third substrate and a first surface having interconnect contacts; and a plurality of bonds forming signal paths between the interconnect contacts of the surfaces of the second circuit layer and the interconnect contacts of the first surfaces of the first and third circuit layers (Fig. 3, third substrate not shown but the steps repeat as described; bonds are shown specifically in Fig. 3i between interconnect contacts 68/82; Col. 3-5).

Bertin fails to specifically teach the at least one of the first and second circuit layers is subsequently polished to form a polished surface after thinning.

Kato teaches using CMP to polish a surface to expose signal paths on a second surface (Fig. 4(g-i); substrate 1, conductive posts 4a/b; Col. 6, lines 5-16).

In view of the teachings of *Kato*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Bertin* above to include the polishing the surface using CMP because CMP is a well-known method to expose contacts on a substrate as it will provide a smooth flat surface for bonding as exemplified by *Kato*.

Bertin also fails to specifically teach wherein at least one of the first and second circuit layers is substantially flexible. In particular, since *Bertin* teaches forming the insulation portion of the vertical interconnects by thermal oxidation resulting in high stress insulation layer, it fails to teach flexible circuit layers (Note: the flexible circuit layer must possess a low stress dielectric in order for it to be flexible).

Leedy teaches an IC circuit structure comprising substantially flexible circuit layers wherein each of the circuit layers comprise an insulating low stress dielectric that insulates electrical elements and through-substrate conductors wherein said low stress dielectric layers are formed by an alternative dielectric deposition (Fig. 3 and 8, Col. 9, lines 15-49 and Col. 16, lines 38-56).

In view of the teachings of *Leedy*, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the teachings of *Bertin* to include that the insulating dielectric used in the IC structure and the circuit layers is a low stress dielectric layer (by using the formation technique of *Leedy* rather than *Bertin*) such that the circuit layers, including the flexible substrate, will then too be flexible circuit layers due to the inclusion of the low stress dielectric and the thinned semiconductor wafer because low stress dielectrics are desirable to form flexible circuit layers such that they may be able to withstand external stresses and furthermore still

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