stress. The stressed TiW films can flake from the walls of sputtering systems and produce particulates. Ni is another common diffusion barrier for Au, but it has only a moderate interaction with polyimide and thus, moderate adhesion. The most important advantage of Ni is that it can be electrolytically or electroless plated. Electroless plating is useful in protecting the sidewalls of Cu conductor lines from attack by polyamic acid.

Top Layer Metallization

The top metal layer in a TFML interconnection system serves a different function and has different requirements than the internal layers. It must be resistant to corrosion, strongly adherent to the dielectric and compatible with the assembly processes (wire bonding, soldering or die attachment). Au is used most commonly as a top layer metal because of its excellent corrosion resistance and its compatibility with die attachment and wire bonding processes. Au requires an adhesion/barrier metal between itself and the dielectric or underlying conductor. The most common interface metals for Au are Ni, Cr or TiW. Cr or TiW are sputtered, Ni is usually electroplated and Au may be sputtered, electroplated or electroless plated. For wire bonding or die attach, the Au is usually 1 - 3 μm thick. For soldering, excessive Au embrittles the solder, so a thin flash (less than 0.1 μm) of Au is used over the solderable metal, either Ni or Cu. For flip chip solder bonding, a metallization sequence such as sputtered Cr/Ni-Cu plated with Ni and Au [8] or Cr/Cu with a flash of Au [12] is used.

7.3.3 Dielectric Materials

There are many options for the dielectric material in a thin film interconnection system. The dielectric must have good thermal and chemical stability over the range of conditions encountered in thin film processing, assembly and end use. The CTE of the dielectric should be well matched to the substrate to minimize stress and warping of the substrate. Processes must be capable of depositing the dielectric in thicknesses up to 25 μm with low stress and no cracks or pinholes. Ideally the dielectric should smooth or planarize the large topography created by underlying conductor patterns. The most important electrical property for the dielectric material is a low relative dielectric constant (ε_r) as discussed in Section 7.2. The dielectric material also should have a reasonably low dissipation factor to avoid significant losses in the dielectric at high frequencies.

Polymer Dielectrics

High thermal stability polymers are the most frequently used dielectric materials for TFML interconnections, although silicon oxides have also been used.

Polymers are attractive in general because they have low dielectric constants and can be deposited from solution using spin or spray coating processes. Polymer dielectrics are discussed in detail in Chapter 8.

The most common polymer dielectrics are polyimides, a broad class of polymers characterized by aromatic groups and an imide ring in the repeat structure. Polyimides are deposited as a soluble precursor, usually polyamic acid, or as a soluble ester or acetylene terminated polyimide that is already imidized. The solution viscosity or coating parameters can be varied to achieve a wide range in film thickness. The polymer solution flows on the substrate, thus planarizing the conductor and via topography. Curing the solution at temperatures up to 450°C removes the solvents and converts the precursor to a stable, insoluble polyimide.

Fully-cured polyimide films are generally stable to 500°C, mechanically tough and flexible, and inert to process solvents and chemicals. Polyimides also have a low dielectric constant (2.0 - 3.5), a relatively low dissipation factor and high breakdown voltage. Polyimides that were developed first and are still widely used, such as PMDA-ODA and BTDA-based chemistries (refer to Chapter 8), have two significant drawbacks: (1) high moisture absorption resulting in a large variation in dielectric constant (30% variation in ε_r over the full range of relative humidity) [14], and (2) a large CTE (20 - 50 ppm/°C) that causes warping of low-CTE substrates (refer to Equation 5). To alleviate these short comings, low thermal expansion polyimides with a rigid backbone structure have been introduced [15]. The low CTE polyimides also have less moisture absorption, a lower dielectric constant (2.9 - 3.0) and higher tensile strength than the earlier polyimides.

A number of alternative polymers with certain advantages over polyimides also have been introduced. Polyphenylquinoxaline (PPQ) has a low dielectric constant (2.9), low moisture absorption, good mechanical properties and good adhesion. Polyquinolines have a low dielectric constant (2.6), very low moisture absorption, low stress when deposited on silicon, good planarization, long shelf life at room temperature and do not cause corrosion of Cu [16]. Polybenzocyclobutenes (PBCBs) have several desirable properties including excellent planarization, a low cure temperature (250°C), a low dielectric constant (2.7), low dissipation factor, low moisture absorption (0.3%) and good adhesion to Cu without metal adhesion layers. However, the PBCBs have a very high CTE (50 ppm/°C) and low elongation at break, and are susceptible to oxidation during curing or temperature aging. The oxidation problem has been solved by curing under a nitrogen atmosphere and adding an antioxidant to the formulation. Fluorinated poly(aryl ethers) have very low moisture absorption and an extremely stable dielectric constant (2.7) with temperature aging. The development of

specialty polymers for thin film interconnections will continue to be an active area for development as the MCM-D market grows.

Silicon Dioxide Dielectric

Silicon dioxide (SiO_2 is used as a dielectric medium by nCHIP, a company that manufactures "Silicon Circuit Boards" consisting of thin film interconnections on silicon substrates. The SiO_2 dielectric layers are deposited by a plasma chemical vapor deposition (CVD) process that produces films up to 20 μm thick under moderate compressive stress. nCHIP cites several advantages of the SiO_2 dielectric:

1. It requires fewer processing steps than polymer dielectrics.
2. The compressive stress in the film cancels the intrinsic tensile stress of metal films and produces a flat substrate.
3. SiO_2 has a reasonably high thermal conductivity (1.5 W/m°C, ten times greater than most polymers), eliminating the need for thermal vias to conduct heat through the interconnect layers.
4. SiO_2 does not have the high moisture absorption of polymers.
5. The dielectric is rugged, wire bondable and more reliable under thermal cycling, shock or nonhermetic environments.

Potential disadvantages of this dielectric are its slightly higher dielectric constant ($\varepsilon_r = 4.0$), its lack of planarization, susceptibility to pinholes and the slow deposition rates and high cost of the process gases, particularly silane. Although the CVD process requires fewer steps than polymer deposition and curing, it is unclear which dielectric will be more cost effective in a manufacturing environment. Additional vendors must offer SiO_2 dielectric and comparative studies of polymer dielectrics versus SiO_2 must be conducted before this dielectric will find widespread use in TFML interconnections.

7.4 THIN FILM MULTILAYER PROCESSING

TFML interconnections are fabricated using a repetitive sequence of unit processes for depositing and patterning conductor and dielectric layers. This section begins by describing the unit processes that are used most frequently. Then two basic approaches for patterning conductor features, additive and subtractive processing, are described and compared. Finally, some of the unique challenges imposed by TFML designs are discussed.

7.4.1 Conductor Deposition and Patterning Processes

Conductor Deposition

Conductor materials can be deposited by vacuum-based processes such as evaporation, sputtering, ion plating or by wet processes such as electrolytic or electroless plating. Several textbooks provide detailed descriptions of thin film deposition processes [17]-[18]. A recent paper compares the film properties (resistivity, stress, microstructure and adhesion) of Cu, Al and Au deposited by sputtering, evaporation, enhanced ion plating and electroplating [19]. The metal deposition processes that are used most frequently are described below.

Sputtering. Sputtering is a vacuum-based process in which the ions (usually Ar^+) in a plasma are accelerated toward a target material, ejecting or "sputtering" the target atoms by momentum transfer. The sputtered atoms deposit on surfaces exposed to the plasma, including substrates. The plasma can be sustained by either an RF or DC discharge. Magnets can be used to concentrate the plasma and enhance the sputtering rates without overheating the target. The substrate is heated by condensation, and both the target and substrate are heated by ion bombardment. The ability to cool the substrate or target can determine the maximum deposition rate.

Sputtering is the most widely used vacuum deposition process because it offers a number of advantages:

1. Almost any material can be deposited, including insulators, adhesion metals, thin film resistors (such as tantalum nitride or Ni-Cr) or the primary conductor.
2. Excellent adhesion to the substrate or dielectric material can be achieved by backsputtering or bombarding the surface with argon ions prior to depositing the metal.
3. Films can be deposited with excellent control of thickness, stress and morphology through variations of process parameters such as pressure, power and electrical bias of the substrates.
4. Sputtered thin films have low resistivity due to the high packing density of the atoms.
5. The films achieve conformal coverage of via holes and other topography.
6. Automated equipment is available for sputtering because of its widespread use in the IC industry.

The main drawbacks to sputtering are its relatively low throughput rate (because of slow deposition rates and limited batch size) and the high cost of equipment.

Evaporation. To deposit metals by evaporation, the metal is heated to a vapor using an electrical resistance heater or electron beam, and the vapor condenses on the substrates. Because the process is carried out at much lower pressures than sputtering (10^{-5} - 10^{-6} torr versus 10^{-2} - 10^{-3} torr for sputtering), the mean free path of the vaporized metal atoms is tens of meters, and deposition occurs only on surfaces that are directly exposed by "line of sight" to the deposition source. Therefore vertical surfaces such as via sidewalls are not coated as thickly as horizontal surfaces and overhanging surfaces can completely shadow underlying surfaces from deposition. The line of sight deposition can be used to advantage in liftoff processes (discussed later). In general, evaporated films have poorer adhesion than sputtered films because the atoms arrive at the substrate with lower energy. There also is less control of film stress and microstructure with evaporated films, since there is no controllable substrate bias to affect ion bombardment of the growing film.

Alternative Vacuum Deposition Processes. A variety of alternative vacuum deposition processes may be considered for thin film interconnections. Examples are ion cluster evaporation, ion plating (or enhanced ion plating), cathodic arc deposition, or ion beam sputtering. In ion cluster evaporation and ion plating, a thermally evaporated material is ionized and the metal ions are accelerated toward a biased substrate. These processes achieve good adhesion and packing density due to the high energy of arriving atoms. Film morphology and properties can be controlled by varying the evaporation rate and substrate bias. Cathodic arc deposition and ion beam sputtering are alternative processes for sputtering a target material. Cathodic arc deposition can achieve very high deposition rates. The primary limitation to all of these alternative processes is the relative lack of industry experience and automated equipment for high throughput processing.

Electroplating. Metals can be deposited from ions in a liquid solution by electroplating or electroless plating. Electroplating requires the application of an electrical potential to a metal seed layer on the substrate, while electroless plating can deposit metal through chemical reactions without an applied potential. Electroless plating is limited to thin coatings and therefore is useful mainly for interface or barrier metals. Electroless plating of Ni also has been used to fill vias [20].

For the thick conductor layers required in most TFML interconnections, electrolytic plating is used. Electroplating is well understood and widely used for top metal Ni/Au metallization. Electrolytic plating first requires deposition of a seed layer, usually by sputtering. An electrical contact is made to the seed layer and a current is applied. The substrate acts as the anode in an electrolytic cell and the metal ions are reduced and deposited on the substrate. The plated

metal can be deposited as a blanket coating or in open areas defined in a photoresist film (the additive approach described later).

The main advantage of electroplating is the high deposition rate, typically on the order of μm per minute. Therefore, electroplating, often is used for thick power/ground planes or thick signal lines (> 5 μm). A drawback of plating is the difficulty in controlling the process and film properties. The plating deposition rate, uniformity, film stress and morphology are dependent on a variety of process parameters, such as bath composition, temperature, agitation, electrode design and the plated area. The bath composition must be continually monitored and adjusted. Impurities in the plating bath can cause poor adhesion, defects or variation in the properties of plated films. In general, electroplated films have lower density and higher resistivity than vacuum deposited films. Finally, electroplating cannot deposit some metals and allloys that can be deposited by sputtering.

Conductor Patterning

Conductor layers can be patterned by either subtractive or additive processes, as discussed in Section 7.4.3. The unit processes discussed below are primarily used for subtractive patterning (etching) or direct writing of conductor patterns.

Wet Etching. Wet etching removes conductor material at a controlled rate by oxidizing the metal and converting it to a soluble product in an acid solution. It is the patterning process used most widely for TFML structures because it involves inexpensive equipment and can achieve high etch rates. The ideal etchant will selectively etch the desired metal without attacking the substrate or interface metals. The main limitation of wet etching is the resolution or aspect ratio achieved in conductor features. Because the chemical reactions proceed at an equal rate in all directions, wet etching undercuts the photoresist and produces a sloped sidewall. Figure 7-5 shows the undercut and sloped sidewall in a sputtered copper film 8 μm thick that has been spray etched. The undercut limits wet etching to aspect ratios below about 0.5, sufficient for most thin film interconnect designs.

Wet etching may be done by immersion or by spraying the etchant. Spray etching produces more vertical sidewalls and achieves better etch uniformity and higher etch rates by removing depleted reactants. Accurate control of linewidth requires a method for detecting the endpoint of etch. Bath parameters such as temperature, oxidation potential, pH and additives such as surfactants must also be controlled.

Dry Etching Dry vacuum processes for metal etching include ion beam etching, reactive ion beam etching (RIBE) and reactive ion etching (RIE). These techniques can produce much higher aspect ratios because the processes are activated by charged species accelerated perpendicularly to the metal surface.

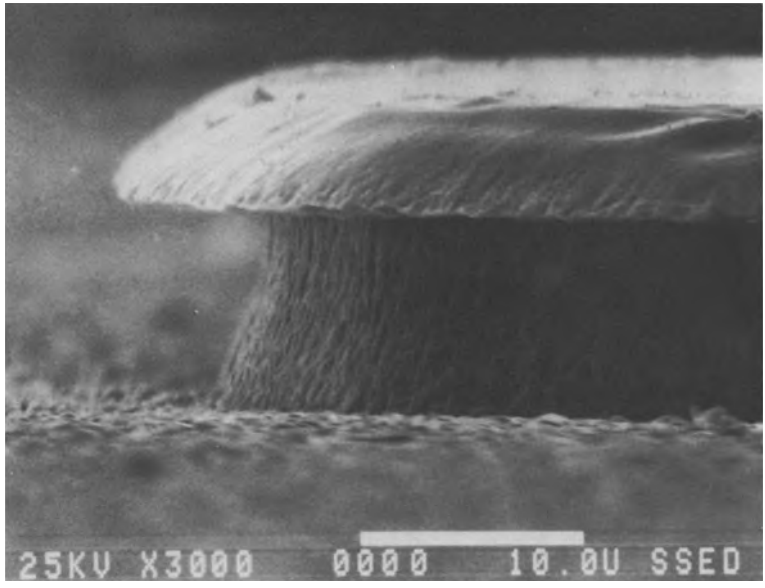

Figure 7-5 SEM micrograph of the sidewall in a spray etched copper film (8 μm thick), showing undercut beneath the photoresist.

Ion beam etching (or ion milling) uses a beam of inert gas ions (such as Ar^+) accelerated perpendicularly or at an angle to the substrate to dislodge metal atoms (as in sputtering). Ion milling can etch very high aspect ratio features in any material, however, it etches at a slow rate, has poor selectivity (many materials etch at similar rates) and causes heating of the substrate and photoresist. RIBE is a similar process, but uses a reactive gas to achieve higher rates or better selectivity. RIE uses a plasma, usually sustained by an rf discharge between parallel plates, as a source of reactive ions and neutral species that etch the conductor material. RIE achieves higher etch rates and better selectivity than ion milling or RIBE. RIE of Al is a widely practiced process in the IC industry, whereas the RIE of Cu requires high electrode temperatures to volatilize the reaction products, and is not a practical option at this time. The biggest drawback to all of the dry etch processes is the high cost of equipment.

Laser Patterning Some of the most promising alternative processes for patterning conductors are based on the use of lasers to write conductor lines directly. The two basic approaches for laser direct writing are: (1) using a laser to decompose liquid or gaseous organometallic compounds, and (2) decomposing catalytic metals such as palladium (Pd), followed by selective electroless plating of Cu or Au. The direct writing processes eliminate the need for masks or photolithographic processes and can be computer driven, but are limited in writing speed and thickness of the deposited conductor. Thus, they are most attractive for quick turnaround, low volume prototype fabrication, or for the local repair of conductor faults. Figure 7-6 shows links in a conductor pattern made by localized laser irradiation of a Cu formate film [21].

Lasers also can be used to etch conductor material, either by direct ablation in an inert atmosphere or by initiating reactions in a reactive gas or liquid. Laser ablation has been used for many years to trim thin film resistors. The main limitation to laser etching is the long time required to clear large areas. Thus,

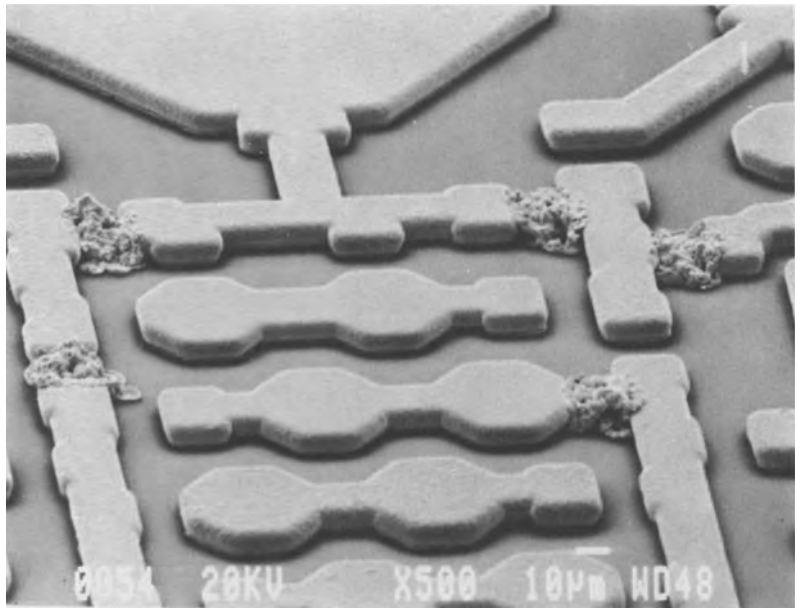

Figure 7-6 Links in a copper conductor pattern filled in by localized laser irradiation of copper formate solution. (Courtesy of R. Miracky, Microelectronics and Computer Technology Corp.)

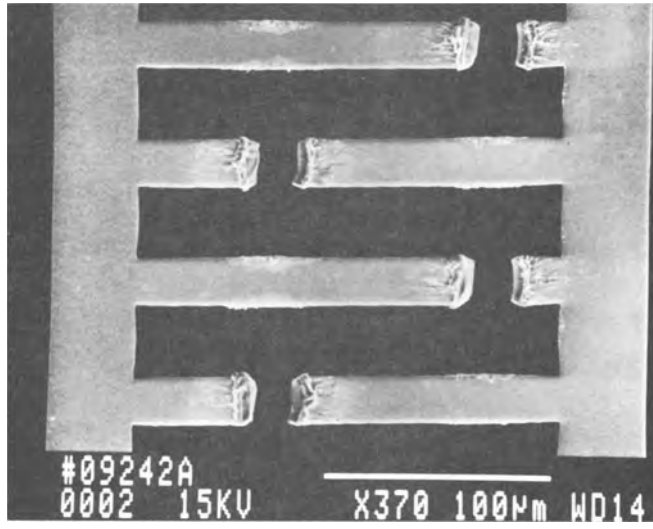

Figure 7-7 Openings in gold-nickel conductor lines (5 µm thick × 15 µm wide), cut by a frequency-doubled Nd:YAG laser. (Courtesy of R. Miracky, Microelectronics and Computer Technology Corp.)

laser etching processes are most useful for defect repair. Figure 7-7 shows Au-Ni conductor lines 5 µm thick × 15 µm wide on polyimide, cut by a frequency-doubled Nd:YAG laser [21]. Note the minimal damage to the polyimide.

7.4.2 Dielectric Deposition and Patterning Processes

Because the predominant dielectric materials are polymers deposited from solution, the following discussion focuses on polymer deposition and patterning processes, particularly those used for polyimide.

Polymer Deposition Processes

Polymer films can be deposited from solution by a variety of techniques including spin coating, spraying, dipping, screen printing, roll coating and extrusion. In all of these processes, the low viscosity of the deposited solution

allows it to flow and planarize underlying topography. The thickness, uniformity and planarization of the film depend on the viscosity and solids content of the solution. Surface tension in the coating causes edge bead, a build up of polymer near the edge of the substrate that can interfere with the patterning of features near the edge.

After deposition, the films are cured by heating at a controlled rate in an oven, hot plate or tube furnace to evaporate solvents and complete such reactions as the conversion of polyamic acid to polyimide. As the film cures, its viscosity increases until it is not able to flow; further volume reduction causes the film to partially conform to underlying topography. The final properties and adhesion of the polymer films depend on curing rate and final curing temperature, ranging from 250°C - 450°C. The atmosphere of the curing chamber is also important. In general, a nonoxidizing atmosphere is preferred to avoid oxidation of underlying conductor layers or the polymer itself.

Multiple coats may be used to achieve the layer thickness required for high impedance interconnections. The planarization improves with each coat. An important consideration in multiple coatings is the polymer-to-polymer adhesion. Good adhesion requires polymer interdiffusion at this interface. Interdiffusion depends on the degree of cure and the T_g of the underlying film. In general, a lower cure temperature or a lower T_g for the underlying film will improve polymer to polymer adhesion. Polymers that have poor self adhesion are sometimes treated with a plasma to roughen the surface prior to subsequent coatings.

An organosilane-based adhesion promoter is often used to improve the adhesion of the first polyimide coat to silicon or ceramic substrates [22], [23]. The adhesion promoter is applied as a very thin film, usually by spin coating. In recent years, polyimide formulations that are self priming or that contain adhesion promoters have become available.

Spin Coating. The most common process for depositing polymer films is spin coating. This well characterized process is used frequently for depositing photoresists in IC fabrication. Highly automated equipment, known as track systems, can load substrates from a cassette, dispense the polymer solution, spin the substrate at a controlled speed and acceleration, remove the edge bead by applying a solvent to the outer edge of the spinning substrate and perform an initial cure on hot plates. Adhesion promoters also can be applied on the track system. The film thickness can be controlled accurately by varying the spin speed and time and very uniform thicknesses can be obtained. The main drawback to spin coating is its relatively low throughput rate and difficulty in spin coating large, square substrates. Spin coating also wastes 90 - 95% of the dispensed polymer.

Spray Coating. An attractive alternative to spin coating is spray coating. In systems designed for microelectronics processing, substrates are loaded on a conveyor that moves beneath a reciprocating arm that dispenses the solution at a controlled rate through an atomizing nozzle. The thickness can be controlled accurately by varying the flow rate and the conveyor speed. The diluting solvent, solution viscosity, solution concentration, nozzle diameter and nozzle distance from the substrate are critical to the film uniformity. Spray coating is an ideal production process because of its high throughput capability and its ability to coat a wide range of film thicknesses on a wide range of substrate shapes and sizes, including large, square substrates. However, spray coating produces a larger edge bead and more local thickness variation than spin coating. Also, the process is sensitive to particulates, which can cause local dewetting and pinholes in sprayed films. The correct solvent and solution concentration will permit enough flow on the substrate to prevent pinholes, yet not enough to cause pooling and large thickness variation.

Extrusion. FAS Technologies recently introduced an extrusion process for coating polymer films [24]. The polymer solution is dispensed by a positive displacement, diaphragm driven pump with a master cylinder for filtering the solution at low pressure and a slave cylinder for accumulating and dispensing the solution. The metered solution is forced through a linear orifice in an extrusion head that is ~0.25 mm above the surface of the substrates that are moving beneath the head. This casts a polymer film across the full width of the substrate. The extrusion process can deposit films 1 - 100 μm thick with 2 - 5%, uniformity across the substrate and from substrate to substrate.

The extrusion process has several important advantages:

1. The large material waste of spinning or spraying is eliminated, since most of the polymer stays on the substrate.
2. Films can be deposited on large square substrates.
3. Edge bead can be eliminated and a clear zone can be left around the perimeter of the substrate.
4. A wide range of thicknesses can be deposited in a single pass.
5. High throughput can be achieved.

Possible concerns include the effect of substrate warpage on coating uniformity, and the effects of particulates, vias and topography on film defects. Further characterization of this process is required, but it has the potential for significantly reducing the material cost in high volume production.

Patterning of Polyimide Films

Polyimide films may be patterned by a variety of processes including wet or dry etching through a photolithographically defined mask, direct photopatterning of

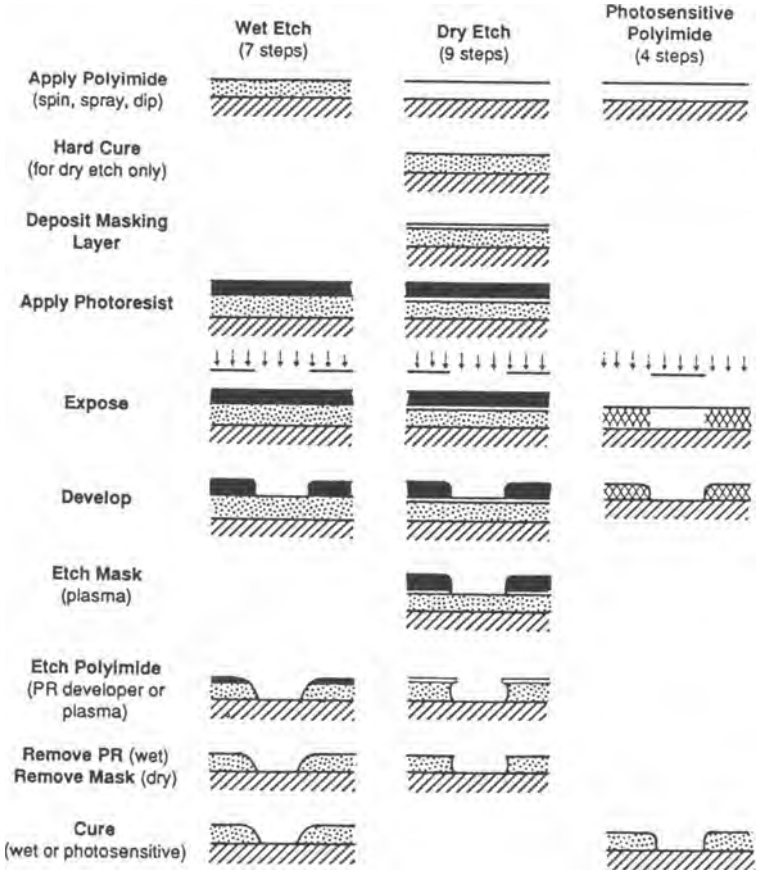

Figure 7-8 Process steps for patterning polyimide films by three different methods: wet etching, reactive ion etching and photopatterning of photosensitive polyimide.

photosensitive polyimides or laser ablation. The process steps involved in wet etching, dry etching and photopatterning are shown in Figure 7-8.

Wet Etching. Polyimide films can be wet etched by partially curing the film, patterning a photoresist coating, and dissolving the exposed polymer in an aqueous base solution. Many positive photoresist developers etch the partially cured polyimide, permitting development and wet etching in a single step. Wet etching is a simple and inexpensive process, but produces low aspect ratio features because of the isotropic etch. The etch rate and geometries are highly dependent on the extent of partial curing, which is difficult to control. After patterning, the film must be fully cured. This results in further shrinkage and loss of resolution. More importantly, residues left after etching can cause high via resistance. In spite of these problems, the economic incentives for a wet etch process are significant, and there has been considerable activity in developing polyimides or other polymers that can be wet etched. Polyimide formulations that are designed for a two step patterning process (separate photoresist developer and polyimide etchant) have recently been demonstrated to give steep sidewall angles and very smooth features. Figure 7-9 shows a 25 μm wide opening etched in a 10 μm thick film by such a two step process [25].

Dry Etching. Dry etching processes, such as plasma etching, RIE or RIBE, can produce much higher aspect ratio features in polymer films by using charged species in a plasma or ion beam to initiate etching in a direction perpendicular to the substrate surface. The most common dry etching process is RIE. Substrates are placed on the powered electrode sustaining an RF plasma in a gas mixture of oxygen and a fluorine containing gas such as CF_4, SF_6 or CHF_3. Because the polymer dielectrics etch at nearly the same rate as photoresists, the RIE of thick films requires that a masking layer of a slow etching material, such as a metal, silicon dioxide or spin-on glass, is deposited and patterned on top of the polymer. The full process sequence is shown in the middle column of Figure 7-8.

Dry etch processes can be used on fully cured polymer films and are less sensitive than wet etching to the specific chemistry of the polymer. Very low via resistance can be achieved, since the plasma etches any polymer residue at the bottom of vias (although metal oxidation or redeposition of materials from the RIE mask or chamber must be minimized). RIE processes can pattern high aspect ratio vias with nearly vertical sidewalls. More often, process parameters are varied to produce a controlled sidewall angle of 70 - 80 degrees from horizonal for better metal step coverage. Figure 7-10 shows a via etched by RIE in a 25 μm thick polyimide film, with a sidewall angle of 70 degrees. The main drawbacks to the dry etch processes are the high equipment cost and limited throughput rates.

Photosensitive Polyimide. The number of process steps required to pattern polyimide films is greatly reduced by using formulations that are photosensitive. The chemistry of photosensitive polyimides (PSPIs) is discussed in Chapter 8. Most PSPIs are negative acting so that areas exposed to ultraviolet (UV)

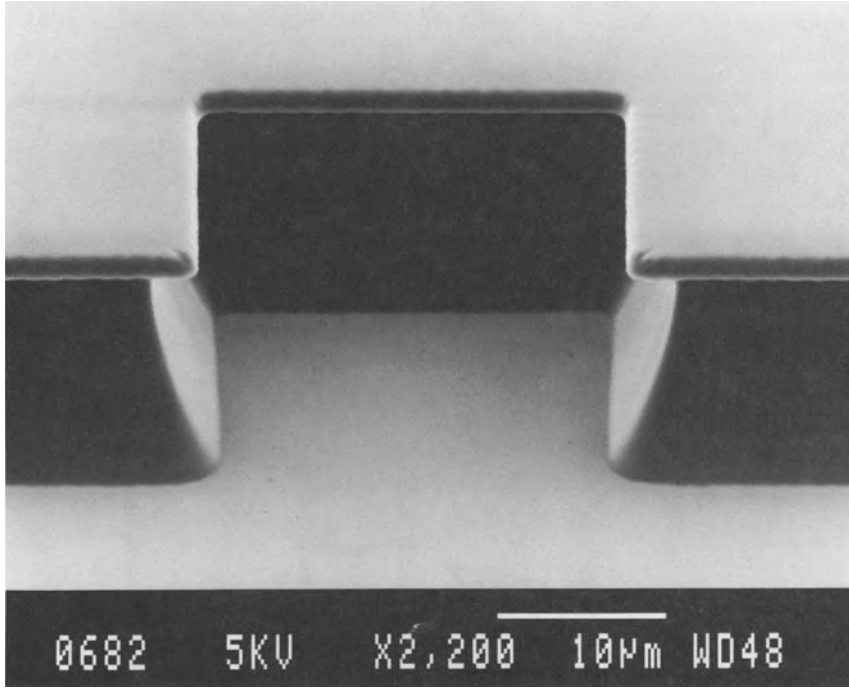

Figure 7-9 Ultradel 4212® polyimide patterned by spray etching with a specially formulated wet etchant. The coating will be 10 µm thick when fully cured, and the photoresist opening is 25 µm wide. (Courtesy of H. Neuhaus, Amoco Chemcial Company.)

radiation become cross linked and insoluble. The unexposed material is dissolved in a developer solution and the patterned film is cured to complete the imidization reactions and drive off solvents and crosslinking agents.

The photopatterning process involves considerably fewer steps, as shown in Figure 7-8 and eliminates the need for expensive plasma equipment. However, the resolution and aspect ratio of patterned features, particularly via holes, are limited by several factors:

1. Developer solutions cause swelling of the crosslinked polymer, which can cause a small opening to close or form webs,
2. There is considerable shrinkage during the final cure (typically 50% thickness loss), causing a loss in via aspect ratio, and

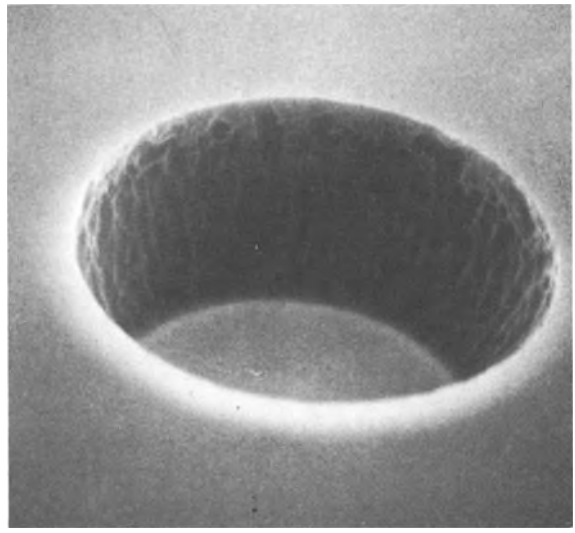

Figure 7-10 Via hole 25 μm in diameter etched in a polymide film 25 μm thick by reactive ion etching.

3. Polyimide and photoinitiators are highly absorbing at UV wavelengths, which limits the depth of crosslinking in the film.

During development, the uncrosslinked polymer beneath the crosslinked surface layer is dissolved, resulting in an undercut sidewall. This problem may be solved by filtering the highly absorbed wavelengths. Thick PSPI films also may be patterned by multiple coating and development of thin films. A final concern with PSPIs is the poor mechanical properties of the cured films, a result of their lower molecular weight. In spite of these shortcomings, the potential cost advantage offered by PSPI is so great that significant development efforts continue. Many Japanese companies manufacturing thin film interconnections are using PSPIs.

Laser Etching. A promising future technique for patterning polymer films is etching by laser ablation. Polyimides and other polymers can be thermally or photochemically decomposed by a variety of lasers and wavelengths, including CO_2, Nd-YAG, Ar^+ and excimer lasers. Pulsed excimer lasers operating at wavelengths of 193 - 351 nm have produced the best results with cleanly etched via holes and minimal thermal decomposition or residues. The mechanism is

believed to be a photochemical process in which chemical bonds in the polymer are broken and the products are explosively ejected. Because of the high absorption of UV radiation and the poor thermal conductivity of polyimides and the short pulse duration (typically 10 - 20 ns), the etched depth per pulse is about 0.1 - 0.5 μm with little thermal diffusion. Typical fluences for etching polymers are 100 - 600 J/cm^2, which is below the damage threshold for most metals (typically > 1 - 2 J/cm^2) [26]. Thus, metals are a good mask or etch stop for laser etching.

There are three methods for patterning polymers by laser ablation: (1) individual vias may be written directly with an aperture-controlled or focused beam that may be rastered, (2) complex patterns may be ablated by projecting a broad laser beam through a special lens and mask, or (3) a broad beam may be scanned over a contact mask deposited and patterned on the polymer. Direct writing of individual vias offers the advantages of maskless processing: direct computer control, short turnaround time, low tooling costs (no masks) and high yield. However, the writing speed for vias is limited to a few vias per second, which may not be an acceptable throughput rate for manufacturing TFML substrates with thousands of vias per layer.

A large number of vias can be etched simultaneously by depositing and patterning a masking material (such as Cu or Al) on the polymer and scanning a broad beam across the surface [26]. In this process, the laser essentially replaces a reactive ion etcher. Figure 7-11 shows a via etched in a 12 μm thick polyimide film by exposing a broad beam XeCl (308 nm) excimer laser through a deposited Al mask 2 μm thick. The mask is still on the polyimide. Note the lack of undercut that typically occurs in RIE of vias. Broad beam projection patterning through a special projection mask is very attractive if the optics and specialized masks can be developed. Projection patterning eliminates all of the process steps, equipment and yield defects associated with photolithography, mask deposition and polymer etching. Projection laser etching is used to pattern polyimide layers on the latest IBM Thermal Conduction Module (TCM) for the ES/9000 mainframe computers [27].

7.4.3 Basic Process Approaches: Additive and Subtractive

In PWB manufacturing, there are two basic approaches for patterning conductor features: additive and subtractive processing. In the additive approach, a negative image of the conductor pattern is defined in a photoresist film, and conductor is deposited in the open areas. In the subtractive approach, a blanket coating of conductor is deposited, a positive image of the conductor pattern is defined in photoresist and exposed metal is etched away. These process approaches are described in more detail and compared below.

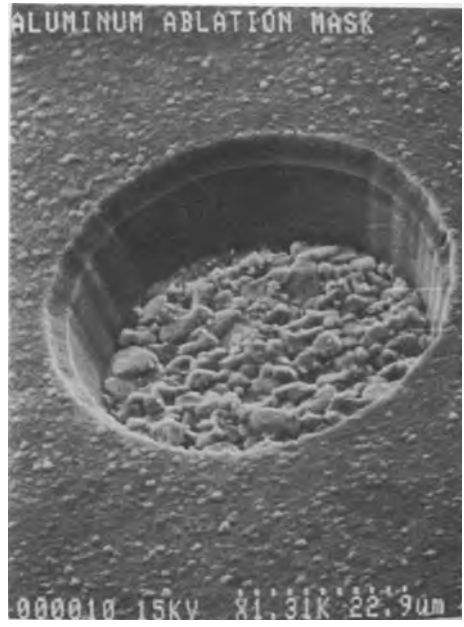

Figure 7-11 Via hole etched in a 12 μm thick polyimide film by broad beam laser ablation through a deposited aluminum mask 2 μm thick. The mask is still on the polyimide. (Courtesy of T. Tessier, Motorola Corporate Manufacturing Research Center.)

Additive Approach

The most common additive process, based on selective electroplating, is shown in Figure 7-12. First, a thin blanket coating of conductor (usually an adhesion metal followed by Cu) is deposited on the substrate to act as an electrical contact. A negative image of the conductor pattern is defined in a photoresist film thicker than the desired conductor thickness, and the conductor lines are electroplated in the open areas. The photoresist is stripped and another photoresist film is applied and patterned to define the via posts for interconnection between layers. The vias posts are electroplated and the photoresist and preplate layers are stripped. At this point, the exposed Cu may be coated with an electroless Ni to prevent interaction with the dielectric. Next, the dielectric (polyimide) is coated and the tops of the via posts are exposed by mechanical polishing [28] or by etching via holes in the dielectric (as in the DEC process, Chapter 17). The process sequence is repeated to build up additional layers.

An alternative additive process is based on liftoff of conductor material. A negative image of the conductor pattern is defined in photoresist and a blanket

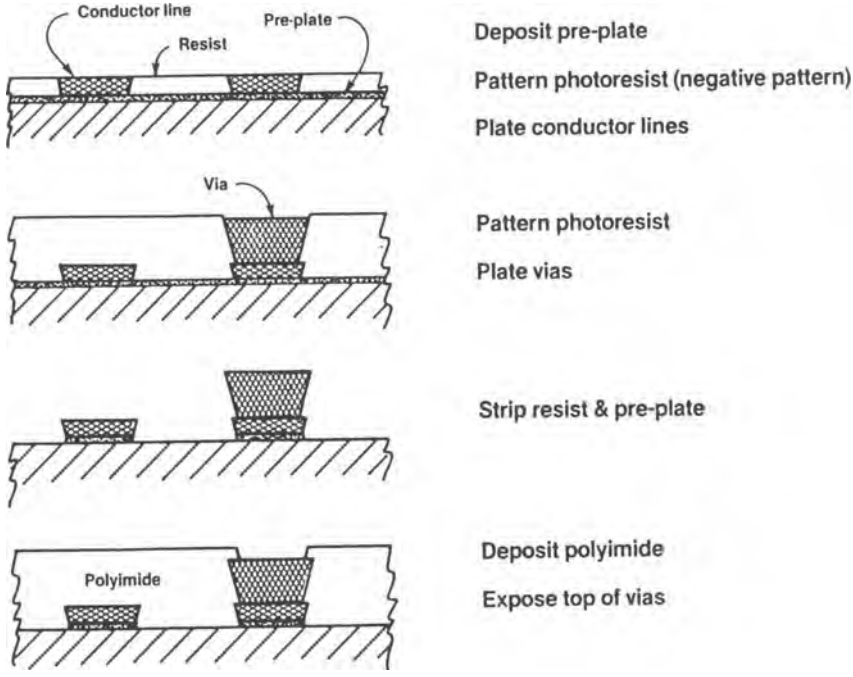

Figure 7-12 Simplified process sequence for patterning conductor lines and via posts by selective plating, an additive approach.

coating of conductor is deposited, usually by evaporation. By dissolving the photoresist, the metal deposited on top of the resist is removed and the patterned conductor is left behind. In an alternative liftoff process known as dielectric assisted liftoff, the dielectric is deposited first, followed by a soluble release layer, such as polysulfone, and a hard masking layer such as silicon nitride or oxide. All three layers are patterned (usually by RIE), leaving an overhanging ledge in the hard mask. The conductor is evaporated, and the release layer is dissolved to remove the conductor that is not in the etched areas. This leaves a self planarized conductor pattern.

Subtractive Approach

A simplified subtractive process is shown in Figure 7-13. The conductor is deposited as a blanket coating by a method such as sputtering, possibly followed

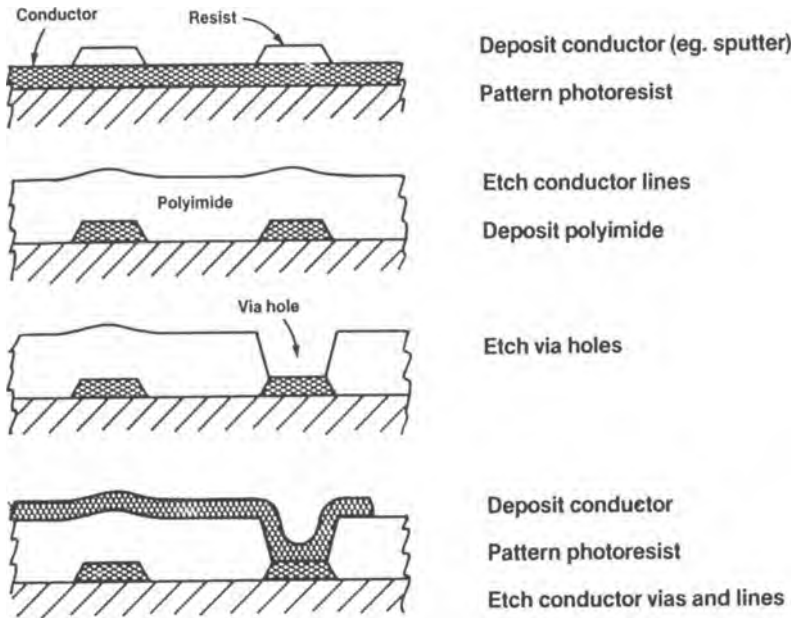

Figure 7-13 Simplified process sequence for patterning conductor lines and filling vias by subtractive patterning.

by electroplating to achieve the desired thickness. A positive image of the conductor pattern is defined in a photoresist film that may be thinner than the conductor film. The exposed conductor is removed by wet or dry etching and the photoresist film is stripped. The dielectric is coated in a blanket layer and an RIE mask may be deposited on the dielectric. A photoresist film is patterned with openings for vias. The vias are etched by a wet or dry process and the mask or resist is stripped. Another blanket layer of conductor is deposited with the conductor conformally coating the sidewalls of the via hole. The vias and next layer of conductor lines are then patterned in a single photolithography and etching step. This sequence is repeated for additional layers. An important difference from the additive approach is that vias cannot be vertically stacked, but must be staggered or staircased through multiple dielectric layers. The cross section in Figure 7-14 shows conformal staggered vias through three dielectric layers.

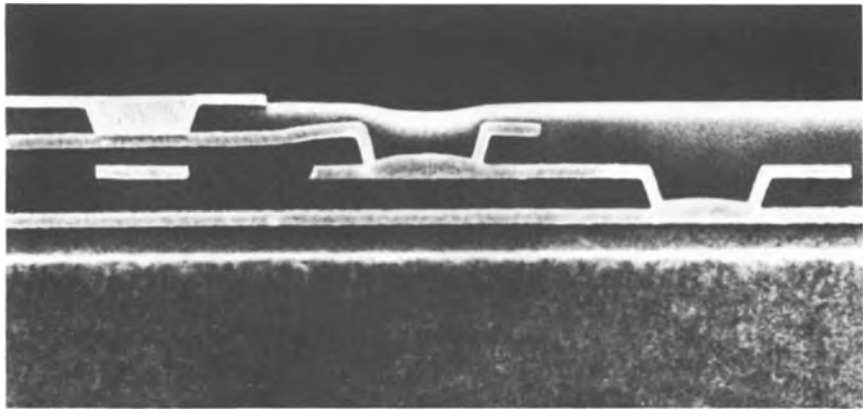

Figure 7-14 Cross section of a four metal layer TFML interconnection, with staircased vias through three dielectric layers. All metal layers are 5 μm thick. Notice the planarization of the via topography by the polyimide. (Courtesy Advanced Packaging Systems.)

Comparison of Additive and Subtractive Approaches

The additive approach has the advantage of being able to pattern very high aspect ratio features, because it is easier to define vertical wall features in photoresist than in etched metals. The additive approach can also form vertically stacked vias, leading to higher routing densities and possibly better heat transfer for thermal vias. However, there is some concern with stress and CTE mismatch in vertically stacked vias. The additional metal interface at the top of the via post (not present in the conformal via) may cause reliability problems or high via resistance. The mechanical polishing process that planarizes the dielectric down to the via posts is difficult to control. Etching to expose the vias involves additional process steps and equipment. Electroplating baths require tight controls (as discussed earlier) and plating rates and uniformity depend on the plated area and feature sizes. Finally, electroplating produces a higher resistivity conductor than sputtering or evaporation and cannot be used for Al interconnects.

The subtractive approach generally produces lower aspect ratios than selective plating because of undercut in the conductor etching process. The

routing density also is lower because of staggered vias that require more area. However, subtractive patterning has a number of advantages. It requires fewer processing steps than either selective plating or dielectric assisted liftoff. Any conductor material can be used, and there are more process options for patterning both the conductor and dielectric. In general, the subtractive approach is similar to the processes used for fabricating multilevel interconnections on ICs.

Most of the TFML processes reported in the literature have used subtractive approaches. Cu conductor layers are usually sputtered and then electroplated to the final thickness, while Al is sputtered. IBM uses a combination of subtractive etching and liftoff approaches for the TCM in the ES/9000 computer [27]. Several TFML substrate foundries are using selective plating approaches, including Alcoa (producing the Advanced VLSI Package (AVP) developed by AT&T) and DEC (see Chapter 17 for a process description). The most notable example of an additive approach with mechanically polished dielectric layers is the process developed by the Microelectronics and Computer Technology Corp. (MCC) [28].

7.4.4 Unique Process Requirements

The TFML processes employ many of the techniques and equipment used in IC fabrication. However, the substrates and geometries required for TFML interconnections present a number of unique challenges for conventional IC processing. The following section describes the unique process requirements imposed by the relatively thick films, high aspect ratio features and large substrates used for TFML interconnections.

Thick Film, High Aspect Ratio

Because of the requirement for low resistive losses and low interconnect capacitance, the conductor and dielectric layers must be relatively thick, on the order of 2 - 5 μm for conductor layers and 5 - 25 μm for dielectric layers. These thick films require long processing times, especially for dry (plasma-based) deposition and etching processes. Thick films also produce high strain energy that leads to substrate warping (Equation 7-5) and creates the potential for cracking or spontaneous delamination of films.

In order to achieve high interconnect density, conductor linewidths and dielectric vias must be closely spaced. The combination of small, lateral spacing and thick films means that features with high aspect ratios (thickness/width) must be patterned. In general, this requires anisotropic patterning processes, such as RIE, that etch faster vertically than horizontally. The high aspect ratio features create large topography as layers are built up, and this topography must be planarized for accurate photolithographic patterning.

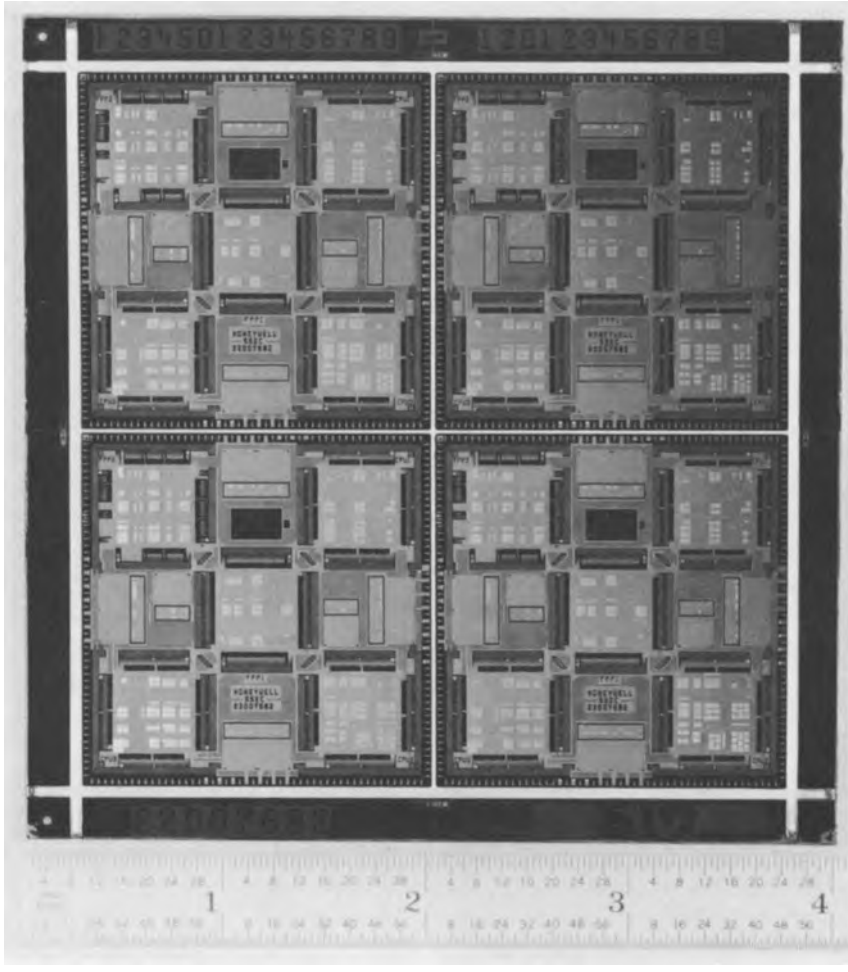

Figure 7-15 4" square TFML substrate containing four interconnection substrates separated by saw streets. The substrate is alumina with four metal layers of copper/polyimide interconnections. The individual substrates are assembled with chips and mounted in the package in Figure 7-16. (Courtesy of Honeywell Solid State Electronics Center.)

Large Substrates

MCMs and substrates vary greatly in size; MCMs up to 125 mm square are common and currently in production [8]. For smaller MCMs, it is usually most

cost effective to pattern several interconnection substrates on a larger starting substrate (the term "multiple up" is frequently used in the PWB industry to describe multiple circuits repeated on a substrate). Figure 7-15 shows four interconnection substrates patterned on a 4" × 4" × 0.050" thick ceramic substrate with four layers of TFML interconnections. The individual substrates (approximately 1.8" square) are separated by sawing, assembled with ICs and mounted into the MCM shown in Figure 7-16.

The large area and square shape of the substrate presents some unique challenges. First, the warpage induced by CTE mismatch increases linearly with substrate area or with the square of the substrate side length or diameter (Equation 7-5). Large substrates must be thicker to prevent this warpage; however, thick substrates increase the volume and weight of the MCM.

Choosing a square or round starting substrate depends on a number of factors. Round substrates in standard sizes of 100, 125, 150 or 200 mm are handled conveniently by automated wafer handling equipment. However, the final MCM is usually square or rectangular (as dictated by the shape of PWB or electronic chassis), and square starting substrates provide more efficient area utilization for single or multiple up substrates. Large square substrates are more difficult to handle with automated equipment designed for round wafers. It also is more difficult to spin coat polymers and remove the edge bead on square substrates. Some of the techniques and equipment developed for the fabrication of photomasks or flat panel displays are well adapted to the processing of large square MCM substrates.

Yield

The most significant impact of the large substrate area is its effect on process yield. This is illustrated by a simple yield model that assumes that defects are distributed randomly on a surface without clustering. (This is not usually observed in practice and is a worst case assumption.) The distribution of defects is described by a Poisson distribution. The yield, or probability of having no fault producing defects, is given by Equation 7-6:

$$Y = \exp (-A_c D) \tag{7-6}$$

where A_c is the critical area in which a defect will cause a fault and D is the area density of defects larger than a critical size. For particles in the size range of interest, D is inversely proportional to the square of particle size. If we also assume that the critical area A_c is proportional to the total substrate area $A = L^2$,

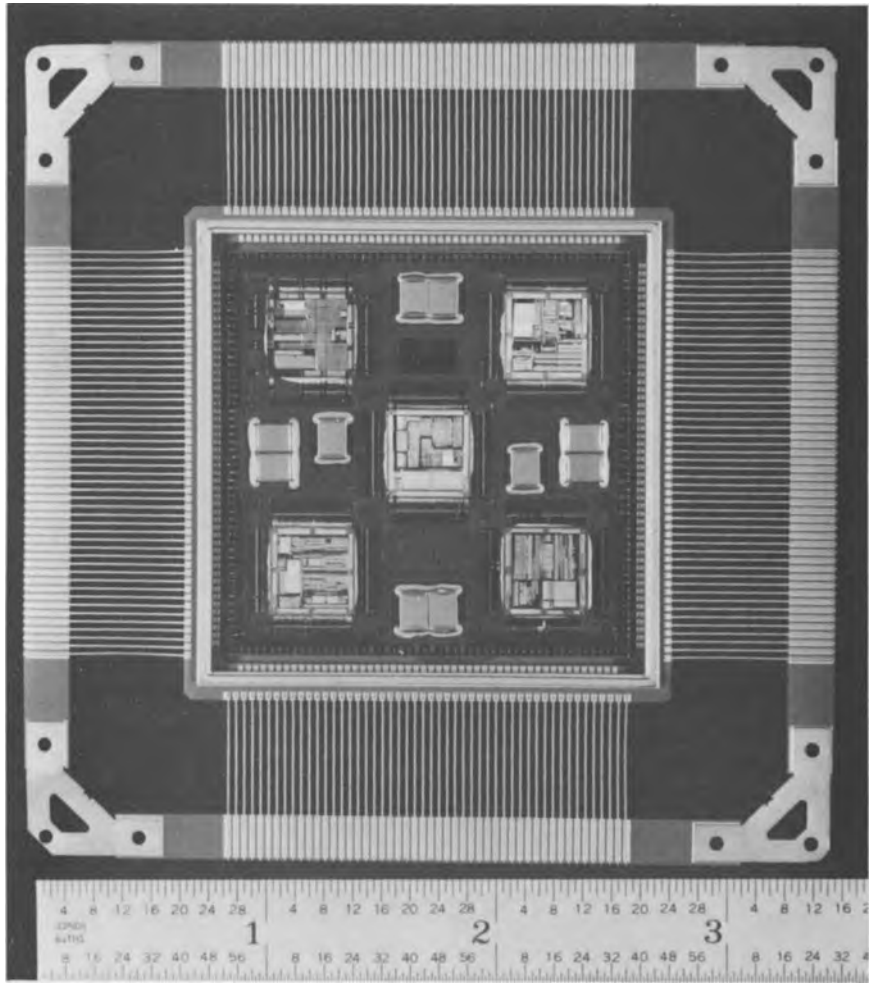

Figure 7-16 Multichip module for a radiation hardened 1750A computer (Generic VHSIC Spaceborne Computer), containing five chips on a TFML substrate in a 2.1" square cofired ceramic package with 200 leads. (Courtesy of Honeywell Solid State Electronics Center.)

where L is the side length of a square substrate, then:

$$Y = \exp\left[-k\,(L/x_c)^2\right] \tag{7-7}$$

where x_c is the minimum critical defect size [29]. For faults in features such as conductor lines, x_c is some fraction (typically 50%) of the linewidth. Although critical features in thin film interconnection substrates are roughly an order of magnitude larger than IC feature sizes (10 μm versus 1 μm), the side length is also an order of magnitude larger (10 cm versus 1 cm) and the yield, as predicted by the proportionality L/x_c, is equivalent to IC process yields. As the substrate size, L, or total interconnect length increases, the predicted yield will decrease exponentially with L^2, as shown by Equation 7-7.

Another way of viewing the yield challenge is to consider that a silicon wafer with a number of critical defects will still yield some good die after testing and dicing, whereas a thin film interconnection substrate that is comparable in size to the wafer must have no critical defects to yield a functional product. Because of this severe yield constraint, many substrate designs incorporate features that permit repair of a limited number of interconnects after testing. Repair methods can involve wire bonding (Figure 7-3) or direct patterning of top surface conductor lines (Figures 7-6, 7-7) [21].

7.5 DESIGN STRATEGIES FOR THIN FILM INTERCONNECTIONS

The following section discusses general strategies for achieving efficient MCM designs using TFML technology. Then it describes several implementations of TFML technology, with examples of MCM-Ds offered by various companies.

7.5.1. General Design Strategies

The design of an MCM is dictated by system requirements and the IC technology balanced against the capabilities of the interconnection technology. The total number of chips in an MCM is determined by system partitioning. It is usually desirable to capture a function within the MCM in order to reduce the number of off package connections. Once the number of chips is determined, the maximum packing density of chips within the MCM (and the MCM size) is determined by one of the following limiting factors:

1. The footprints of the chips and other components
2. The number and density of off package connections
3. The interconnect routing density
4. The thermal density

It is important to recognize the limiting factor so that technology advancements can be directed toward that factor. For example, in an MCM containing memory die, the packing density is probably limited by the component footprints rather than the interconnection density, and the emphasis in design and technology selection should be placed on fine pitch bonding or three dimensional packaging rather than on high routing density. For an MCM with microprocessor chips, the routing density or the off package connections probably determines the minimum package size.

The TFML technology offers reduced component footprints as well as high routing density. For wire bonding or tape automated bonding, it is desirable for the substrate to match the bond pad pitch on the IC, which can be as small as 100 μm in current technology. This is not difficult for thin film patterning processes, whereas MCM-C technologies normally require a double row of bond pads to achieve this density. For even higher packing density, flip chip bonding is desirable. The thin film system is well suited for flip chip bonding because it can be processed on a CTE matched substrate (such as Si or AlN) and can meet the flatness and density requirements for flip chip bonding. Another way to achieve high chip packing density is to pattern the interconnection over the face of the die, as is the High Density Interconnect (HDI) overlay approach discussed in the next section.

The routing density of TFML interconnections is limited by either the linewidth and spacing or, more often, by the via pitch. Photolithographic capabilities and yield place a lower limit on feature sizes. In general, linewidths and via diameters can be reduced by decreasing the conductor and dielectric thickness. However, this increases the interconnect resistance and capacitance, and thereby reduces the high speed performance of the interconnections. Thus the design of TFML interconnections is determined by a tradeoff between large conductor cross sections for high speed performance and fine lines/thin layers for high interconnect density. Electrical simulation of interconnects is important for performing this tradeoff.

There are several ways of improving the thermal performance of a thin film interconnection system. Since polymer dielectrics are poor thermal conductors, there is a high thermal impedance through the interconnect layers. The specific thermal impedance for vertical conduction through 40 μm of polyimide with no spreading would be approximately 2.5°C cm^2/W. The most common method for reducing thermal impedance is to pattern a dense array of metallized vias through

all the dielectric layers beneath the chip attach pads (Figure 7-3; thermal vias can also be seen on the die attach sites of the substrate in Figure 7-15). It has been shown that Cu vias 35 μm in diameter on a 100 μm triangular pitch can reduce the thermal impedance through four 10 μm thick polyimide layers to less than 2.6°C/W for the heat generated by a 0.5 cm square chip (specific thermal impedance of 0.1°C cm^2/W) [30]. The thermal vias permit partial routing through the via array beneath the chips. For even lower thermal impedance, an opening can be patterned through the interconnection layers, placing the chip in direct contact with the substrate. However, this greatly reduces the area available for interconnection routing.

The optimum way to achieve efficient heat removal plus high interconnect density is to have the interconnections on the active side of the chips and heat removal from the backside. This is achieved in flip chip bonding; however, compliant materials (such as conductive pastes or solders) or special designs (such as the IBM Thermal Conduction Module or liquid immersion cooling) are required to remove heat from the backside of the chips [31]. Another alternative is the HDI approach, which places the chips in direct contact with the substrate and fabricates the interconnection on an overlay laminated to the face of the chips (discussed more in the next section). In this technology, the thermal density is limited by the ability to remove heat from the substrate, rather than from the ICs.

7.5.2 Implementations of Thin Film Interconnections

Thin Film Substrate in a Package

There are many ways to incorporate TFML interconnections into high density packaging structures, as shown in Figure 7-1. The most widely used approach is to fabricate TFML interconnections on a substrate that is populated with chips and mounted into a second level package, similar to bonding a chip into a single chip package. This permits the use of a wide variety of substrate and package materials. The multichip substrate can be procured as a component by a hybrid or IC packaging facility that manufactures MCMs. Thin film interconnection substrates have been available (albeit in small quantities) from a number of vendors, including Alcoa (shown in Table 7-1), nChip, Polycon and Advanced Packaging Systems.

Options for the second level package include metal flatpacks with glass insulated leads, cofired ceramic packages of Al_2O_3 or AlN [32], and plastic packages. The metal and ceramic packages can be hermetically sealed after thoroughly baking out the polymer dielectric material. For this reason, they are the most widely used package for military qualified MCM-Ds. Figure 7-16 shows an MCM-D for a radiation hardened MIL-STD-1750A computer

(Honeywell's Generic VHSIC Spaceborne Computer) containing five chips on a TFML substrate in a 2.1" square cofired ceramic package with 200 leads. The substrate (shown in Figure 7-15) has four metal layers and 1400 cm of interconnect wiring. There are 1100 gold wire bonds between the chips and substrate and 200 wire bonds between the substrate and package. In an earlier design, the same substrate was mounted in a Kovar flat pack with glass feedthrough leads [33]. A complementary memory module with nine radiation hardened 8k × 8 SRAM memory die and a memory line driver chip in a 2.6" × 1.6" cofired ceramic package is shown in Section 9.3. An IEEE task force has recently developed a recommendation to JEDEC for a series of standard package sizes for MCM-D substrates. This will reduce the tooling expense for packages and permit standardization of testing and handling fixtures.

Plastic packaging may be done in two ways: (1) the assembled multichip substrate is soldered to a premolded plastic leadframe, an encapsulant is applied for mechanical and environmental protection and a cover and optional heat sink is attached, or (2) the multichip substrate is soldered to a leadframe and then molded into an epoxy-based material. The most significant implementation of plastic packaged MCM-D is AT&T's Polyhic technology [34]. They are producing several standard sizes of plastic leaded chip carriers, quad flat packs and dual in line packages containing MCM-D substrates.

TFML on MCM-C

Patterning the TFML interconnections directly on a package base such as cofired ceramic eliminates the substrate to package bonds, a drawback of the first approach. Power and ground distribution layers can also be incorporated into the substrate. This approach has been termed MCM-D/C, for MCM-D on ceramic. MCM-D/C has been widely implemented in large mainframe computer systems. The outstanding examples are: the NEC SX series of supercomputers which use copper/polyimide interconnections on a multilayer Al_2O_3 cofired ceramic substrate as an interconnect for individually packaged flip TAB carriers [35], and latest version of the IBM thermal conduction module for the ES/9000 computer, which uses 63 layers of cofired glass-ceramic with Cu metallization to handle the signal interconnection and power/ground distribution and a thin film layer of Cu on polyimide for partial redistribution of the flip chip bonding pads to engineering change pads [8], [27]. Motorola, Honeywell and the Microelectronics Center of North Carolina have also reported on the development of this approach.

While the multilayer ceramic substrate is attractive because it serves as the package housing and second level interconnection, it presents a number of technical problems:

1. It is difficult to handle large, pinned substrates in IC process equipment.
2. Lapping and polishing are normally required to achieve a sufficiently flat and defect free surface for thin film patterning.
3. The thin film patterns must mate with the vias in the cofired ceramic, which have a large uncertainty in their location.
4. No seal rings can be brazed on the top surface, since a flat surface is required for photopatterning processes.
5. Substrates are expensive, and thus the TFML structures must have high yield or be reworkable.

The most likely users of MCM-D/C will continue to be vertically integrated manufacturers that control all aspects of MCM fabrication and assembly.

Chip-on-Board

In conventional chip-on-board packaging, unpackaged ICs are bonded directly to an interconnecting substrate (PWB or flexible tape) and protected with a glob top encapsulant. This approach has been used for a number of years in low cost, low density applications such as watches. Thin film interconnections offer the possibility of extending this approach to much higher levels of integration with higher interconnect density. A ceramic, metal or multilayer ceramic substrate equivalent in size to a PWB is patterned with TFML interconnections.

This approach is distinguished from conventional MCMs by the relatively large size of the substrate and the removal of sealing structures such as seal rings and lids. This requires a protective coating for the chips to prevent corrosion or mechanical damage. There has been active development of reliability without hermeticity in recent years and a number of promising coatings have been introduced, including glob top encapsulants [36] and vapor deposited coatings. The chip on substrate approach offers advantages in both cost and performance since it eliminates several components and assembly steps as well as the thermal and electrical impedance of additional packaging interfaces. However, it requires high confidence in functional die before assembly, and sophisticated testing methods are needed for the assembled board.

High Density Interconnect (HDI) Overlay Approach

Some thin film interconnection systems have unique features that fall outside the standard approaches discussed above. One such system is the General Electric high density interconnection (HDI) represented in Figure 7-17 [37]. In this approach, the chips are mounted in cavities in a substrate. A Kapton (polyimide) film is laminated to the face of the chips and a laser is used to etch vias holes for contact to the chip bonding pads. A TFML interconnect structure is built on

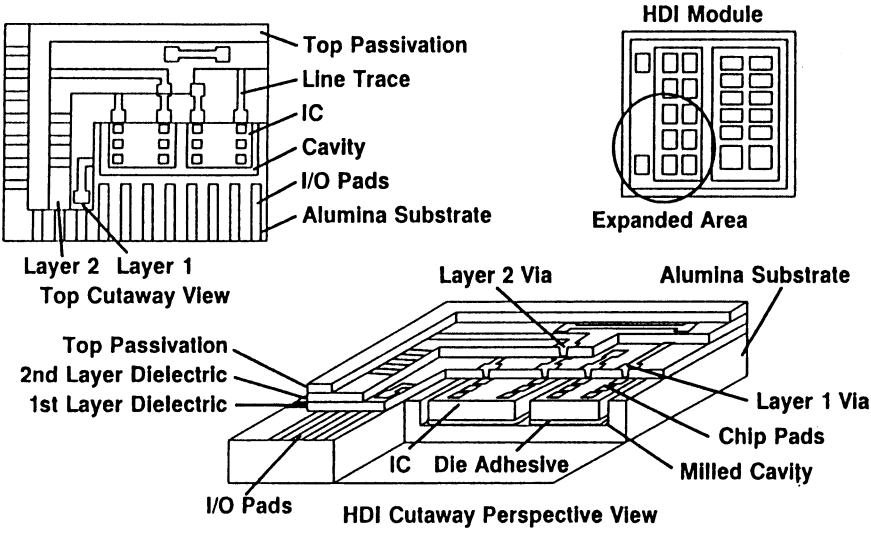

Figure 7-17 Representation of the General Electric High Density Interconnect overlay approach. (Courtesy of R. Fillion, GE.)

the Kapton overlay, using the laser to etch via holes in the polymer dielectric and to pattern the conductor photoresist. Cu conductor is deposited by sputtering and plating and patterned by wet etching. The completed substrate is mounted into a second level package.

The advantage of this approach is that die can be tightly packed, essentially side by side, and heat can be removed efficiently since the die are in direct contact with the substrate. High routing density can be achieved since no thermal vias are required through the interconnect layers. Chip bonding operations (such as wire bonding) are eliminated by the metallurgical via contact to the chips. Rework is the biggest concern with this approach. The overlay can be removed by heating and peeling, but removal of defective die requires a more complicated procedure. There is also a concern with the cost and throughput of the laser-based processes. Finally, there are limited sources for this type of interconnect.

DEC High Density Signal Carrier

A thin film interconnection system with several unique features is used by DEC in the High Density Signal Carrier (HDSC) for their VAX-9000 series of mainframe computers. In this technology, copper/polyimide thin film

interconnections are built on a temporary Al substrate and then detached, leaving a free standing film. One film contains four power distribution layers (the power core); the other contains two interconnect layers surrounded by reference planes, plus the top bonding layer (the signal core). These two cores are laminated together and the power core is electrically connected to the top surface by drilling and plating through holes as in PWB processing. Cutouts are excised for the chips, and the structure is laminated to a Cr-Cu substrate. This approach offers excellent power distribution and heat removal for very high power density ECL ICs. However, since the chips are in direct contact with the metal substrate, there is no wiring under the chips, limiting the interconnection density. The DEC technology is described in greater detail in Chapter 17.

MCC Quick Turnaround Interconnect

Another unique concept for using TFML interconnections is the quick turnaround interconnection (QTAI) proposed by MCC. The QTAI is designed to reduce the turnaround time and tooling costs of new interconnect designs. This is done using a generic substrate with power and ground distribution layers and reconfigurable interconnection layers consisting of short x- and y- segments with vias to the top surface (analogous to a gate array for IC design). The substrate can be personalized with one metal layer which connects the required segments to achieve the interconnections. The top layer also provides the chip bonding pads. The QTAI has been demonstrated in a crossbar switch containing 16 identical ICs (0.300" × 0.360" chips with 103 leads/chip) and 336 external connections, on a substrate approximately 2" square [38].

7.6 APPLICATIONS, GROWTH OF THIN FILM INTERCONNECTIONS

7.6.1 Interconnection Technology Selection

The thin film interconnection system offers many fundamental performance advantages, as discussed in Section 7.2, namely: high interconnection density, high speed signal transmission, low impedance power distribution and high bonding density. It also offers flexibility in terms of substrate materials, thermal designs and package implementation. However, the selection of an interconnection technology involves a number of additional considerations.

The interconnection technology must be compatible and robust for a variety of assembly processes. IC assembly operations have more experience with die attachment and bonding to ceramic substrates. In general, the harder ceramic surface permits the use of higher force, temperature, and energy in thermosonic

and ultrasonic wire bonding. The bonding and die attach pads on ceramic substrates are also more robust toward rework processes than thin film metallization on polymer dielectrics. Finally, there is less concern with absorbed moisture in hermetically sealed MCM-C packages. All of the assembly and sealing operations have been demonstrated for polymer-based TFML systems, but there is less experience and a smaller data base for the technology.

Because of the relative immaturity of TFML technology, there is less life cycle and field performance data compared to older technologies (although IBM, AT&T and DEC have generated extensive life cycle data internally). There is a general concern in the military community with the reliability of packages containing polymers. Some of these concerns arise from early failures attributed to impurities in epoxy die attach materials. In general, ceramic interconnect systems are considered more reliable at this time. More accelerated life cycle testing, failure analysis and field testing of TFML systems is required.

The most important barrier to the use of MCM-D is its high cost and limited availability. Initial applications have been in customized MCMs for large mainframe or supercomputers (as in the NEC, IBM and DEC examples discussed earlier) or in prototype military systems. None of these applications has generated the high volume of standardized modules and substrates necessary to reduce costs and provide a broad manufacturing base. Most of the high volume manufacturing facilities are for captive products. A vendor infrastructure has not developed for providing thin film substrates or assembled MCM-Ds as a component, as exists for single chip and multichip ceramic packages. The development of this infrastructure is the most important requirement for the widespread application of thin film interconnection systems.

7.6.2 Evolution of TFML Applications

Since thin film interconnections cannot compete with alternative interconnect technologies on a cost basis at this time, initial applications of the technology must be performance driven. Thin film interconnections must be required for small size and/or weight, as in space-based electronics, military avionics, or medical implants. Alternatively, TFML interconnects must be demanded by the requirements of fast clock speeds and high interconnect density, as in supercomputers, mainframes, or high speed digital processors using GaAs ICs.

The emergence of TFML technology in these specialized applications will be followed by higher volume products where size is still a discriminator, such as laptop or notebook computers, commercial avionics, or possibly telecommunications electronics. As the range of applications and production volumes increase, the required vendor infrastructure will develop, and costs will be driven down to make MCM-D competitive with MCM-C and MCM-L

technologies. At the same time, assembly experience and reliability data will grow, increasing confidence in the reliability of the technology. An unresolved issue is whether thin film substrates will be provided as a component by traditional package manufacturers (cofired ceramic vendors) or specialized thin film substrate foundries, or whether assembled MCM-Ds will be manufactured by captive systems houses, IC foundries, hybrid manufacturers or full service MCM foundries.

7.6.3 Future Applications

Thin film interconnection systems provide a technology base for even higher performance packaging technologies that are currently under development. Some examples are mentioned briefly:

1. Thin film interconnections are needed for hybrid wafer scale integration (HWSI), in which a wafer is tested and diced, and the good die are reconstructed into an array with essentially the same density as the original wafer. This approach requires flip chip bonding to a CTE matched substrate (possibly with active or passive devices, as discussed in Section 7.3), or an HDI-type of overlay interconnection. HWSI achieves the high circuit density of monolithic wafer scale integration, but avoids the need for redundant circuitry.

2. Stacking of die, especially memory ICs, is being developed to achieve very high volumetric density with additional interconnection in the vertical direction. Thin film interconnections are sometimes patterned on the face of these die cubes. TFML substrates are often used to interconnect the die stacks [39] because of the bonding density, flatness, and special metallization needed.

3. Integrated optical waveguides for chip-to-chip interconnections have been built using thin film structures with the same materials system as for electrical interconnects, using polyimides for the waveguide media [40]. This offers the possibility of a combination of optical and electrical interconnections in the same substrate.

4. Superconductors have been proposed for overcoming the speed/density limitations of traditional conductor materials [41]. Very thin, fine line superconductor interconnections will be lossless, as long as the temperature and current are below the critical values. This will permit almost unlimited interconnection density, lossless signal and power distribution and very thin multilayer structures.

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8

Selection Criteria for Multichip Module Dielectrics

Claudius Feger and Christine Feger

8.1 INTRODUCTION

In the last decade, polymeric dielectrics have been widely accepted as materials of choice for interlayer dielectrics in MCMs [1]-[2]. The driving forces for this development are:

1. The low dielectric constant, usually exhibited by organic polymers, allows higher packaging densities in comparison to ceramic packages that have a higher dielectric constant. Furthermore, a lower dielectric constant dielectric material leads to faster transmission speeds and to lower power consumption.

2. Polymers are relatively easy to process with procedures developed for semiconductor thin films and therefore are widely understood. Although the equipment and materials can be expensive in comparison to thick film technology, most companies already have the knowledge and some equipment in place and can start development work without a large investment in new technology.

3. Many interesting combinations of properties can be tailored by making changes in the chemical composition of these polymers. The search for

the ultimate dielectric polymer, coupled with the emergence of a lucrative market for such specialty polymers, has increased tremendously the number of chemical companies offering polymers to the electronics packaging industry. Thus engineers today have the luxury and responsibility to select from an ever increasing market offering the best material for their specific application.

To apply polymeric dielectrics in MCMs it is essential to have basic knowledge in two very different areas:

1. Polymer science including polymer chemistry, polymer physics, polymer processing and an understanding how these areas relate to the observed properties, and

2. MCM engineering including electrical design, electronics packaging technology and an understanding of both thin film and thick film processes.

Unfortunately, the two areas rarely are interrelated. Available literature either is directed exclusively to the polymer science community or exclusively to the engineering community. Too often this results in costly misunderstandings and a lack of needed cross-fertilization. This chapter tries to fill the gap in the literature, attempting to allow the reader schooled in electrical engineering to understand polymer material aspects and to assist the chemist or physicist unfamiliar with polymers and/or electronics packaging in their development efforts. This chapter describes the basic properties required of polymeric dielectrics in high performance computer MCMs, the chemistry and properties of the most common polymeric dielectrics under consideration today (polyimides, fluorocarbon polymers, polyphenylquinoxalines (PPQ) and benzocyclobutenes (BCB)) and relates processing requirements to material properties. The reader should become better equipped to use vendor material data sheets to make more informed material selections for a particular application. Before describing the process variables in MCM manufacturing, the behavior of dielectrics in an electric field and their function in a package will be considered.

8.2 BEHAVIOR AND FUNCTION OF DIELECTRICS

There are three reasons why good dielectric properties are important for electronics packaging: signal speed, power consumption and wiring density. In the following section, the response of a dielectric in an electric field is described,

explaining the dependence of signal speed, power consumption and wiring density on dielectric properties.

Dielectrics, materials that do not conduct electricity, are also called insulators. Exposure to a static electric field causes the electric charges present in any dielectric material as permanent electric dipoles and/or induced electric dipoles to be moved, polarizing the material. The equilibrium polarization remains a material constant for a given electrical field. However, it is the dielectric constant, ε, also symbolized by κ, that is used to characterize the dielectric properties of a dielectric, not the polarization. ε most commonly is defined as the ratio of capacitance in a capacitor filled with the dielectric material to capacitance of the identical capacitor filled with a vacuum. The magnitude of ε depends on the amount of mobile (polarizable) electrical charges and the degree of mobility of these charges in the material. Because the charge mobility depends on temperature, ε is temperature dependent. Time is required to establish the equilibrium polarization. Thus in a dynamic electric field the dielectric constant depends also on the frequency of the field change. In an AC field, the dielectric constant is complex (complex permittivity, ε^*) and has two components: the real component (ε') called the dielectric constant of the material[1], or the relative permittivity, and the imaginary component (ε'') called the loss component or the dielectric loss factor. Instead of ε'' the dielectric loss tangent or dissipation factor ($\tan \delta_\varepsilon = \varepsilon''/\varepsilon'$) is usually reported.[2] Loss or energy absorption occurs because energy and time are required to establish the polarization. Consequently, in a dynamic field the polarization of the material lags the applied field. A dielectric material with both the lowest possible dielectric constant and dielectric loss is desirable for applications as electrical insulators.

An electric signal moving through a dielectric can be described as an electromagnetic sine wave or as a superposition of different sine waves. As the signal advances it polarizes the dielectric. This interaction with the dielectric limits the speed of the signal. The speed at which an electromagnetic sine wave propagates through a medium is inversely proportional to the square root of ε, a factor relevant to the signal speed in an electronic package.

If the signal is a superposition of many different sine waves, as in a square wave signal pulse, the dielectric behavior at each of the component frequencies

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1 Commonly the ' is omitted in symbolizing the real component of the complex dielectric constant as the dielectric constant of interest is the one for dynamic (AC) fields.

2 Incorrectly, tan δ is sometimes called the dielectric loss factor, the term reserved for ε''.

has to be considered. If the dielectric constants at the various frequencies differ, signal shape dispersion can result leading ultimately to weak signals unable to trigger the intended on/off event. To counteract signal dispersion higher energy signal pulses need to be used that directly influence the power consumption of a computer.

The final property to be discussed here concerns signal density. Electromagnetic signal waves traveling through a signal line can induce a signal in a parallel signal line. This phenomena is often called crosstalk. The magnitude of the induced signal depends on the magnitude of the original signal, the distance between the two conductor lines and the dielectric constant of the material between them. The lower the dielectric constant the closer the signal lines can be without inducing signals of significant magnitude.

8.3 MULTILEVEL THIN FILM STRUCTURES

Current state of the art MCMs in high performance computers consist of a multilayer ceramic (MLC) carrier which is combined with a polymer/metal thin film module (TFM)[3]. The MCMs are populated either with chips connected by wire bonding, tape automated bonding (TAB) or by flip chip as described in Chapter 9. TFMs consist of at least two signal planes but can have many more layers. All TFMs currently in production have one feature in common: they all use a polyimide as an interlayer dielectric [2] as described in later sections of this chapter.

8.3.1 Major Technical Challenges

It is desirable for any electronic component, particularly for the package, to avoid field failure. Package field failures, such as electrical shorts or opens, often occur because the package first fails mechanically, which then leads eventually to failure in conductor lines by corrosion, etc. Figure 8-1 shows a schematic drawing of a TFM. Highlighted in the drawing are areas responsible for the mechanical failure of the TFM:

1. Interfacial failure leading to local adhesion loss or to catastrophic delamination with complete detachment of a layer from the substrate

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[3] This area is discussed from the perspective of IBM mainframe computers with emphasis on C4 chip connection technology.

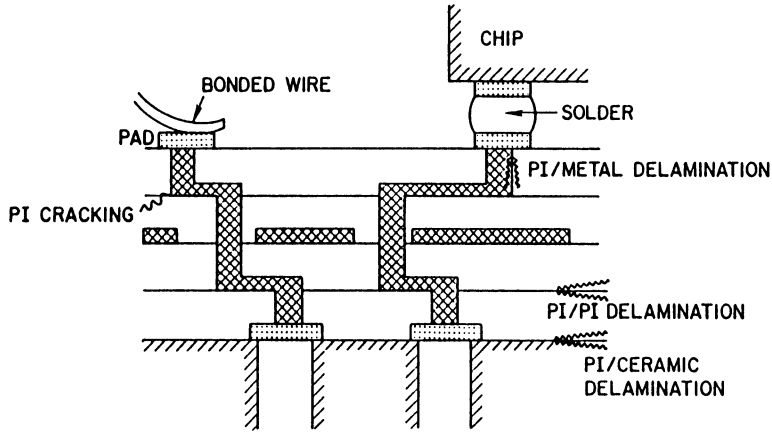

Figure 8-1 Schematic drawing of a thin film module (TFM).

2. Material failure such as cracking or crazing[4].

Interfacial and material failures are related to the presence of stress. In fully cured polymeric coatings, such stress is due nearly exclusively to the presence of materials with differing coefficients of thermal expansion (CTE). Therefore, one of the major technical challenges in the manufacture of TFMs is stress management, focusing on low stress materials.

Mechanical failure sometimes occurs because the properties of an initially good material degrade during processing. The severest demand on organic polymers in TFMs is the necessity to survive the high temperatures (up to 370°C) of the chip joining process. In this flip chip solder bump (FCSB) process, chips are connected to the substrate solder bumps that are used as electrical contacts between chips and signal and power sources. The solder bumps are made of a lead/tin alloy with a melting point on the order of 360°C. The requirement to withstand exposure to the many solvents and aggressive processes such as plasma cleaning which occur in the fabrication sequence also is very challenging.

Requirements on a polymeric dielectric for building reliable TFM structures lead to a wish list for the ideal TFM polymer. Table 8-1 shows such a list of

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[4] Crazing is a material failure which usually precedes crack formation in polymeric materials.

Table 8-1 Properties of an ideal packaging polymer.

Dielectric constant	2.0 to 3.0 frequency independent
CTE (ppm/C)	1 to 5
Thermal stability	at 400∘C <0.1 wt. %/hr
Young's modulus	0.7 < x < 3.0 GPa
Elongation at break	>10%
Critical crack propagation	above 2.5% strain
Adhesion	good to metals, substrate and self
Application	from solution (spin, spray)
Planarization	> 90%
Shrinkage	< 10 vol. %
Water absorption	0.1 to 0.5 %
Solvent resistance	no swelling, no crazing
Etchability	RIE, laser, wet: no residue
Color	light, transparent

ideal properties. The requirements for a given application need to be ranked in order of their importance as determined by both the manufacturing process and the desired performance. While performance mostly is based on speed and density, both of which are related to the dielectric constant of the polymer, there are several options for the fabrication process. The range of these options may be limited if some processes are fixed, such as C4 chip connection process, so the material must be selected with that in mind. Some processes can be changed to suit the dielectric. These decisions depend on the extent that a company is committed to a given chip connection process or fabrication facility.

8.3.2 MCM Fabrication Processes

First, one has to decide on a chip connection technology as discussed in Chapter 9. Wire bonding and TAB require only moderate temperatures to make the

connections and easily accommodate the CTE mismatch between chip and module due to the relative flexibility of the joints. Unfortunately, the number of I/Os and the cooling of TAB (flip TAB has no cooling problem) or wire bonded chips are serious limitations. Flip chips or C4s usually require a high chip joining process temperature. However, they allow much higher I/O densities.

Next, it is necessary to decide what substrate to use. Alumina multilayer ceramic (MLC) substrates have the advantages of a mature technology and good mechanical properties and the disadvantages of a high CTE and a high dielectric constant. Silicon, used as the substrate, matches the CTE of the chip perfectly, but silicon is relatively brittle and via formation and multilevel structures in silicon substrates are difficult to obtain. Glass ceramics, which have CTEs matched to silicon, have relatively low dielectric constants and can be used for manufacturing complex MLCs. However, their mechanical and thermal properties are limitations. These ceramics are discussed further in Chapter 6.

The relationship between the dielectric and conductor must be considered when selecting the conductor. The CTE of the conductor is usually higher than that of the substrate. The dielectric should be chosen to act as a cushion between the metal and substrate. Copper is often desired for its low resistivity (1.7×10^{-6} Ω-cm) and because it is possible to plate-up. Its disadvantage is that it has very poor adhesion to polyimides and requires capping with an adhesion layer such as chrome. Aluminum is sometimes used for its good adhesion to polyimides simplifying the processing, but it has a higher resistivity ($\approx 2.7 \times 10^{-6}$ Ω-cm) and can exhibit migration when heated repeatedly to typical polyimide curing temperatures. Such migration can lead to the formation of filaments that grow on the aluminum lines and can eventually cause shorts. Aluminum lines thinned by migration can rupture under the stress caused by the expanding polyimide.

The next decision concerns the design of the multilayer thin film (MTF) process. For instance, it is planar or non-planar as described in Chapter 7. The choice of design often determines the processes necessary to realize the product. A planar process might involve via formation, via laser ablation, blanket metal evaporation, chemical mechanical polishing, liftoff processing and metal etching. A non-planar process might involve reactive ion etching (RIE) of the polymer, metal sputtering and metal wet etching. Electro or electroless plating might be applied in either design. All processing steps possibly may have negative effects on the organic films or only with some polymers. In any case, the choice of design and processing steps significantly influences the choice of the dielectric.

In recent years photosensitive polyimides (PSPIs) have become available commercially. Figure 8-2 shows a comparison between a process utilizing PSPI and one with conventional polyimide. Obviously the PSPI process involves fewer process steps and, therefore, promises higher cost effectiveness.

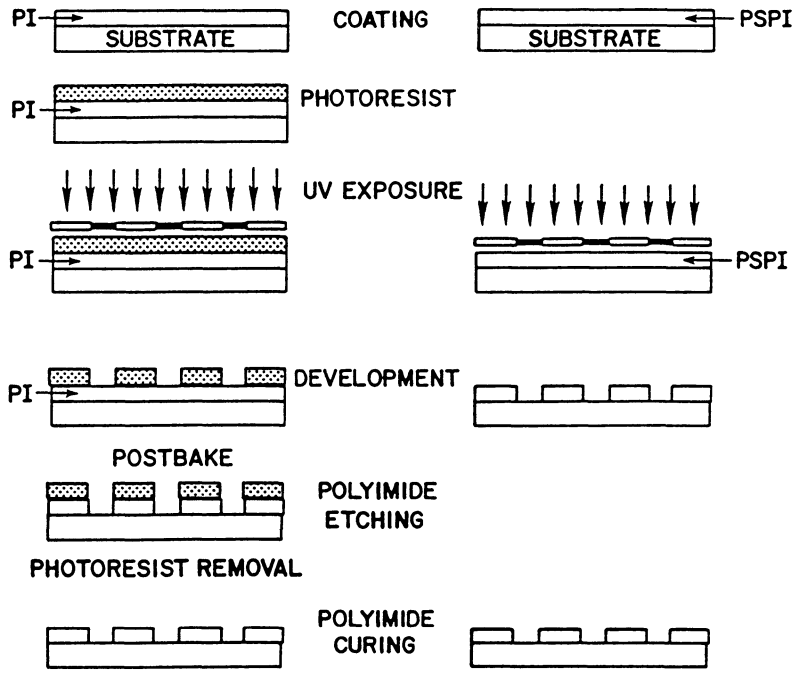

Figure 8-2 Comparison of the process steps in TFM built with conventional and photosensitive polyimide.

Unfortunately, PSPIs still have low photosensitivity, high stress, propensity to mechanical failure, high dielectric constants compared to their nonphotosensitive analogs, inferior thermal stability and often poorer shelf life. Because of the very substantial advantages PSPIs potentially have over conventional polyimides, research in this area is very intense.

8.3.3 Dielectric Processing

The most widely used methods to apply a dielectric are spin coating, spray coating, lamination and extrusion coating, all of which are described in Section 7.4.2. Most polymers require that a primer (adhesion promoter) be applied before polymer deposition. After drying, the polymer is cured to remove solvents. Chemical processes also can occur, producing volatiles species which also must be removed. The final properties of the dielectric are determined by the cure schedule. However, the properties also can be affected by further processing.

Patterning of the dielectric can be done by dry processes (RIE or plasma etching) or by wet etching as presented in Section 7.4.3. RIE or plasma etching, using oxygen plasmas, works for most polymeric dielectrics. Wet etching, usually with aqueous alkaline solutions, works only with certain polymer dielectrics such as polyimides and generally only if the polymer is undercured.

Liftoff (described in Section 7.4.3) is another process to which polymeric dielectrics may be exposed. The interaction of the hot solvent in the liftoff process with the underlaying polymeric dielectric can cause problems like swelling or solvent induced crazing.

After design and processing decisions are made, the polymeric dielectric is chosen. The combination of polymer properties must be appropriate for the user's particular application. Important properties for this consideration are dielectric constant, thermal stability, glass transition temperature (T_g), CTE, moduli, elongation at break, failure mechanisms, solvent resistance, adhesion to various materials, water uptake, planarization, curing conditions, etchability (plasma, RIE, wet etc.), shelf life and others (ionics content, batch to batch stability, barrier properties, processing conditions etc.). Some of these properties are related and knowledge of one property can give an indication of the quality of another. How to interpret data provided by a supplier or obtained from the literature will be discussed in the next paragraphs.

8.4 POLYMER PROPERTIES

8.4.1 Some Polymer Specific Terms

Polymers are either amorphous or semicrystalline. Amorphous materials do not exhibit any crystalline nor liquid crystalline order. They can be thought of as frozen liquids (glasses). Their softening temperature is the glass transition temperature above which no further transitions are observed. Semicrystalline polymers consist of amorphous and crystalline phases and also are called two phase or multiphase polymers. The degree of crystallinity can vary with processing conditions and film thickness. The phase structure of a polymeric material is called its morphology. Particles added to a polymer result in a filled polymer.

From a chemical standpoint, one distinguishes between linear, branched and crosslinked polymers. In a linear polymer, all repeat units, the building blocks of the polymer, are connected only to one or two other units. In branched or crosslinked polymers, some repeat units (branch or crosslink points) are connected to more than two other units. As the ratio between crosslink points and linear units increases, so does the crosslink density, the glass transition and,

often, the brittleness of the material. Linear and branched polymers dissolve in appropriate solvents; crosslinked polymers only swell. Linear and branched polymers can be deformed plastically by heating them above their glass transition temperatures or their melting points as long as this is below their thermal decomposition temperature. Therefore, these materials are called thermoplastics. They are usually tough materials. Crosslinked polymers can be deformed elastically even above their melting or softening temperature. These materials usually are processed starting from small, soluble units that produce the insoluble, crosslinked polymer upon chemical reactions during cure. They are called thermosets. They tend to be brittle but are easily processed.

The chain of repeat units is called the backbone of the polymer. This backbone ranges from flexible to rigid. In the latter case one speaks of rigid rod backbones. Some polyimides have rather rigid backbones which are called rigid rod-like. Rigid rod-like backbones can align themselves with respect to a substrate. This phenomenon is called chain orientation and causes many properties to be anisotropic.

8.4.2 Dielectric Constant

The dielectric constant of a dielectrical material should be low (2 - 3.5) and constant over a very wide frequency range from DC to well into the GHz range. The dielectric loss tangent, tan δ_ε, should be frequency independent and below 0.01.

Routinely, dielectric measurements are made by parallel plate capacitance methods over a range of only 0.1 kHz - 1 MHz and over a wide temperature range. The dielectric constant does not vary significantly with frequency (on the order of 0.1) for many of the polymeric dielectrics used in electronic packaging. However, some fluoro-containing polyimides exhibit significant changes with frequency on the order of 0.3 - 0.5 [4]. The values obtained by parallel plate capacitance measurements on films depend very critically on the uniformity of the film. Consequently literature values are often inconsistent. Sources of error such as absorbed water, contact resistance, ion content, edge effects and/or pinholes can complicate further the measurement of dielectric constants. The combination of these error sources leads to the multitude of values found in the literature for identical materials; reported variations of as much as 0.7 for the same material are not uncommon. Tables 8-2 through 8-6 indicate ranges of values for properties of packaging polymers taken from product literature. Table 8-2 shows values for some classes of materials obtained by parallel plate capacitance measurements between 0.1 kHz and 1 MHz.

Many high temperature stable polymers exhibit rigid rod-like backbones. In the presence of a substrate such materials orient themselves with respect to the

Table 8-2 Ranges of Dielectric Constants.

Ceramics	PIs	Fluoro-polymers	BCBs	PPQs	PIQs
5 - 9	2.5 - 3.8	1.9 - 2.6	2.6 - 2.8	2.8 - 3.0	3.2 - 3.4

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

substrate and consequently many properties are anisotropic [5]. Particularly in rigid rod-like polyimides, the dielectric constant in the plane may be higher than that perpendicular to the plane [5], [7], [24]-[26]. Unfortunately measured by the usual parallel plate capacitance method only the lower value, that perpendicular to the plane, can be determined.

8.4.3 Thermal Stability

Sufficient thermal stability is essential for organic dielectrics because the polymer properties, particularly mechanical properties, must remain unchanged during high temperature processes, such as curing of subsequent layers, chip joining or rework. Additionally, outgassing, which usually accompanies thermal degradation, can destroy the multilayer structure, by causing delamination.

Thermal stability is usually measured by thermal gravimetric analysis (TGA) which measures the weight of a sample versus temperature. Two modes of measurement are available. In the dynamic mode, the sample is heated with a given heating rate (typically 10°C/minute) and the temperature at which a percentage of weight (1%, 5% or 10%) has been lost is recorded. This method measures kinetic effects and the results are heating rate dependent: the higher the heating rate the higher the temperature at which the particular loss is observed.

In the isothermal mode, the sample is heated quickly, then held at a given temperature and the weight loss per hour is measured. The results are given as weight loss in unit of percent per hour (wt.-%/h). From an electronic packaging standpoint, the values obtained through the first method are of little value. Because many processing steps involve annealing at relatively high temperatures, weight loss data at a given temperature are much more useful in understanding the thermal stability of a material.

Contrary to common sense, a low weight loss per hour value does not necessarily describe high thermal stability. A material is only thermally stable when its properties at the temperature in question do not change.

Table 8-3 Isothermal Weight Loss Data (wt.-%/h in N_2).

Temperature	PIs	Fluoro-polymers	BCBs	PPQs	PIQs
350°C	negligible	0.006-too high	1	negligible	negligible
400°C	0.05-1.5	2-too high	10	0.02	0.1-0.5

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

Curing reactions are accompanied by weight loss caused by initial solvent loss or loss of condensation products. Additional weight loss can occur in polymers at high temperatures caused either by outgassing of residual solvent or by degradation reactions [8]. The latter can be of two types: chain scission accompanied by the formation of radicals and elimination of water, CO_2, HF, etc., leading to formation of unsaturated compounds (carbon enrichment). Whereas a small number of elimination reactions might alter the polymer properties only slightly, radical formation is usually only the first step in a series of reactions. The most common of them is crosslinking of the polymer. This can lead to embrittlement, changes in the glass transition temperature, lowered solvent uptake, lowered elongation at break, adhesion loss, etc. It is important to keep in mind that if one property changes usually others do as well. As desirable as a lowered solvent uptake might be, the parallel increase in brittleness might make such an improvement undesirable. In Table 8-3 weight loss ranges obtained from isothermal measurements are given for some classes of electronics packaging polymers.

8.4.4 The Glass Transition Temperature

The glass transition temperature, T_g, is the temperature at which glassy polymers soften. Above this temperature polymers that are not crosslinked can flow. If the polymer is a two phase material (consisting of crystalline or liquid crystalline and glassy domains), the T_g is the temperature at which the glassy phase softens. These materials behave like a crosslinked material and thus do not flow above T_g. The T_g is important because a number of properties change above this temperature. Above the T_g, stresses are released (due to a drop in modulus), the CTE increases (without increasing the stress as long as the material is not three dimensionally constrained due to the mentioned modulus drops above T_g), defects (such as crazes) might be healed, adhesion might increase and dimensions

Table 8-4 Ranges of Glass Transition Temperatures, T_g (°C).

PIs	Fluoro-polymers	BCBs	PPQs	PIQs
300-> 400	160-320	310-> 350	361	300-> 400

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

(line spacing) might change due to polymer flow. The magnitude of these changes depends on the amount of the glassy domains in the system. The most pronounced changes occur in purely glassy materials with a sharp glass transition and are less pronounced in multiphase systems.

For our discussion it is important to mention two important characteristics of the glass transition [27]. First, T_g is not a clearly defined temperature but rather a temperature range. Secondly, T_g is not a transition in an equilibrium thermodynamic sense, although the underlying phenomena might be such a (second order) transition. This has two consequences. First, measured T_g values depend on kinetic factors such as the frequency of the measurement and/or the heating rate of the sample. Secondly, the temperature given as T_g is chosen more or less arbitrarily to be an easily observable feature of a measured experimental curve. Typically T_g is measured by differential scanning calorimetry (DSC) or by dynamic mechanical methods such as dynamic mechanical thermal analysis (DMTA), dynamic mechanical analysis (DMA), or torsion pendulum. The T_g in DSC measurements is chosen to be either the onset or the midpoint of the observed transition. T_g values obtained by DSC are lower than the dynamic mechanical values, where the frequency is usually fixed at 1 Hz but higher frequencies are used as well. In dynamic mechanical methods, the T_g is usually taken to be at the maximum of the tan δ peak. Sometimes the temperature at the onset of the modulus drop is given.

The T_g can be affected by the degree of cure [10] and by the stress exerted on the polymer chains [11]. Crosslinking has a particularly strong effect on the glass transition especially at high degrees of conversion where small changes in the degree of crosslinking can lead to large T_g changes. A list of ranges of T_g for various classes of polymers is given in Table 8-4.

8.4.5 Coefficient of Thermal Expansion

Stress build up in electronics packages is due mostly to the different coefficients of thermal expansion (CTEs) of the materials encountered in a package [24]. An

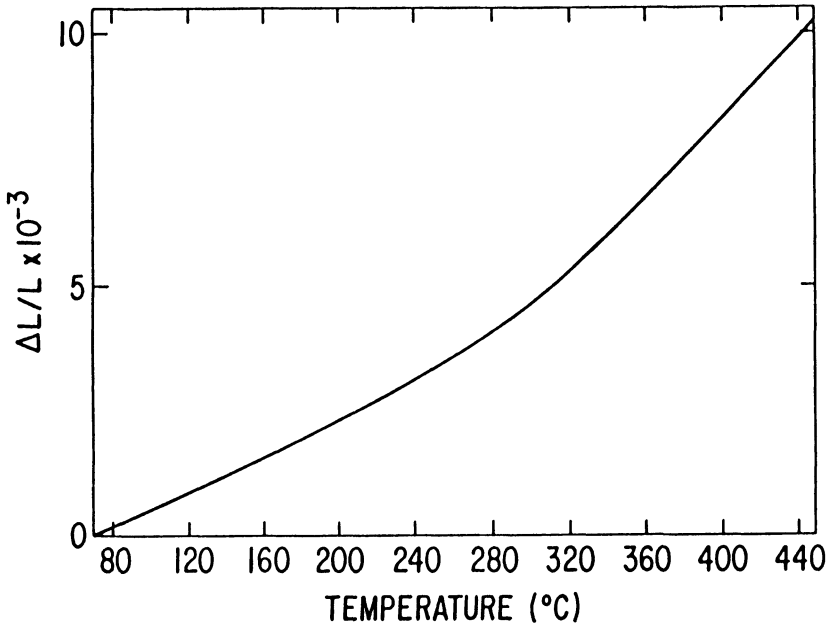

Figure 8-3 Relative dimensional change (Δl/l) versus temperature for a typical polymer dielectric such as BPDA-DA cured to 400°C at 5°C/min.

estimate of the magnitude of stresses in a package can be obtained knowing the CTE of the polymeric dielectric. As with other properties, the CTE of a polymer is a complex property depending on many factors. For example, it changes with temperature (Figure 8-3) and, therefore, the values of CTE should specify a temperature range. Furthermore, it can depend on the film thickness, the degree of cure, the heating (curing) schedule and the direction of the measurement with respect to the substrate plane [13]. If the polymeric material is isotropic, only one value is needed (for a given temperature range and cure state). However, many thin films, particularly of polyimides, are anisotropic. Therefore, the linear in-plane CTE can differ markedly from the linear out-of-plane CTE [13]-[14] (Table 8-5). Volume or bulk CTEs are rarely given.

Typically, the linear in plane CTE is measured on free standing films with a thermal mechanical analyzer (TMA) over a wide temperature range. Measurements on coatings also have been made by measuring wafer bending through x-ray analysis or optically with a laser (wafer bending instruments) [13]. In all the measurements on coatings, the CTE has to be extracted from the

Table 8-5 Linear Coefficients of Thermal Expansion (ppm/°C = 10^{-6} m/m°C).

Direction	PIs	Fluoro-polymers	BCBs	PPQs	PIQs
In-plane	2 - 60	90 - 300	65	40	3 - 58
Out-of-plane	60 - 100	90 - 300	65	40	n/a

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

substrate stress. The out-of-plane (often called z-directional) linear CTE can be measured by laser interferometry.

The thermal stress in a package is determined by the in-plane linear CTE, the film and substrate thickness, the relaxation modulus and the substrate CTE and modulus. The stress originating from the differences in film and substrate CTE is often called the thermal mismatch stress. If the one directional (tensile) stress, T, is known, one can calculate the stress in single layer coatings or thin multilayer films that is given by $T/(1 - \upsilon)$, where υ is Poisson's ratio, which in polymers is usually between 0.4 and 0.5. (Poisson's ratio is a measure of the compressibility of a material and is 0.5 for incompressible materials.) In thick multilayers, particularly in the presence of vias and signal lines, expansion perpendicular to the substrate is restricted. In such three dimensionally confined structures the stresses can become very high because the stress is now given by $T/(1 - 2\upsilon)$. The closer Poisson's ratio is to 0.5 the higher the stress and the higher the likelihood that mechanical failure (fracture) will occur.

The CTE is related to the elastic modulus of a material. The elastic modulus reflects the energy needed to change the bond length in the polymer chain by mechanical energy, the CTE reflects the same change effected by thermal energy. A steep energy profile for even the weakest bond(s) in the chain characterizes a high modulus, low CTE material; a shallow profile describes a low modulus, high CTE material. Because the thermal mismatch stress is determined by the product of the elastic modulus of the coating and the CTE difference between substrate and coating, a lower film CTE does not always lead to lower stress. Consequently, some low stress materials have been designed to exhibit lowered elastic moduli but higher CTEs. Another factor influencing the CTE, particularly in rigid rod polymers (like some low stress polyimides), is chain orientation. In these materials the linear in-plane CTE is lower the more the chains are oriented in-plane. Because the orientation is affected by the cure schedule as well as by the film thickness, the CTE depends on both. In general, thinner coatings have

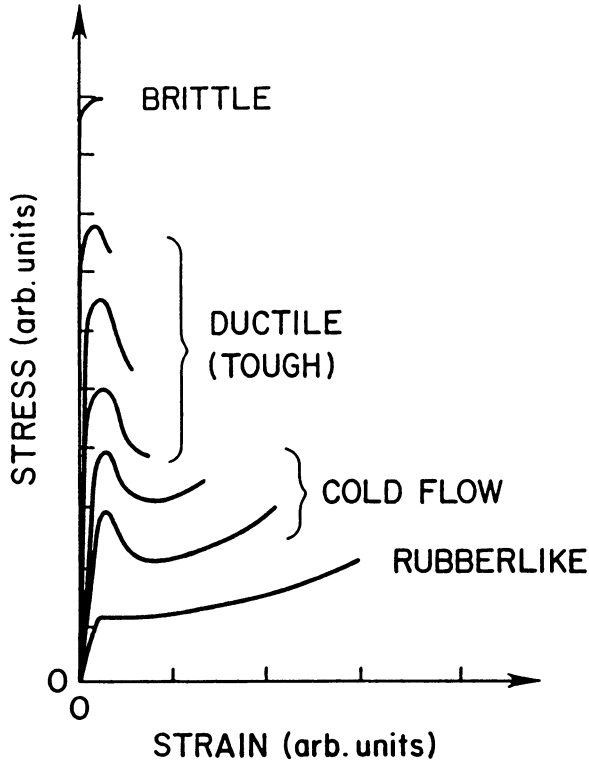

Figure 8-4 Schematic stress-strain behavior of a polymer at various temperatures.

the highest orientation and lowest CTE. Consequently, if thicker coatings are needed it is preferable to work with a low modulus, low stress material.

8.4.6 Mechanical Properties

The mechanical properties of the polymeric dielectric are of great importance for the package reliability in the short term, during handling and processing, as well as in the long term, during the lifetime of the package. The mechanical properties of polymers are a fascinating and intricate area in polymer science [9], [15]. This is due to the viscoelastic nature of polymers. The concept of viscoelasticity is developed from the fact that polymers respond to a mechanical stress by a combination of elastic (solid-like) and viscous (liquid-like) behavior. The ratio of the two behaviors depends on temperature and time (time referring

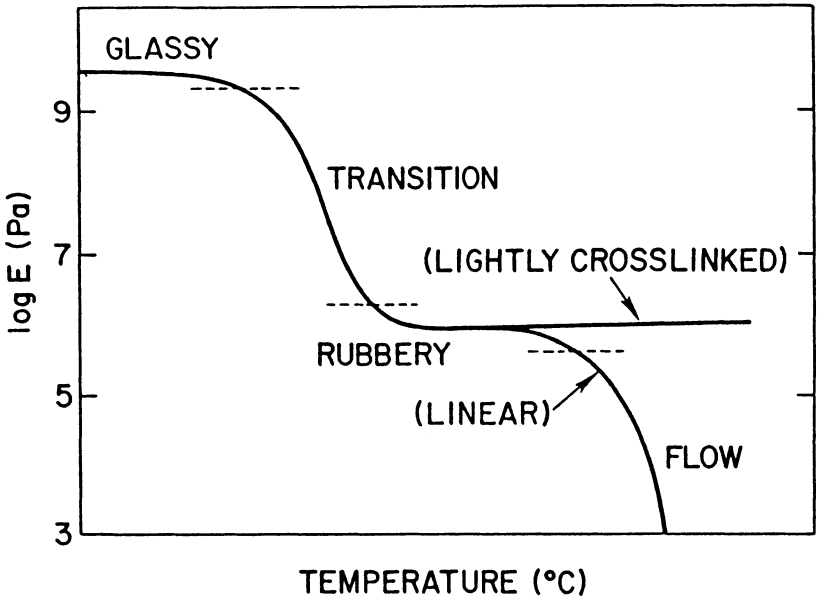

Figure 8-5 Schematic of the modulus change with temperature for a generic polymer.

to the time of application of a disturbance, such as the frequency of a dynamic mechanical measurement or the strain rate in stress strain experiments). The behavior of many polymers can change with temperature (or rate) from brittle to tough to cold flow to rubber like Figure 8-4. These responses also depend on structural features such as the degree of crosslinking, degree of order and chain orientation, presence of plasticizers such as solvent etc. The most important temperature with respect to the mechanical properties is T_g, which separates the region in amorphous polymers dominated by solid-like behavior from predominantly liquid-like behavior (Figure 8-5).

The data usually found in data sheets are Young's modulus, tensile modulus, linear elastic modulus, tensile strength, yield point, yield strength, elongation at break, and ultimate strength. These are usually extracted from stress strain curves at a given strain rate (Figure 8-6). The modulus is by definition the ratio of stress over strain (deformation) and is a function of rate and temperature. Therefore values of moduli are only useful if temperature and strain rate are given simultaneously. Fortunately, a number of the most important electronics packaging materials do not exhibit a strong strain rate dependence at room

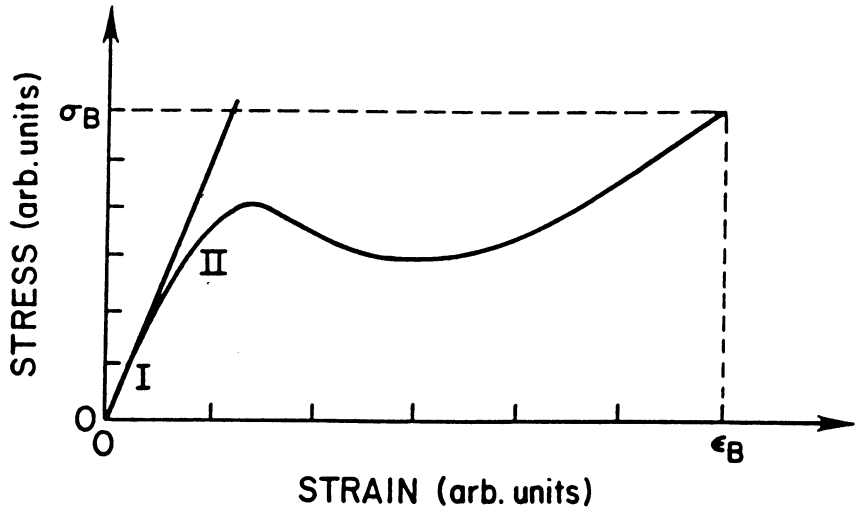

Figure 8-6 Schematic representation of a stress-strain curve for a tough polymer. The elastic limit is reached at *I*, the yield point is reached at *II*, and necking begins at the maximum of the curve. σ_B is the tensile strength and ε_B is the elongation at break. The Young's modulus is the slope of the tangent at small elongation.

temperature [4]. The Young's modulus is identical with the tensile modulus and the linear elastic modulus. They all represent the slope of the stress-strain curve at small strains (the linear region) in a tensile experiment (Table 8-6). In electronics packages, the strain usually encountered (from CTE mismatch) is small. The tensile strength is the maximum stress a material can carry. The yield point is the strain at which the polymer deforms irreversibly by flowing, developing a neck (a decrease of the cross sectional area) in the tensile specimen. This point depends on the accuracy of the measurement which is why ASTM Standard E 8-69 has been introduced. The yield strength represents the stress at which the yield point is reached. The elongation at break (Table 8-6) is the elongation at which a material breaks (maximum achievable strain). This property is watched closely because it gives an indication of the brittleness of the material which, in turn, is important for assessing the propensity of the material for mechanical failure such as cracking. A material is considered brittle when fracture occurs at the first maximum of the stress strain curve and the elongation at break is below 10%. The ultimate strength or ultimate tensile strength is the maximum load (at the elongation at break) divided by the initial cross sectional

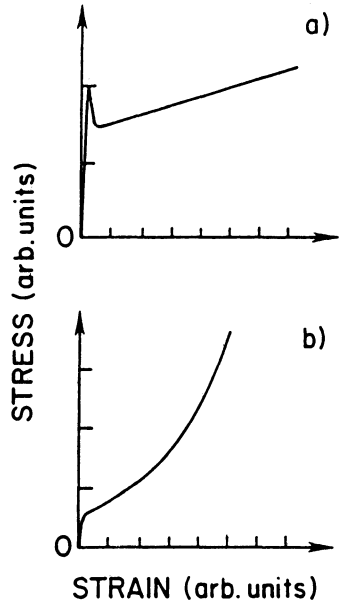

Figure 8-7 Stress-strain curves a) without and b) with consideration of the change in cross sectional area. Note the disappearance of the maximum in the experimental curve upon correction to the true test stress curve [16].

area. Necking in a material causes changes in the specimen. These changes are not reflected in the typical stress strain curves. Stress strain curves with and without correction are shown in Figure 8-7. A list of ranges of two mechanical properties for various packaging materials is given in Table 8-6.

8.4.7 Failure Mechanisms

Mechanical failure is a result of stress and leads to stress release. If the stress in a composite structure becomes too high, stress release occurs either by delamination (adhesive strength is exceeded) or by cracking, crazing or deformation zone formation (cohesive strength of the material is exceeded). A crack is a failure in which two new surfaces are created which are not connected across the crack, for example, a crack is not filled by any material. A craze, created by local yielding, is filled by oriented fibrils separated by voids [15]. Deformation zones are pre-crack zones occurring in materials which do not exhibit crazing, often high T_g materials. In these zones, shearing of the material has occurred; however, the density is not changed significantly.

Many material failures originate at stress concentrators that can be dust particles, vias, corners or edges of signal lines. Material failure can also be

Table 8-6 Young's Moduli and Elongation at Break (%).

	PIs	Fluoro-polymers	BCBs	PPQs	PIQs
Modulus (kpsi)	280 - 1300	200 - 235	480	500	550
Modulus (GPa)	1.9 - 9.0	1.4 - 1.6	3.3	3.45	3.8
Elongation	2 - 120	2 - 12	7	20 - 30	10 - 45

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

Table 8-7 Propensity to Failure Propagation.

DIELECTRIC	FAILURE PROPAGATION
Two phase polyimides	low
Amorphous polyimides	medium - high
Fluoropolymers	medium - high
BCBs	medium - high
PIQs	low - medium
PPQs	medium

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

initiated in areas where material property fluctuations lead to localized reduction of the yield stress. This can be particularly significant in the presence of plasticizers such as solvents or humidity (solvent induced crazing, environmental crazing). It follows that the propensity for forming failure zones will be greatest where stress concentrators are exposed to plasticizers. Failure can also occur due to fatigue; an example would be the cyclic application of stresses which, if applied only once, would not cause yield or fracture. Finally, processing steps like oxygen plasma treatments can cause weak areas. Again, stress concentrators are the most likely areas where accelerated damage occurs.

Crack propagation through a film can lead to catastrophic failure. The force propagating a crack in a coating has been shown to increase with film thickness and with the level of strain in the coating [17]. Crack healing can be attained by annealing the coating above T_g. However, if the cause for the mechanical failure has been thermal mismatch stress, annealing is only a temporary solution.

The propensity for mechanical failure depends strongly on the morphology of a polymer. Glassy, amorphous polymers, in general, will be more prone to failure than two phase systems such as filled polymers, block copolymers or semicrystalline polymers. This is due to the possibility of dissipating energy at the interphase between the phases.

Little data is available about avoiding mechanical failures of a coating. This is due in part to the fact that only a few methods are available to study crack growth in coatings or even in free standing thin films. Because of the lack of data in the literature, only a rough estimate of the propensity for failure propagation and crack formation for various materials is given in Table 8-7.

8.4.8 Chemical Resistance

Resistance to chemicals (solvents and solutions) depends strongly on the nature of the chemical and the polymer. Solvents used in the electronics industry typically include N-methylpyrolidone (NMP), diglyme, isopropyl alcohol (IPA), ethanol, fluorocarbons, 1,1,1-trichloroethane, cellosolve, and water. These solvents are used mainly for liftoff processes, cleaning steps, photoresist processes and flux removal. Solutions are typically aqueous such as plating solutions, caustic etchants, metal etching solutions, adhesion promoters. The problems encountered can be dissolution, swelling, crazing/cracking and degradation (etching). A few general rules exist. Partially fluorinated materials tend to dissolve easier in organic solvents than their hydrogenated counterparts. Perfluorocarbons, however, are the most solvent resistant. Crosslinked materials do not dissolve but they may swell. Swelling increases usually with solvent temperature and decreases with increasing crosslink density. Unfortunately, brittleness also increases with crosslink density. Linear polymers may also exhibit swelling, particularly if they are two phase materials (containing crystalline or liquid crystalline domains). Coatings, particularly of rigid rod-like materials, swell only in the thickness direction because the substrate hinders their expansion in the plane [5]. As with resistance to crack propagation, two phase systems exhibit higher solvent resistance. Solvent induced cracking or crazing is also more likely in amorphous polymers than in multiphase systems. To give a feeling of the variation in solvent uptake between the various dielectric polymers Table 8-8 lists the maximum uptake of NMP at about 80°C. The ranges indicate the dependence of the solvent uptake on the curing schedule.

Table 8-8 Maximum NMP Uptake (wt-%/hr) at 80°C.

PMDA-ODA	BPDA-PDA	Thermid 6015	Teflon® AF	PPQ
40	< 5	> 40 - 10	negligible	< 1%

Note: Uptake in thermid is highly cure dependent.

Resistance to caustic solutions like plating solutions depends strongly on the presence of groups susceptible to nucleophilic attack such as imides and esters. Again, multiphase systems are more resistant to attack, for example by KOH etching solutions. Furthermore, fluorine-containing polymers are usually more difficult to etch by aqueous solutions or are not attacked at all as in the case of Teflon® AF. This is due to the decreased wettability of fluoro-containing polymers compared to polyimides like Kapton®.

8.4.9 Adhesion

Destructive stress relief in a multilayer system occurs either when the cohesive strength of one of the materials is exceeded or when the adhesive strength is exceeded. The latter causes delamination. Often the interfacial strength is the weak link in a package. Fortunately, the adhesive strength between two materials can often be strengthened by using adhesion promoters. The choice of adhesion promoter depends on the substrate [18]. For surfaces with free hydroxyl groups (quartz, glass, alumina, metal oxides) silane coupling agents are used. For inert metal surfaces reactive metal layers are used.

Although partial delamination might not lead to structural disintegration or immediate electric failure of an electronics package, it is nevertheless grounds for concern because usually polymers pick up some amount of water. If a continuous water film can form over a two metal junction, a galvanic element is formed and corrosion occurs. A continuously adhering film acts as corrosion protection.

Adhesion depends on both materials connected in the adhesive link and on the way the adhesive bond is fabricated [18]. For instance the adhesion of copper deposited onto Teflon® AF is good but the adhesion of Teflon® AF deposited onto copper is poor. Particularly interesting is the behavior of polyimides. The polyamic acid precursors usually used can be quite strong acids and as such can dissolve metal oxides [19]. These oxides can act not only as catalysts in the thermal degradation of the polyimide [20], but also can increase the dielectric constant of the polymer. Once the precursor is imidized no acidity

remains. However metal can now migrate into the film because of the lack of metal-polymer interaction. Such Cu diffusion and consequently dielectric constant increase is observed, for example, when Cu is slowly evaporated onto fully imidized polyimides [1]. The most important adhesion issues in MCM packages are the adhesion of the polymeric dielectric to itself, to metals (Cu, Cr, Al, Ti), to ceramics and to SiO_2 and the adhesion of metals to the dielectric.

The measurement of interfacial strength by adhesion tests, such as the very popular peel test, is ambiguous. Most methods depend on many factors such as the speed of peeling, width of peeled strip and the mechanical properties of the peeled material. Peeling of polymer films is particularly problematic because a substantial amount of the peel energy goes into the deformation of the peeled polymer and is not related to the actual adhesion strength. Another problem with most adhesion measurements is that they are destructive by nature. Only after the sample is destroyed, can it be known if its adhesion was good or not.

In listing peel strength data, test parameters usually are not indicated, making comparisons between peel test data impossible. Therefore, adhesion is often described in data sheets simply as "good" or "bad." It cannot be clear from such a generic description if "good" means "good enough for the intended application."

The complexity of adhesion issues becomes apparent when degradation of adhesion occurs over a period of time or after certain processing steps. This area is still under intense scrutiny and understanding of the process is at best limited. However, a few generalizations can be made.

1. Good wetting (good contact) between the two materials at an interface is a condition of good adhesion. Consequently, contamination of surfaces can severely decrease adhesive strength.

2. The influence of both temperature and humidity can severely degrade the adhesion, particularly between metal oxide or ceramic surfaces and many polymers.

3. If the metal oxide-ceramic surface is primed with an adhesion promoter, adhesive strength is retained over a significantly longer period of time.

4. If corrosion of the metal occurs due to humidity, severe adhesion loss is observed.

5. Polymers that exhibit a large modulus drop at T_g usually adhere well, particularly when heated above T_g during processing. This is caused by increased wetting.

6. Crosslinked polymers which start from low molecular weight precursors (thermosets) usually adhere well.

7. Thermal degradation often leads to decreased adhesive strength.

In the following, the generalized adhesion characteristics are given for a number of pertinent polymers:

1. Amorphous polyimides adhere well to themselves and metals such as Cu, Cr and Al.

2. Multiphase polyimides do not adhere well to Cu, but adhere well to reactive metals such as Al and Cr [1]. The adhesion to ceramics is good if aminosilane adhesion promoters are used. The self adhesion of multiphase polyimides is marginal. However, it can be increased by using appropriate curing schemes and/or surface treatments.

3. Fluoropolymers exhibit good self adhesion and good adhesion to ceramics and SiO_2. Also, the adhesion of metals evaporated onto these materials is good. However, fluoropolymers do not stick well to metals when deposited from solution. The adhesion to metals is improved markedly by exceeding T_g.

4. Information on adhesion of BCBs (benzocyclobutene) to various surfaces is not yet available but is expected to be good.

5. PPQs (polyphenylquinoxaline), which are in general amorphous, behave similarly to amorphous polyimides. They have excellent self adhesion and good adhesion to copper. No problems with metal corrosion are observed because PPQs are fully reacted.

6. PIQs (polyimide iso-indoloquinazolinediones) tend to exhibit two phase morphologies and show the same problems as two phase polyimides.

8.4.10 Water Uptake

Water uptake is of concern because it increases the dielectric constant and can lead to adhesion loss, corrosion, decreased stress in general [24] but increased stress in three dimensionally confined areas [4], molecular weight breakdown by hydrolysis, and blistering during heating. The quantity which is usually measured is the maximum amount of water uptake. The kinetics of drying is

Table 8-9 Maximum Water Uptake Values at 95% Relative Humidity and Room Temperature.

DIELECTRIC	WATER UPTAKE (%)
Polyimides	0.25 - 4.0
Fluoropolymers	0.01 - 0.1
BCBs	0.25
PPQs	0.1
PIQs	0.8 - 1.0

particularly important where fast heating rates and areas with continuous metal coverage are involved. Insufficient pre-drying in such cases might lead to blistering for instance, during chip joining [21].

Usually maximum amounts and kinetics of water uptake are measured by thermal gravimetric analysis (TGA), Kahn balance or by piezoelectric balances. The amount of water uptake depends on the degree of cure, on temperature and on relative humidity. These conditions must be given to compare values. It is also important to note that values obtained in steam are not necessarily identical to values obtained by immersion in water. Often the latter are lower. Table 8-9 gives ranges of maximum water uptake for various polymeric dielectrics.

8.4.11 Planarization

Planarization, the ability to produce a flat surface over features, is an important requirement for all TFM dielectrics mainly because good yields in the necessary photolithographic processes are obtained only when the resist is planar and uniformly thick. Sufficient uniformity and planarity are obtained only when the surface to be patterned is planar. Values for planarization are given as the percent of difference between the feature height before and after coating divided by the original feature height. Usually planarization is given for isolated features but sometimes planarization over double features is reported. In the latter case, planarization depends on the line spacing and is better for smaller line spaces.

Three properties determine the ability of a material to planarize. First, application of the dielectric should proceed from solutions with high solid content but low viscosity. Some solventless crosslinking systems can exhibit planarization values of over 95%. To obtain the necessary film thickness, the

Table 8-10 % Planarization, Solids Content and Shrinkage.

DIELECTRIC	PLANARIZATION (%)	SOLIDS CONTENT (%)	SHRINKAGE (%)
Polyimides			
PAAs	0.3 - 0.4	10 - 16	25 - 47
PAA-esters	0.3 - .05	20 - 30	25 - 35
PSPI 1	0.2 - 0.4	20 - 35	50 - 60
PSPI 2	0.3 - 0.5	10 - 30	10 - 30
Fluoropolymers	low	2 - 10	none
BCBs	up to 0.95	35 - 62	little
PIQs	0.2 - 0.7	12 - 50	20 - 35
PPQs	0.4 - 0.5	20 - 25	20 - 35

Note: PAA-polyamic acid; PSPI 1 - not intrinsically photosensitive polyimide; PSPI 2 - intrinsically photosensitive polyimide; BCBs can be powder coated.

viscosity of the solution used to apply the coating has to stay within given limits. That means for linear polymers a balance has to be found between a desired low viscosity for planarization and the desired mechanical properties that are best at high molecular weights. Modification of the precursors of the polymer is sometimes necessary. Thus, polyamic acid esters and polyisoimides both have higher solubility and lower viscosity than the corresponding polyamic acids.

Most high temperature stable, solution cast polymers contain appreciable amounts of solvent even after drying at temperatures around 100°C [4]. As a consequence these films shrink upon further heating. Additionally, shrinkage is observed when the curing reaction produces volatile by-products. This is particularly severe in photosensitive polyimides in which photopackages have to be burned out (not intrinsically photosensitive polyimides). Any amount of shrinkage is detrimental to planarization because the absolute shrinkage of the thinner film above a feature is less than that of the thicker film over the substrate.

Finally, polymer flow during cure can lead to increased planarization. This effect is only observed in thermoset materials because melt viscosities of high

Table 8-11 Propensity to Exhibit Cure Dependence of Properties.

DIELECTRIC	CURE DEPENDENCE
Polyimides	considerable
Fluoropolymers	little
BCBs	considerable
PPQs	little
PIQs	n/a

PIs = polyimides BCBs = benzocyclobutenes PPQs = polyphenylquinoxalines
PIQs = polyimide iso-indoloquinazolinediones

molecular weight polymers are very high. Table 8-10 gives ranges for percent of planarization, solids content and film shrinkage in the direction perpendicular to the film plane for the group of electronic packaging polymers under consideration.

8.4.12 Influence of Curing Conditions

Curing usually signifies any heat treatment. It always involves drying, and often involves chemical reactions and structural development (orientation, ordering, high temperature processes). In a number of important dielectrics the properties depend on the degree of cure. It is, therefore, very important to know what the best curing conditions are, how processing influences the degree of cure and what is the relationship between the cure schedule and the resultant properties. Some polymers, on the other hand, show only a very slight dependence on cure schedules. In general it can be said that all crosslinking materials (thermosets) and all materials in which a multiphase structure is formed exhibit properties that are cure dependent. Table 8-11 gives an indication of which dielectrics have cure-dependent properties.

8.5 POLYMER MATERIALS

After contemplating the most important properties of dielectrics for MCMs, the various materials are discussed in this section.

Table 8-12 Suppliers and Trade Names for Several Polyimides.

SUPPLIER	TRADE NAME
DuPont Corporation	Pyralin® PI-2545, PI-2525, PI-2611
Hitachi Chemical Company	PIQ L100, PIX L100, PAL, PIQ-13
Olin/Ciba-Geigy	Probimide® 200 series
National Starch	Thermid® EL-series
Amoco	Ultradel™ 4000 System
Ethyl Corporation	Eymyd® HP
Rogers Corporation	Durimide™ 100 and 120
Hoechst-Celanese	SIXEF® -44 and -33

Note: Trade names usually apply for a series of materials with varying structures.

8.5.1 Polyimides

Polyimides have been by far the most important materials for MCM packaging and are available from many sources (Table 8-12). They are a class of condensation polymers which have at least one imide group in their repeat unit [22]. The polyimides that are most widely used in the electronics industry all have two aromatic cycloimides in their repeat unit (Figure 8-8); the remainder of the repeat unit consists of aromatic hydrocarbons and connecting groups such as ether (-O-), carbonyl (C=O), 6F (CF_3 - C - CF_3 or hexafluoroisopropylidene). Polyimides are synthesized from dianhydrides and diamines. The convention for naming polyimides does not follow IUPAC rules. They are named after the dianhydride[5] and diamine from which they are synthesized. For example, the polyimide based on biphenyl dianhydride or (BPDA), and p-phenylenediamine (PDA) is referred to as BPDA-PDA polyimide. Some of the most common dianhydrides and diamines together with their common abbreviations are shown in Figure 8-9.

The chemical structure of the repeat unit determines the basic chemical and

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5 The names used for the dianhydrides and diamines rarely are IUPAC names which are very lengthy and confusing to the nonchemist.

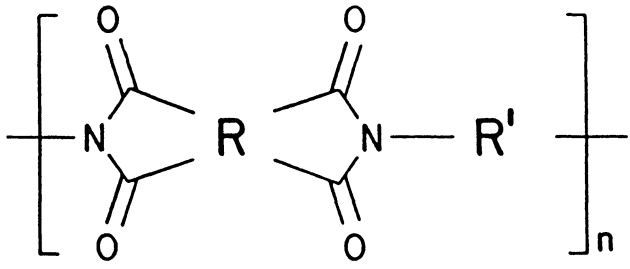


Figure 8-8 Schematic representation of polyimide with two aromatic cycloimides per repeat unit.

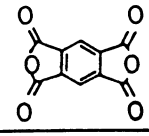
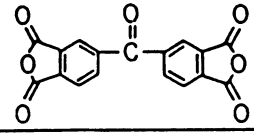
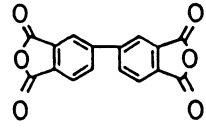
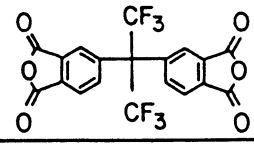
physical properties of the polyimide. The characteristics of the various polyimides can vary widely, although the polyimides used in packaging applications generally have a number of properties in common. These are summarized in Table 8-13. In general, the main advantages of polyimides are high thermal stability, good mechanical properties, and low CTEs. The main concerns are high water uptake and low adhesion.

In comparing polyimides it is of utmost importance to know the chemical structures or at least to know the exact commercial names and descriptions. Unfortunately, many polyimide trade names are confusing. Products with similar trade names are often altogether different materials. On the other hand, sometimes only the solvent or the concentration is changed. It is not surprising that people using these materials, but unfamiliar with the chemistry, tend to lump these materials together under the generic term "polyimides." However, this is comparable to describing electrical conductors as metals. Just as there are sharp differences between aluminum and copper, for example, there are sharp differences between polyimides based on PMDA-ODA (pyromellitic dianhydride and oxydianiline) and on BPDA-PDA.

Polyimides come in two basic variations:

- Polyimide precursors that are applied from solution and converted to insoluble polyimides by curing. These curing processes can be rather complex involving solvent and water removal, imidization, and often crystallization [10]. Only properly cured polyimides exhibit the desired properties.

- Polyimides that remain soluble in their fully imidized form. These include polyimides which contain siloxane segments. Curing of these materials involves only solvent removal.

PMDA	
BTDA	
BPDA	
6FDA	

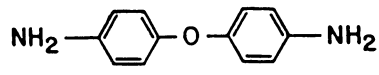
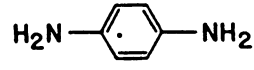
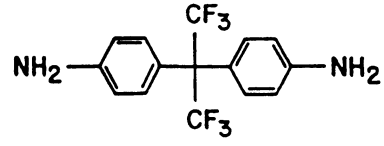
ODA	
PDA	
6FDAM	

Figure 8-9 a) Common dianhydrides and b) diamines with their usual abbreviations.

Table 8-13 Typical Properties of Polyimides.

Dielectric constant	2.9 - 3.5 frequency independent (10^2 - 10^7 Hz); some PIs are anisotropic
CTE (ppm/°C)	in-plane: 5 - 45; in z-direction: 60 - 100
Thermal stability	at 400°C: < 0.1 wt.-%/h
Young's modulus (GPa)	2.5 - 10.0
Elongation at break (%)	10 - 120
Critical crack propagation	above 2.0% strain
Adhesion	marginal to metals, substrate and self; good with adhesion promoter
Application	spin or spray from precursor solutions
Planarization (%)	20 - 75
Shrinkage (vol. %)	30 - 47
Water absorption (%)	0.5 to 4.0
Solvent resistance	swelling in hot NMP, no crazing
Etchability	usually good, residue can cause problems

The most widely used precursor is polyamic acid (Figure 8-10a). More recently, esters (Figure 8-10b) and isoimides (Figure 8-10c) have found applications in the manufacture of MCMs. For example, the MCMs in the IBM System 390/ES9000 are fabricated using a PMDA-ODA ethyl ester precursor but have also been produced using an acetylene terminated BTDA-based isoimide precursor.

Polyamic acids are chosen over other polyimide precursors because they are the best known polyimides, widely used and cost effective, when compared to polyamic acid esters. Disadvantages include their poor adhesion, particularly their poor self-adhesion, and their propensity for attacking metals through their acid functionality. Polyamic acid esters generally have higher solubility and planarize better than the polyamic acids while retaining most of their good

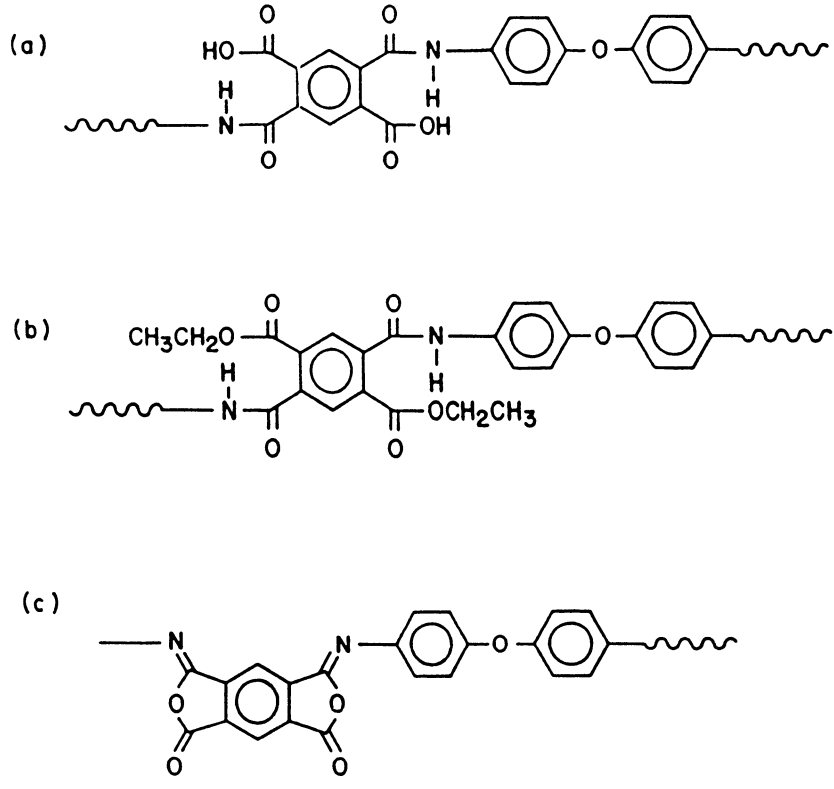


Figure 8-10 Precursors to PMDA-ODA polyimide: a) polyamic acid, b) polyamic acid ethyl ester and c) polyisoimide.

mechanical properties. Esters are difficult to synthesize and are therefore significantly more expensive. Adhesion is slightly improved.

In addition to classical polyimide precursors, thermosetting polyimides are offered, combining a fully imidized polyimide or isoimide oligomer with reactive end groups such as acetylene. Thermosetting polyimides have a number of advantages such as good planarization and good adhesion to themselves and to metal. Disadvantages include low elongation at break, low thermal stability at 400°C, swelling in process solvents and a tendency for solvent induced crazing.

Photosensitive polyimides (PSPIs) are photoresists based on polyimide chemistry. Usually, the photosensitive moiety is eliminated during the curing process and ultimately thermally degraded and volatilized. A smaller group of

photosensitive polyimides are inherently photosensitive [23]. Inherently photosensitive polyimides are usually fully imidized and crosslinking occurs between the main chains. In both cases, sensitizers and other additives are part of the system. The main problems encountered with PSPIs are the short shelf life (some new materials, however, can have a shelf life of one year), the relatively low photosensitivity and the enormous amount of shrinkage (50% and more) incurred during curing, leading to high levels of stress. Furthermore, the resultant polymer tends to contain more voids than the corresponding polyimide without the photopackage. The higher void concentration causes increased water uptake. Inherently photosensitive polyimides often exhibit low thermal stability at 400°C. Exposure to such temperatures can increase the crosslink density leading to low elongation at break and a tendency to craze particularly in the presence of solvents.

PMDA-ODA

Until around 1985 PMDA-ODA based polyimides (Figure 8-11) were the most widely used polymeric interlayer dielectrics and today many companies still produce and use them. They were first commercialized by DuPont under the name Kapton® (in film form) and as Pyralin® 2545 or 2540 (as polyamic acid in NMP/hydrocarbon solution). The advantages of PMDA-ODA are its high thermal stability at 400°C in nitrogen, its excellent mechanical properties and excellent solvent resistance (no crazing). The disadvantages are its marginal adhesion to itself and to Cu, its limited planarization and its large water uptake.

BPDA-PDA

To overcome some of the shortcomings of PMDA-ODA, particularly with respect to its stress build up, BPDA-PDA (Figure 8-12) was first introduced by Hitachi in 1985. This polyimide is characterized by a rigid rod-like backbone (little flexibility in the chain) that imparts a high modulus and a low CTE to the material. The exact values depend on the degree of orientation with respect to the substrate surface, the film thickness and the cure conditions. Besides a lower CTE (5 ppm in 5 μm thick coating) and resulting lower stress, BPDA-PDA exhibits lower water uptake and lower swelling in hot NMP8. The dielectric constant of the dry material is 2.9 to 3.0, just below that of PMDA-ODA. Unfortunately, the adhesion is marginal and requires adhesion promotion. It is difficult to wet etch fully cured BPDA-PDA. Water degrades the mechanical and electrical properties of BPDA-PDA only minimally compared to PMDA-ODA. BPDA-PDA is available in film form (Upilex® S from Hitachi) and as polyamic acid solution in NMP (Hitachi's PIQ L100 and PIX L100, DuPont's Pyralin® 2610 and 2611).

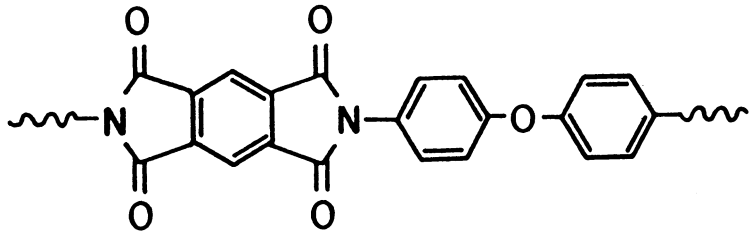


Figure 8-11 PMDA-ODA polyimide.

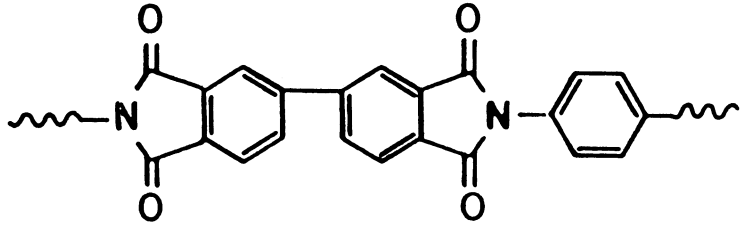


Figure 8-12 BPDA-PDA polyimide.

PIQ-13

PIQ-13 is Hitachi's trade name for polyimide-iso-indolo-quinazolinedione. It is also sold by Cemota. Its precursor is a polyamic acid copolymer based on a mixture of two anhydrides (BTDA and PMDA) and two diamines (4,4'- ODA and 3,4'- ODA with an amid group on the 4 position). It cures in two steps: cycloimidization at about 200°C and the oxime formation at 350°C. This material has been used by Japanese computer manufacturers. Its CTE is 58 ppm/°C for 5 μm films in the range of 30°C - 350°C.

BTDA-Based Polyimides

The most important examples in this group are Pyralin® 2525 and 2555, based on BTDA (benzophenone tetracarboxylic dianhydride) and a mixture of ODA (oxydianiline) and MPDA (m-phenylene diamine). This material is amorphous and therefore has limited solvent resistance compared to the two phase systems. It exhibits a sharp modulus drop at its T_g (about 310°C) which may lead to movement of thin lines above the T_g. The stress relaxation at that temperature leads to a lowering of the thermal mismatch stress at room temperature compared to PMDA-ODA. The advantage of BTDA-ODA/MPDA is its good adhesion to many substrates and to itself. It therefore has been used in one of AT&Ts MCMs.

Photosensitive Polyimides

There is a wide offering of photosensitive materials on the market (Table 8-14). However, their use today is limited because of drawbacks such as high volume shrinkage upon cure, high stress levels, high water uptake, brittleness, short shelf-life and low photosensitivity. Some of these problems have been overcome by the current generation of materials but they still exhibit one or two of these drawbacks. The development activity in this area is considerable.

Fluorinated Polyimides

These materials are the focus of much research driven by the search for lower dielectric constant materials. SIXEF®, based on diamines and dianhydrides containing the hexafluoroisopropyliden (6F) group, exhibit a dielectric constant of 2.65 and were semi-commercially available from Hoechst for a short time. The drawbacks of these materials are lowered solvent resistance, reduced mechanical properties and cost. The weight loss at 400°C is very small (0.1 wt.-%/h), but decomposition occurs above 350°C. Most other materials based on 6F chemistry exhibit very good adhesion, but none of them have been used in MCM packages because of their relatively high CTEs and their low solvent resistance.

Table 8-14 Suppliers and Trade Names for Several Photosensitive Polyimides.

DuPont Corporation	Pyralin® PI-2700 series
Olin/Ciba-Geigy	Probimides® 300 and 400 series
Amoco	Ultradel™ 7000 system
Asahi	Pimel® TL series

Table 8-15 Suppliers and Trade Names for Several Polymeric Dielectrics Other than Polyimides.

Cemota	Syntorg® IP 200
DuPont Corporation	Teflon® AF 1600 and 2400
Rogers Corporation	RO 2000 series
Dow Chemical	XU-13005-02L

8.5.2 Polyphenylquinoxaline

Polyphenylquinoxaline (PPQ) is sold under the name Syntorg® by Cemota (Table 8-15). Its use is limited by the fact that it dissolves only in m-cresol or similarly undesirable solvents. Aside from this drawback PPQs offer many good properties such as good adhesion, high thermal stability, low water uptake, good mechanical properties, and a relatively low dielectric constant of 2.9.

8.5.3 Fluorocarbons

From the standpoint of electrical designers, dielectrics with dielectric constants around 2.0 are highly desirable. Unfortunately, only a few materials combine thermal stability with low dielectric constants. Among them are fluorocarbons such as polytetrafluoroethane (PTFE, Teflon®) and the recently introduced amorphous Teflon® AF. PTFE in its bulk form has many drawbacks such as insolubility, very high CTE (>300 ppm/°C) and marginal mechanical properties. Composites of PTFE with inorganic fillers, usually quartz (available from Rogers Corporation), have interesting properties. However, standard processes such as spin application cannot be used. The amorphous fluorocarbons, Teflon® AF, are soluble in perfluoro solvents. Their dielectric constants, about 1.9, are very desirable. However, their T_gs (160°C and 240°C respectively) are too low for most practical MCM applications. Moreover, adhesion of these materials to metal is poor and their adhesion to SiO_2 degrades rapidly in the presence of water. However, adhesion of metal deposited onto these dielectrics is good.

8.5.4 Benzocyclobutenes

Benzocyclobutenes (BCBs) are the most recent addition to the growing number of dielectrics intended for the electronics industry. Currently, only one material is commercially available from Dow Chemical (Table 8-15). It contains divinyltetramethyl disiloxane (DVS) and is called DVS-bis-BCB. BCBs have very intriguing properties such as excellent planarization and low dielectric constant (2.65). However, they are plagued by low oxidation stability in air (at 150°C). The commercial product contains an antioxidant to alleviate this problem. The thermal stability of BCBs in nitrogen is good at 300°C but at 350°C weight loss is 1 wt.-%/h. Because these materials are new, further developments can be expected.

8.6 SUMMARY

Polymeric dielectrics offer very low dielectric constants as well as ease of processing and, therefore, are ideally suited for interlayer dielectrics in MCM

structures. However, the choice of polymeric material is limited by the demanding thermal stability requirements. The most widely used materials, polyimides, usually require complex curing schedules which determine the ultimate properties of the polymer. The final film properties (CTE, elongation at break, modulus) can depend also on film thickness and, in some cases, on the nature of the substrate. These dependencies are still not well understood. PSPIs are still in the early stages of development although some use has been reported. Processing advantages are a strong driver for their further development. Very low dielectric constant materials (< 2.5) are currently just below the necessary thermal properties for high performance computer MCMs. The application of BCBs is limited to processing in nitrogen below 350°C and below 150°C in air. Finally, it must be stressed that many aspects of polymer dielectrics for packaging applications are not well understood and are the subject of intense research.

Acknowledgments

We would like to thank Gareth Hougham and Jeff Hedrick as well as many other of our colleagues for sharing and discussing their data and knowledge. We also thank our management at IBM for allowing us to undertake this project.

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9

CHIP-TO-SUBSTRATE (FIRST LEVEL) CONNECTION TECHNOLOGY OPTIONS

9.1 INTRODUCTION [1]

The selection of a first level connection technology for the connection of die to the multichip module (MCM) package or substrate involves several factors, each of which should be evaluated for specific MCM applications. This chapter discusses the basics of the three most widely used connection technologies, and together with die attachment, assesses their applicability to specific MCM constructions.

When choosing a chip connection technology, tradeoffs must be made between performance, density and cost. Performance here is defined as electrical (speed, design, testability) and mechanical (thermal dissipation, reliability, rework, repair). Density is related to chip size versus I/O count and chip to chip spacing on the module, both of which contribute to the overall size of the MCM.

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[1] Editors' Note: The sections in this Chapter form the focus for individual author contributions. The Chapter as a whole, and the Introduction and the Summary were assembled by the Editors with written technical contributions by S. Bezuk, E. Larson and D. Haagenson. These authors and the editors appreciate also the helpful discussions pertaining to the chapter as a whole from C. C. Wong and T. Dixon Dudderar, AT&T Bell Laboratories.

Cost is the MCM unit cost which includes: chip and substrate costs, device preparation costs, manufacturing equipment costs and process costs related to cycle time and yield. Each process contains specific costs covered in the following sections of this chapter. The goal is to provide a marketable MCM product that is competitive in all these areas. To accomplish this goal, a thorough evaluation must be made during the MCM design phase to determine the correct connection technology selection(s) for particular MCM products.

9.1.1 Chip Connection Technologies

The three most prominent first level connection technologies discussed in this chapter are:

1. Wire bonding
2. Tape automated bonding (TAB)
3. Flip chip solder bump (FCSB)

These technologies also have been defined in Chapters 1 and 2. MCM designs may require one or more of these technologies to exist on the same module.

Wire bond is the oldest and most mature of the chip connection schemes. A die is attached rigidly to the surface of the package or substrate and each bond pad of the chip is individually connected to a corresponding pad on the package with a small (usually 1 - 2 mil diameter) wire. Wire bonding is discussed in detail in Section 9.3. TAB is a process that connects a chip to metal traces patterned in a metal frame or adhered to a polymer. Cutting or excising the chip from the frame with the metal leads attached then allows for its placement and attachment to the substrate. TAB comes in several varieties and is discussed in Section 9.4. Conventional TAB is similar to wire bond in that the chip is face up on the substrate. Flip TAB places the chip face down, presenting the back of the die for chip cooling and short TAB leads for better electrical performance. Placing the die in a cavity also can provide shorter TAB leads and permit the heat to be removed through the back of the die and substrate. Wire bond and TAB both use peripheral pad layouts (except for array TAB), limiting the I/O capabilities of these technologies. FCSB, on the other hand, uses an array of solder balls on the I/O pads of the chip to provide a soldered chip connection to the substrate. It has the shortest chip-to-substrate connection and also presents the back of the die for cooling. Controlled Collapse Chip Connection (C4), used by IBM since the 1960s, is one example of FCSB. Another example of flip chip includes the use of conductive polymers as the connecting medium. FCSB technology is discussed generically in Section 9.5 and a case study related to C4 is presented in Section 9.6.

Each of these chip connection technologies has advantages and disadvantages discussed in the chapter. Higher performance in any area generally means higher cost for the final package. Design issues must be considered carefully in choosing one technology over the other for a particular application. In some cases, a combination of connection technologies may be beneficial to maximize both the performance and cost of the final product.

9.1.2 Electrical Design

Design for electrical performance involves two areas of concern affected by the interconnection and packaging strategies. The first area of concern is I/O count versus chip and packaging density. The second area is pure electrical performance resulting from low resistance and inductance values.

When looking at the I/O capabilities of each of the available technology alternatives, the area array capabilities of FCSB offer the maximum number of connections for a given chip size. FCSB also offers the closest chip-to-chip spacing available, since no area is consumed around the periphery of the die. The maximum lead count available with TAB is approximately equal to those of wire bond but less than that for FCSB. TAB and wire bond also consume area outside the die for the outer connection points. This area varies with the selection of MCM materials and the resulting design constraints. The area required for these outer connection points is minimized if the pad pitch on the die is equal to the pad pitch on the substrate. Flip TAB designs can take advantage of these equal die and package pad pitches, resulting in shorter leads and in denser packaging of the die in MCMs.

When considering electrical performance in terms of RL properties, FCSB clearly has performance advantages relative to TAB and wire bond due to the very short connection length as discussed in Chapter 1. Since TAB leads generally have a larger cross section than wire bond wires, and TAB potentially can be designed with shorter lead lengths, TAB offers the next best performance electrically. One of the main disadvantages of wire bonding is the potentially high RL properties of the wires when compared to FCSB or TAB connections.

Electrical testability and burn-in are other areas of electrical design that should be considered. TAB offers the potential for testing and burn-in prior to committing the die to a substrate or module. Wire bond and FCSB chips must be committed to the module before the primary chip connection is tested, and before the chip is burned in.

9.1.3 Mechanical Design

Chip connection technologies serve to connect the chip electrically to the MCM substrate but they also can provide all or part of the mechanical connection to

the substrate. The mechanical connection gives rise to reliability concerns. Stresses are generated when materials with different coefficients of thermal expansions (CTE) are joined together. Differences in CTE, due to the use of different materials, limit the chip size and I/O count for FCSB when different substrate and die materials are used, for example, silicon die on ceramic substrates. Substrate materials that have a CTE value closer to silicon generally are more expensive.

Cooling MCMs is another tradeoff in mechanical design. The denser the circuits are packed and the higher the chip operating power, the more heat is generated and must be dissipated per unit area. Each of the connection technologies allows different configurations for removing heat from the die. Mounting the chip face up, as with wire bond and conventional TAB, allows heat to be removed through the substrate. When designing with this in mind, the die bonding adhesive must be considered, since it contributes to the overall value of thermal resistance. For some conventional TAB applications, the TAB leads provide adequate structural strength, but an adhesive must be used between the die and substrate for thermal reasons only. Mounting the chip face down as with flip TAB and FCSB provides the back of the chip for heat removal. This can be very efficient but much more expensive. These package or MCM enclosures can be very dependent on particular designs.

9.1.4 Technology Comparisons

The maturity of the technology and the infrastructure existing in the industry are important issues. Wire bond is the oldest technology and is in widespread use. The process is well understood and documented. Equipment is available from many companies to support the technology. Chips and substrates can be purchased and used with none of the extra processing (bumping) required for TAB and FCSB designs. TAB is the second most widely used technology. This process, developed to speed the connection production process because of the ability to bond all the leads at once (gang bonding), is actually more involved than that for wire bonding. However, the intermediate step of attaching the chip to the TAB tape (Inner lead bonding - ILB) can allow for the testing and burn-in of the chips at this stage. Equipment and process information is available for TAB, but the infrastructure is less developed than that for wire bonding. Equipment, TAB tape and special chip bumping costs generally make this technology more expensive for low volume MCM applications. High volume production is required to make the bonding speed and testability of TAB pay off. FCSB, although it has been around since the early 1960s, has been championed by relatively few companies, most notably IBM. For all its longevity, FCSB is the least mature chip connection technology available on the open market. When

chips are available in solder bumped form, from commercial chip vendors, this technology will attain its full potential.

Process yield and repairability are two major factors determining MCM cost. Repair is considered an absolute must for most MCMs. A finished MCM represents a significant monetary investment when compared to a single chip package. All of the chip connection technologies described in this chapter are repairable to some extent. A wire bond repair requires the manual removal of the die and all connected wires before the chip is replaced, and therefore becomes much less desirable as I/O counts on the chip increase. TAB and FCSB processes, on the other hand, lend themselves to less labor intensive and potentially more automated repair processes. This is especially true for solder metallurgies, where all the leads or bumps on the die can be reflowed simultaneously, allowing for one step removal of the failed device.

9.2 DIE BONDING AND PHYSICAL ATTACHMENT

Robert E. Rackerby

Die attach, the process by which the die is anchored to the substrate, is usually the first process performed in the assembly of microelectronic packages. Historically, the mission of single chip die bonding was to secure the die and provide a controlled electrical and thermal path to the substrate. This was accomplished by introducing an adhesive, usually a silver-filled epoxy or solder, between the die and substrate. The metal content or composition of the adhesive was manipulated until the desired thermal or electrical parameters were obtained. Die bonding is currently done [1] via two technologies: through the introduction of an adhesive between the die backside and substrate or by an electrical connection procedure, such as tape automated bonding (TAB) or solder bumping (see Figure 9-1), and the descriptions in Sections 9.4 and 9.5. In this section, we limit the discussion to those processes involving an adhesive between the backside of the die and the substrate.

The demands of MCMs have changed the conventional view of die attach. The complex interaction of materials, processes and cost often forces MCM designers into difficult processing tradeoffs. Frequently the die bonding material for an MCM is required to perform many different tasks which never were required for single chip applications. Rework is a primary example of a new addition to the list of bond material requirements. In the past, failures after die bond were not catastrophic because the individual part cost was low. Most high performance MCMs are quite expensive and require the ability to rework individual chip sites to remain cost effective.

9.2.1 Die Attach Material Choices

There are two classes of adhesive available for die bonding: organic and inorganic materials. These materials are divided further into their components as listed in Table 9-1. The inorganic materials, Au-Si eutectic, silver-glass pastes and soft solders have the benefits of low contamination byproducts (moisture or corrosive compounds), but suffer from relatively high processing temperatures. Some of the soft solders also suffer from fatigue problems [2] - [3]. The organic compounds, on the other hand, have nearly the opposite characteristics. Organic compounds are effective materials for use on large die because they easily withstand large strains, but may be inappropriate for hermetic environments due to outgassing.

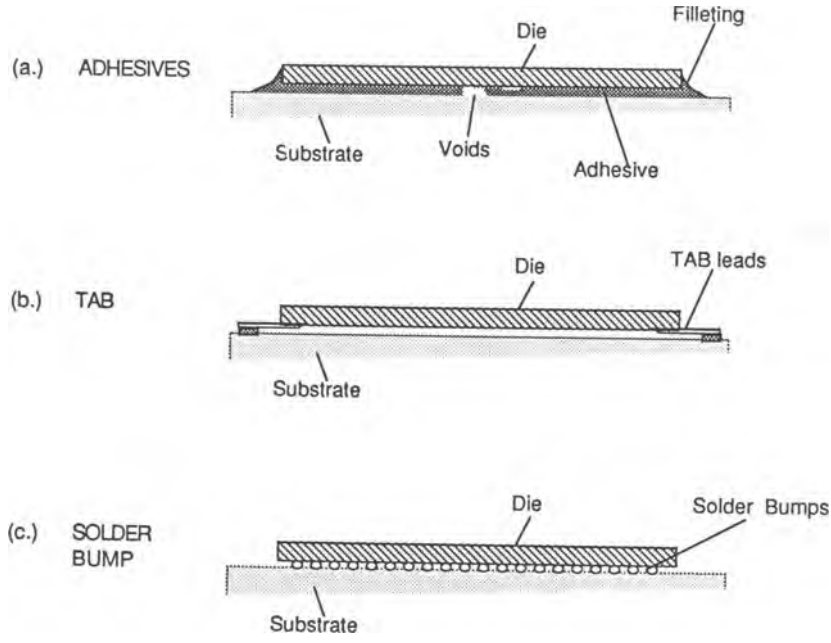


Figure 9-1 Die attach techniques showing two classes of die attachment: adhesive and electrical. Figure 9-1a Showing die attachment to substrate with adhesive. Figure 9-1b and 9-1c show an electrical connection method for mechanical attachment.

There are two classes of organic adhesives used for die attach, thermosets and thermoplastics. The thermoset compounds are characterized by epoxies and a few polyimide compounds. After they are cured, they remain solid with temperature increases up to their decomposition temperature. In contrast, thermoplastic compounds can be melted repeatedly to a liquid and resolidified with few or no side effects [4]. Thermoplastics decompose when heated past their boiling points.

Au-Si Eutectics/Silver-Glass Pastes/Soft Solders

The primary reason for choosing these materials is good thermal performance. High power applications have historically employed these materials. High processing temperatures [2]-[3], [5] usually rule out these materials for all but MCM-C. Rework is possible on an engineering basis with the eutectic and

Table 9-1 Inorganic and Organic Adhesives for Die Bonding.

DIE BONDING MATERIALS		
Inorganic Adhesives	Organic Adhesives	
	Thermoset	Thermoplastic
Gold-silicon Eutectic	Epoxy	Polyimide
Silver-glass Pastes	Polyimide	
Soft Solder Alloys	Urethane	
	Thermoset/Thermoplastic Mixtures	

solder materials, but is impossible with silver-glass. These constraints severely limit the usefulness of these materials.

The bonding mechanisms of the inorganic compounds are somewhat similar. The Au-Si eutectic and solder materials establish metallurgical bonds with the die and substrate [2]-[3], [5]. In the case of the Au-Si eutectic materials, a high degree of silicon diffusion from the die establishes a hard soldered joint [2]-[3]. Soft solders, containing some mixture of Pb, Sn, In, Ge or Ag, create a bond based on intermetallic formation [3]. However, the degree of silicon diffusion is somewhat less than with the Au-Si eutectic.

Silver-glass pastes bond by three mechanisms: metallurgical, chemical and mechanical. The metallurgical mechanism is accomplished by forming Au-Ag intermetallics between the gold plated substrate and the sintered silver matrix formed in the silver-glass paste [6]-[8]. The chemical mechanism is achieved by oxygen bonding between the metal oxides in the glass to the silicon on the backside of the die [2], [9]. Mechanical bonding takes place at both the backside of the die and the substrate when the glass re-vitrifies upon cooling [8]-[9].

Epoxies

Epoxies, like all the organic adhesives, are relatively easy to work with, are compatible with most surfaces and are amenable to rework. Epoxies (filled and unfilled) have a much broader use in the production of MCMs. In the last several years, epoxies have become clean enough for most MCM applications with the exception of some high reliability applications [2] found in the space or military industries.

Bleedout is a complication in the use of epoxies [10]-[11]. Bleedout is a condition characterized by resin flowing over portions of the substrate and coating unintended areas during the cure cycle. Experimental data indicate bleedout may be related to the surface energies of both substrate and resins [10]. Lack of surface cleanliness contributes to bleedout because it changes the surface energy of the substrate.

Chemically, epoxies are the dirtiest of the die bonding adhesives. The crosslinking agents, hardener and resin, react producing several byproducts in addition to the long epoxide chains. Ammonium hydroxide was a byproduct in the early development of epoxies. The ammonium hydroxide subsequently caused corrosion of the metal traces within the package. Advancements in epoxy technology have essentially eliminated this problem, leaving halogen and metallic cations such as Na^+ and K^+ present in minute concentrations (typically less than 10 ppm) [12] as dominant contaminants. Some epoxies may be suitable for environments requiring hermetic seals, however, they must be thoroughly tested and characterized for unwanted byproducts as a function of operating temperature.

The bonding mechanism for the epoxies is mechanical and chemical. When the epoxy cures, it undergoes a phase change and hardens. This phase change also establishes mechanical bonds where the epoxy sticks to microscopic fissures and crevices in the die and substrate. Chemical bonding, however, is responsible for the bulk of the joint strength. During cure, portions of the epoxy chains adhere to water adsorbed to the surface of both the die and substrate. The mechanism of chain attachment is through Lewis acid-base charge transfer [2]. The epoxy chains become electron acceptors while the surface film of water acts as electron donors. The bond sites for the epoxy chains are present uniformly across both the substrate and die.

Polyimides

Polyimides have processing characteristics similar to that of the epoxies [2]. However, they tend to be more thermally stable than the epoxies [4]. Filling polyimides with metals, such as silver or copper, tends to lower their thermal stability [13]. Polyimides can be formulated as either thermoplastics or thermosets. The condensation cure mechanism produces a thermoplastic compound whereas addition curing yields a thermoset [14]. Polyimides for die attach are chemically similar to thermoplastics, both have the ability to be remelted and cured (solidified) repeatedly [4]. Polyimides also are less susceptible to bleedout than the epoxies.

The polyimides are the cleanest of the organic adhesives for die bonding and are comparable to Au-Si eutectic attach [15]. Their major drawback is a tendency to absorb water (as much as 6% by weight). Measures to ensure

against moisture induced failures include extra drying steps or inclusion of a desiccant. Polyimides adhere to surfaces through chemical and mechanical bonding similar to the mechanism for epoxies [2].

Thermoplastics

Thermoplastics have been used recently for die attach because of their ease of rework and their low glass transition temperature, T_g [4]. The adhesive is applied either as a hot melt or in a preform which is heated to its melting point and allowed to cool after die placement. Thermoplastics do not have high bond strengths and remain quite flexible or ductile relative to thermosets [4]. These properties make them less desirable as die bonding adhesives because they are less likely to pass the adhesive strength specifications required in the Mil-specs.

The bonding mechanisms for the thermoplastics are mechanical in nature, although chemical bonding can take place as well. The hot liquid penetrates the rough microstructure and, upon solidification by cooling, locks the die in place.

Mixtures and Organic Alloys

Mixtures of thermoset and thermoplastic materials represent a relatively new category of adhesives. The purpose of mixing these two polymers is to attempt to blend the best material properties of each into a single compound. The blend is accomplished by either mixing existing polymers together by blending (sometimes called alloying [16]) or chemically grafting the desired functional group to the backbone polymer. The chemical grafting technique holds the most promise for producing a material with desired properties.

9.2.2 Die Attach Processes And Process Control

The die attach process can be broken down into three steps:

1. Dispensing of the adhesive
2. Alignment and placement of the die
3. Curing of the adhesive

In the first step, the adhesive is dispensed in an amount which ensures the proper bondline (thickness of the cured adhesive under the die). Au-Si eutectics, solders and several of the organic compounds are dispensed using a rigid preform. The alternative to using preforms is using a low viscosity paste. All the organic materials are available in a paste or liquid form.

The second step of the process includes die alignment and placement. The die is acquired from its carrier and properly oriented. The die is placed onto the adhesive and set in place producing a fillet of material around the edge of the

Table 9-3 Parameters Associated with Die Bonding Quality Control.

DIE BONDING PROCESS PROBLEMS					
	Dispense	Place	Package Handling	Cure	Rework
Low Bondline	X	X			
Edge Voids	X	X			
Undercutting	X	X			
Material on Die	X	X		X	
Overfilling	X	X			
Flaking	X				
Bridging	X				
Cracking			X	X	
Disbanding			X	X	
Bleedout				X	X
Misorientation Misalignment		X			
Die Chips/Scratch		X	X		

for bonding organic adhesives is different than that used for bonding silver-glass pastes. Machines used to dispense silver-glass pastes have mixers and sophisticated pressure dispensers which are unnecessary on epoxy machines.

Curing of adhesives is usually the easiest to perform and control. It is necessary to control time, temperature and environmental parameters such as humidity or air flow rate.

Quality Control Parameters

Table 9-2 depicts the die bonding process and the list of parameters needing process control. Tables 9-4 through 9-6 compare each control property for each material choice (organic and inorganic). The tables show relative difficulty for controlling each property.

Consider Table 9-4, which shows the relative ease of control for die adhesive dispense parameters. Notice that the paste-based materials (silver-glass

Table 9-4 Relative Ease of Control of Adhesive Dispense Parameters.

ADHESIVE DISPENSE CONTROLLABILITY							
Property	Au-Si Eutectics	Ag-glass Paste	Solder	Epoxy	PI	TP	M
Quantity	3	1	3	2	2	2	2
Uniformity	3	1	3	2	2	2	2
Consistency	3	1	3	2	2	2	2
Pot life	1	1	2	1	1	2	1
Bondline thickness	3	1	3	3	2	2	2
1 = DIFFICULT 2 = MODERATE 3 = EASY							

PI = polyimide TP = thermoplastic M = mixture

and organics) are more difficult to control than the metallic preforms (Au-Si and solder). Silver-glass pastes are the most difficult to dispense and control. Because of the degree of fluidity of the Au-Si or solder metals, excess material is not likely to impact the overall result as is the case with the organic adhesive. Pot life is a concern with all the materials. As the adhesives sit around prior to use, controlling their environment is important, especially with the thermoset compounds. Oxidation of the solder compounds has an impact on the overall strength of the resulting bond. In the case of Au-Si eutectics, oxidation on the backside of the die creates difficulty in achieving a proper bond. Formation of the eutectic melt is hindered.

The complexity of the MCM determines the overall importance of the die alignment and placement step. Table 9-5 compares the level of difficulty encountered during die placement. Because the eutectic and solder processes usually are done manually, controlling these parameters is difficult. The process for silver-glass pastes is difficult to control because of its stringent bond thickness requirement. Silver-glass pastes shrink upon firing which impacts die alignment accuracy and repeatability. The organic compounds are all easier to control at this step than the inorganics. In MCMs, where the placement requirement is stringent, organic materials may be the only materials.

In Table 9-6 the process parameters for adhesive cure are addressed. Adhesives which require a separate cure usually can be cured in one step. The exception, silver-glass pastes, is due to the fact that its firing profile tends to

Table 9-5 Relative Ease of Control of Die Alignment and Placement.

DIE ALIGNMENT AND PLACEMENT CONTROLLABILITY							
Property	Au-Si Eutectics	Ag-glass Paste	Solder	Epoxy	PI	TP	M
Placement Accuracy	1	1	1	2	2	2	2
Repeatability	1	1	1	3	3	3	3
1 = DIFFICULT 2 = MODERATE 3 = EASY							

PI = polyimide TP = thermoplastic M = mixture

Table 9-6 Relative Ease of Control of Adhesive Cure.

ADHESIVE CURE CONTROLLABILITY							
Property	Au-Si Eutectics	Ag-glass Paste	Solder	Epoxy	PI	TP	M
Time-temperature	2	1	2	3	3	3	3
Environmental	2	1	2	3	3	3	3
Shrinkage	3	2	3	2	2	3	3
Electrical Test	3	3	3	3	3	3	3
Mechanical Test	3	3	3	3	3	3	3
Inspection	3	3	3	3	3	3	3
1 = DIFFICULT 2 = MODERATE 3 = EASY							

PI = polyimide TP = thermoplastic M = mixture

have several temperature plateaus. Environmental control (atmosphere H_2, N_2 or humidity) is important for the success of the inorganic materials. Again, the eutectic and solder materials are moderately easy to bond and control because of their manual nature.

9.2.3 Die Attach Equipment

Selection of die attach equipment depends on the degree of control needed in the process. MCMs are designed usually with very tight tolerances requiring tight die attach tolerances. The small volume production lot sizes typical of MCMs requires even greater machine flexibility.

MCM-C and MCM-D are likely to be found in low volume, custom part strategies, such as high performance computer systems. MCM-L is likely to be found in high volume applications such as consumer electronics (pocket calculators, cameras, etc.). Trends in die bonding systems are towards higher computerization, automation, robotics and integration [17]. Recent advances have pushed machine-attributable defects below current visual inspection screening ability [17].

9.2.4 Issues for MCMs

Manufacturability and Rework

Reworkability is an important consideration in the manufacture of MCMs because of their cost. Reworking MCM-C and MCM-L is comparatively easy. By choosing organic materials for die bonding, it is possible to manage both the temperature processing hierarchy and material interaction issues. In some cases, it is possible to mix die attach materials to optimize performance and cost. For MCM-C, silver-glass paste materials are used on the high power components of the MCM while organic adhesives are used for the lower power dice (see Figure 9-7). The resulting module may be hermetically sealed provided the epoxy die attachment can withstand the process temperatures required for sealing.

Organic bond adhesives are the only choice available for the MCM-L structure. The inorganic adhesives require process temperatures, usually too high for the resin-based substrates. Solders may be sued in MCM-L for die attach, but care should be taken to ensure it is not accidentally reflowed in later phases of assembly. A bonding material must be chosen whose processing temperatures do not irreversibly distort a resin-based MCM-L substrate. Adhesives with high T_g temperatures or high melting temperatures are unacceptable. The thermoplastics and alloyed organic adhesives are better choices especially if rework is desired because of their low process temperatures and low T_g.

Fabrication of MCM-D structures is mostly compatible with organic adhesives as well. Polyimides are used frequently as dielectrics in the fabrication of MCM-D substrates. It is necessary to consider the materials brought in contact with the polyimide because of its propensity to absorb moisture and epoxies susceptibility to outgas it. These two materials may be incompatible for

hermetic applications. In situations where encapsulants are used to protect the die, epoxies and polyimides may prove compatible.

The easiest MCM to rework is MCM-C followed by MCM-L, with MCM-D being the most difficult. All organic adhesives are reworked readily with MCM-C, even some of the inorganic materials can provide a limited degree of rework coverage. MCM-L and MCM-D are best served by the thermoplastics and polyimide compounds as shown in Table 9-7.

The major cause of rework is defective die. Electrical defects in the die are detected during functionality tests during manufacture. There are several types of defect which render a module unrepairable or rejected. The most common defect in this category is bleedout onto adjacent bond pads. The cured resin is not removable without damaging either the substrate or the other good die in the module.

Failure Mechanisms and Reliability

Many tests are available to analyze the susceptibility to failure for an MCM. Table 9-8 indicates seven of the most frequently used analytical techniques for characterizing adhesives in electronic packaging. In addition to these basic analytic techniques, there are environmental and mechanical stress tests to perform. These tests have their origins in military specifications. Current stress tests are applicable mostly to single chip packaging implementations. MCMs tend to be significantly larger than single chip packages making existing stress tests very harsh on MCMs. Because the Mil-specs are stringent, a few organizations have attempted to write commercialized versions with relaxed endpoints. These efforts have generally been passed over in favor of using the more universal and familiar Mil-specs. The issue of relaxed endpoints for stress tests on MCMs or MCM specific stress tests must be addressed by industry. Some environmental stress tests with practical application in MCMs are described in Table 9-9.

The usual procedure for testing an MCM is to characterize materials in their cured and uncured states using some of the analytic testing techniques (Table 9-8). Some environmental and mechanical stress tests (Table 9-9) can be performed and the results evaluated by using the analytic tests again (Table 9-8). Comparisons can be made among the different materials as a function of different cure procedures. The information gained in stress testing can be used to predict failure modes and estimates of failure rate. A list of failure modes and the tests likely to predict them is given in Table 9-9.

The overall reliability of an MCM is a function of failure mode coverage. Designs that account for the worst failure modes do better than designs that do not. Mechanical failure modes such as delamination or disbanding are handled through material selection which minimizes high temperature exposures during

Table 9-7 Relative Ease of Reworkability for MCM Technologies.

REWORKABILITY							
Property	Au-Si Eutectics	Ag-glass Paste	Solder	Epoxy	PI	TP	M
MCM-C	0/1	0	0/1	3	3	3	3
MCM-L	0	0	0	2	2	3	3
MCM-D	0	0	0/1	1	2	3	2
0 = IMPOSSIBLE 1 = DIFFICULT 2 = MODERATE 3 = EASY							

PI = polyimide TP = thermoplastic M = mixture

Note: Inorganic adhesives generally are not amenable to rework.

Table 9-8 Analytical Characterization of Adhesives Used in Die Attach.

ANALYTICAL TESTING SERVICES	
DSC Differential Scanning Calorimetry	Determination of % cure and T_g. Thermal stability, Reactivity. Phase change versus temperature.
TGA Thermal Gravimetric Analysis	Determination of % cure. Thermal stability. Reactivity. Weight loss versus temperature—Used in conjunction with DSC.
TMA Thermal Mechanical Analysis	Precise determination of T_g. Mechanical performance versus temperature.
RGA Residual Gas Analysis	Identification of impurity and gas composition in hermetic modules. Identification of breakdown products of organic adhesives.
SEM Scanning Electron Microscopy	Determination of failure mode, microstructure of die attach adhesives.
Die Pull	Adhesive strength.
Die Shear	Adhesive strength.

with little damage. MCM-L and MCM-D on the other hand contain intrinsic organic components. When removing the organic adhesive used to bond the die, it is possible to alter permanently or to contaminate the intrinsic organic components of the substrate.

9.3 WIRE BONDING

Erik N. Larson

Wire bonding has a long and successful history as a microelectronic connection method because of its ability to adapt to increasingly complex packaging challenges, its well established reliability, its infrastructure and its potential for low cost. Multichip Module (MCM) technologies are able to leverage the experience gained in both the semiconductor and the hybrid industries using wire bonding techniques. Several forms of the wire bonding process are being used for various single chip and multichip applications. The first objective of this chapter is to supply information to potential users which enables them to decide if a specific wire bonding connection process is appropriate for their MCM application. The second objective is to supply the user with the tools necessary to develop a successful MCM wire bond process. Additional information which benefits the user, including package design, wire bonding equipment, electrical performance, reliability and rework also is covered.

9.3.1 Wire Bonding Methods and Procedures

There are three fundamental wire bond methods which have been developed over the years in the semiconductor industry. These methods are identified as thermocompression (T/C), ultrasonic (U/S) and thermosonic (T/S) bonding. Several wire materials are available, but those used most commonly are gold and an aluminum alloy. Available bonding techniques are identified as "ball" and "wedge" bonding. A bonding process is defined as a combination of one of these methods with a technique. The characteristics of each method along with available processes are shown in Tables 9-10 and 9-11. The technique selected is normally a function of one or more of the following: package design and environment, desired wire density, production volume, surrounding package or module clearance and the metallurgical properties and characteristics of the wire. Common die and package or substrate metallizations are aluminum and gold. Successful wire bonding requires the die to be attached rigidly to the MCM substrate surface using suitable die attach materials.

Each wire bonding method involves three steps to bond the wire to a surface. Initially, there is an applied force holding the wire firmly against the bonding surface. The second step involves the application of bonding energy. To form the thermocompression bond, thermal energy is used. For the ultrasonic bond ultrasonic energy is used and for the thermosonic bond, combined thermal and ultrasonic energies are used. Wire flow during the weld to the bonding pad

Table 9-10 Comparison of Wire Bond Methods.

METHOD	COMMON METALLURGY	TEMPERATURE	PRESSURE	TIME
Thermo-compression	Au wire Al or Au pad	300°C - 400°C	High	High (40 ms+)
Ultrasonic	Al alloy wire Al or Au pad	Ambient	Low	Low (20 ms)
Thermosonic	Al wire Al or Au pad	150°C - 225°C	Low	Low (20 ms)

Table 9-11 Comparison of Wire Bond Processes.

PROCESS	COMMON WIRE/PAD METALLURGY	AVAILABLE SINGLE ROW PAD PITCH	APPROX. MACHINE SPEED
Thermocompression Ball	Au wire Al or Au pad	4.0 mil	2 wires/sec
Ultrasonic Wedge	Al alloy wire Al or Au pad	3.0 mil	4 wires/sec
Thermosonic Ball	Au wire Al or Au pad	4.0 mil	10 wires/sec
Thermosonic Wedge	Au wire Al or Au pad	3.0 mil	3 wires/sec

is achieved, in all cases, by a combination of applied force and applied energy. Material flow during the application of bond energy is responsible for generating a clean interface at the bond zone, which is required for the weld to occur. Many high reliability wire bonding processes include a plasma bond pad cleaning prior to wire bond to enhance bondability and reliability at the interface. The third parameter is the bond time that energy and force are applied. Table 9-10 shows the relative parameters and materials for each wire bonding method.

Wire bonding uses a range of bonding wire diameters from small (< 25 μm, sometimes termed fine wire) to large (> 500 μm) wires. The larger wire (> 75

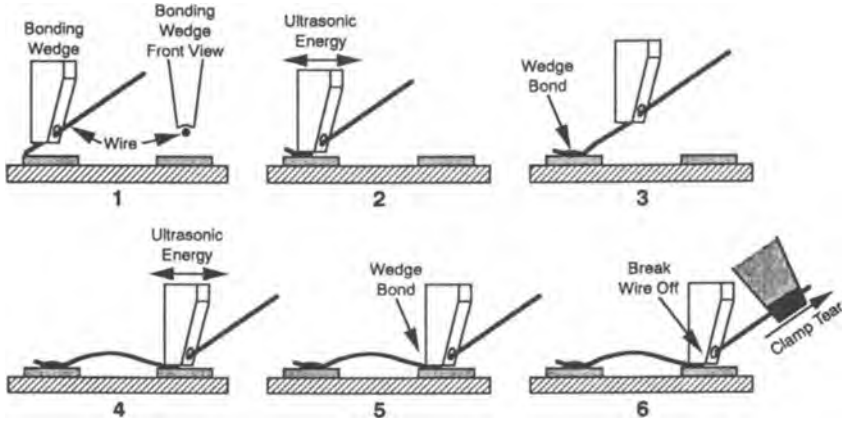
μm) is used primarily for power devices with relatively low wire counts and coarse pad pitches (> 10 mils).

Ultrasonic and Thermosonic Wedge Bonding

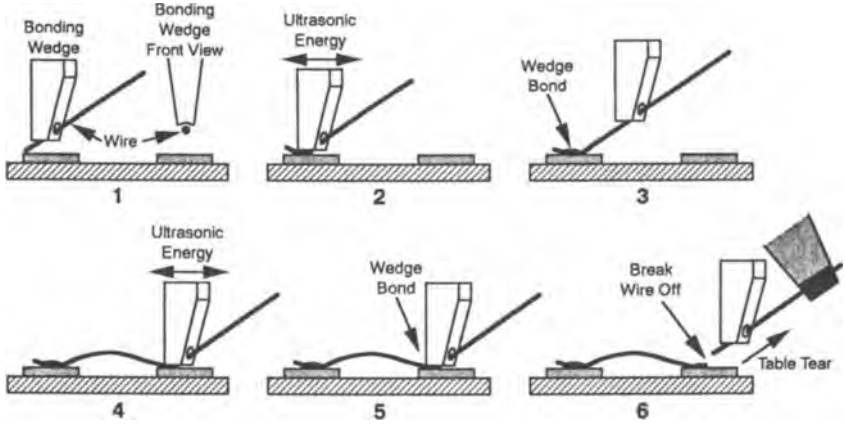
The wedge bonding technique is used for both ultrasonic aluminum wire bonding and thermosonic gold bonding processes. Ultrasonic wedge bonding is a low temperature process (typically at ambient temperature) in which the welding is accomplished by force and ultrasonic energy. The stages of the ultrasonic wedge bonding process are shown in Figures 9-2a and 9-2b. The ultrasonic energy at a frequency of about 60 kHz is applied to a wire, held in contact with a bonding pad by the wedge, or bonding tool. The combination of pressure and ultrasonic energy forms a metallurgical weld without the addition of significant thermal energy. The thermosonic gold wedge bonding process basically is identical to ultrasonic aluminum, with the addition of component heating. The most common wedge bonding process is ultrasonic aluminum. And the major reason is the lower process cycle time, and the reduced equipment complexity achieved with the absence of component heating. In some cases, there can be favorable metallurgical combinations gained by using aluminum wire.

Normally, the first bond is made to the die and the second bond is made to the MCM substrate. This is referred to as forward bonding. It is preferred because it is far less susceptible to edge shorts between the wire and die. This is discussed in more detail later. The procedure for ending the wire after the second bond takes several forms. For the small wire (25 - 50 μm), clamps can be used to break the wire after the second bond while machine bonding force is maintained on the second bond (clamp tear, see Figure 9-2a), or the clamps can remain stationary and the bonding tool can be raised off the second bond to tear the wire (table tear - see Figure 9-2b). The clamp tear process typically offers a slightly higher yield and reliability potential than the table tear process due to the force maintained on the second bond during the clamp tear motion. The clamp tear process also offers a slight speed advantage over the table tear process due to fewer required table motions. However, the table tear process, with a higher wire feed angle capability and a stationary clamp, has the potential to provide slightly more clearance from package obstructions such as a bond shelf or pin grid. The metallurgical characteristics of the ultrasonic wedge bond are shown in Figure 9-3. For large wedge bonding wire (> 75 μm), other methods have been used such as a cutting blade or the placement of the wire into a channel in the wedge for wire termination.

The wedge bond configuration shown in Figure 9-3, is characterized by a directional first-to-second bond alignment. The toe of the bond is the end nearest the severed wire while the heel is at the end of the bond where the wire bends from the bond surface. A negative feature of the wedge bonding



(A)



(B)

Figure 9-2 (a) Wedge bonding - clamp tear process. (b) Wedge bonding - table tear process.

technique is the design and machine demands required to maintain this directional first-to-second bond alignment. The requirement to rotate and align the die and substrate with the direction of the wire can restrict the use of wedge

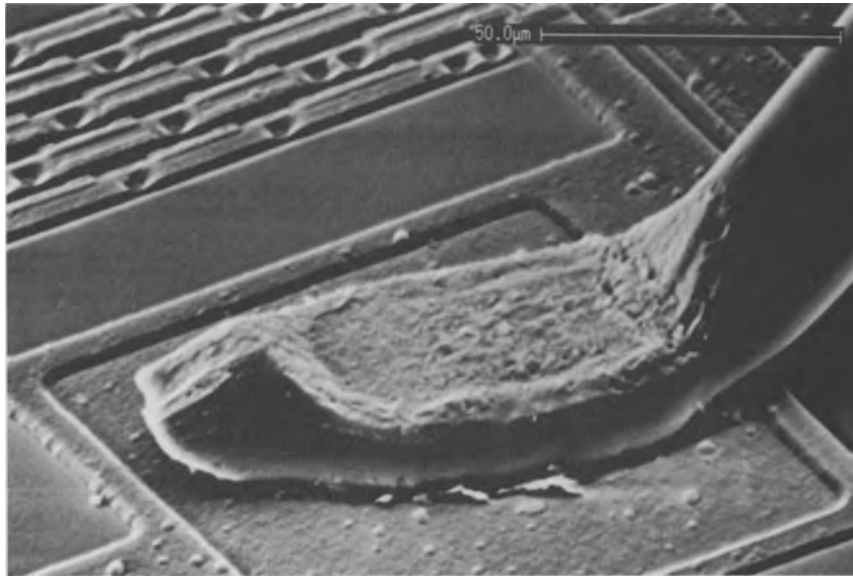


Figure 9-3a Features of the ultrasonic aluminum wire bond to the device. There is a tradeoff between bond development and wire deformation. The quality of the bond integrity cannot be determined from a visual examination of this type. Pull tests must be used to confirm bond strength.

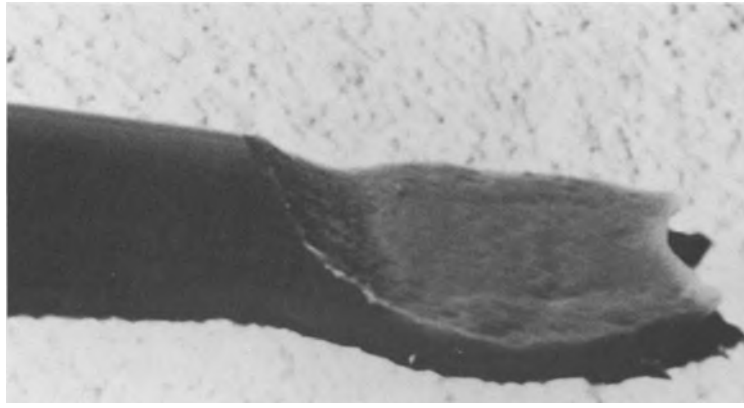


Figure 9-3b The major difference between the second bond and the first bond to the chip is the wire tear feature which is typical of a second ultrasonic bond. (Photos courtesy of Motorola.)

bonding on large MCMs (> 3 inches on a side) due to equipment limitations. An advantage of wedge bonding is the narrow bond configuration allowing a tight spacing between bonds. Aluminum wedge bonding has been demonstrated down to 75 μm by the author. In summary, the ultrasonic and thermosonic wedge bonding processes have the advantage of allowing a small bond pad pitch. However, factors based on machine rotational movements make the overall speed of the process less than that of thermosonic ball bonding.

Thermosonic Ball Bonding

Currently, thermosonic ball bonding operations almost always use gold wire. Relatively small wires (< 75 μm) are used, so that the capillary tool can sufficiently deform the second bond for easy wire separation. The thermal bond (thermocompression or thermosonic) is normally a ball bond process for the first bond position at the die. Originally the ball was formed by using a hydrogen torch, but modern bonders use an electric flame off (EFO) to melt a small portion of the wire extending beneath the capillary. Figure 9-4 shows the stages of the thermosonic ball bonding process. In Figure 9-5, ball bond features for both the first and second bond positions are shown. The vertical nature of the ball bond at the die reduces the possibility of edge shorts to the die. At the outer lead bond, the capillary leaves a characteristic circular pattern termed a crescent

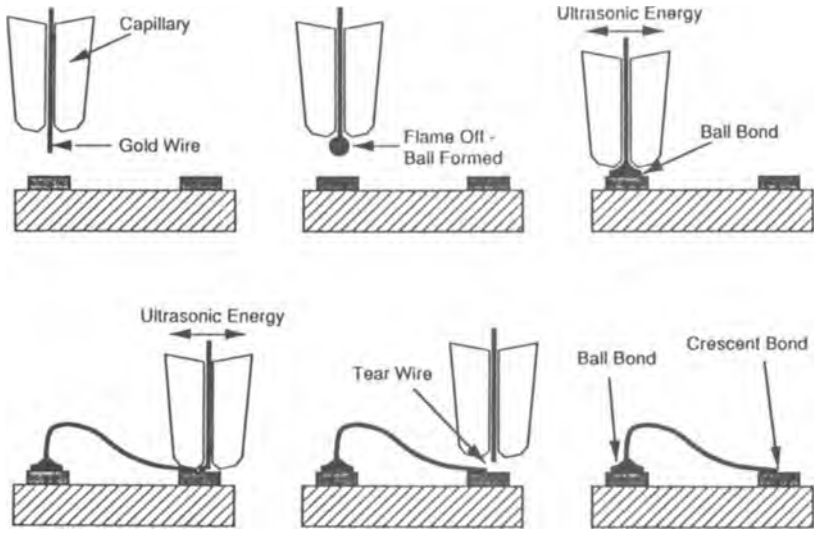


Figure 9-4 Thermosonic ball bonding process.

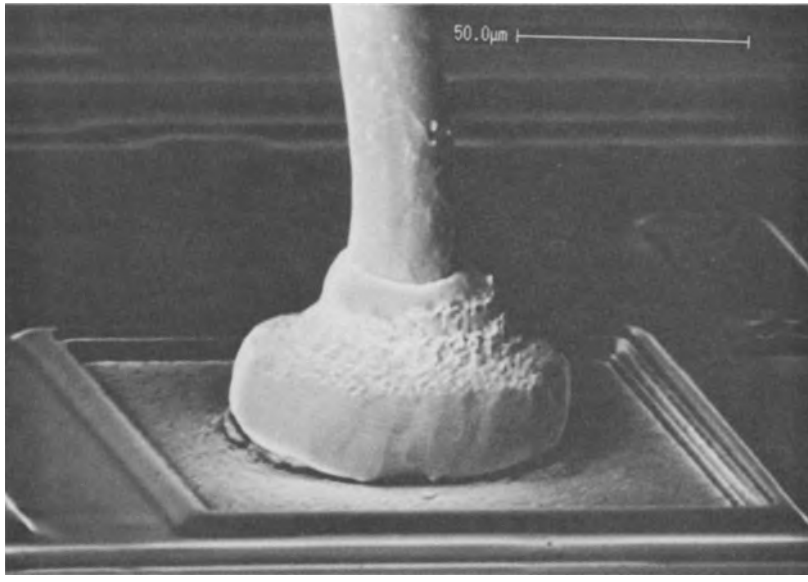


Figure 9-5a Features of the thermosonic ball bond to the device. Shear testing of the ball structure to the pad is becoming a standard method of bond quality evaluation.

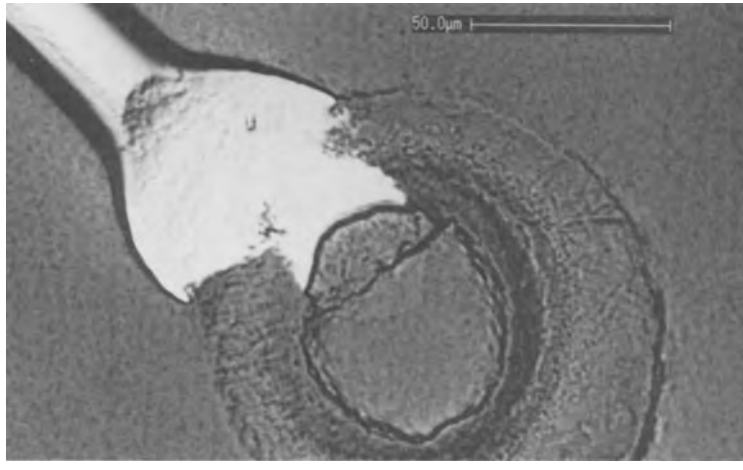


Figure 9-5b Unlike the ultrasonic bond method, the second bond of the "ball bond" method is distinctly different in appearance from that of the first. This is called a "crescent" bond. (Photos courtesy of Motorola.)

bond. The highly flowed gold in this second bond area generates a clean surface area for good interfacial atomic bonding. Once again, precleaning with a plasma process often is used to enhance the reliability of the interface. The round configuration of the first bond allows bonding machine motion to be made very rapidly in any direction. Modern automated wire bonders provide highly controlled targeting accuracy to the center of the bond pad for both ball and wedge bonding. The major pad pitch limiting feature of the ball bond method is the capillary as shown in Figure 9-6. Ball bonding is generally used in applications where the pad pitch is greater than 100 μm.

Thermocompression Ball Bonding

Thermocompression bonding is conceptually the simplest of the wire bonding techniques. Gold wire is used most commonly and deformed plastically by pressure and by bonding surface heat (300°C - 400°C) to form a metallurgical weld with the aluminum or gold bond surface. The high temperatures and long bond times required for thermocompression bonding have reduced its popularity since the development and integration of ultrasonic energy in assisting bond formation.

In summary, of the wire bonding alternatives, thermosonic ball bonding is expected to constitute the greatest wire bond MCM product volume. The vertical feed and looping features of ball bonding enable it to provide the highest chip to chip placement density. The reduced die pad spacing capability and potential metallurgical advantages of aluminum wire promote the ultrasonic wedge bonding process. It also eliminates another concern with ball bonding - the complexity of applying thermal energy to advanced MCM substrate materials and configurations. In low cost MCM applications where glob top encapsulation is used, gold wire has established excellent reliability. This is due to the high strength and ductility of the gold wire.

9.3.2 Wire Bonding Processes and Configurations: Geometry, Density and Package Design Considerations

Wire bonding has been adapted for a wide range of applications and, as a result, several single chip and MCM packaging geometries have been developed. The objectives of these various geometries are to increase chip and package density, electrical performance, and manufacturability while reducing cost. Wire bond density is limited mainly by its requirement for periphery I/O pads on the chip. The minimum I/O pad spacing on the chip results from adjacent pad metal reliability concerns, as well as from the limitations of test probing.

Differences in silicon and packaging manufacturing capabilities, in reliability concerns, as well as in the capabilities of test and assembly equipment, have

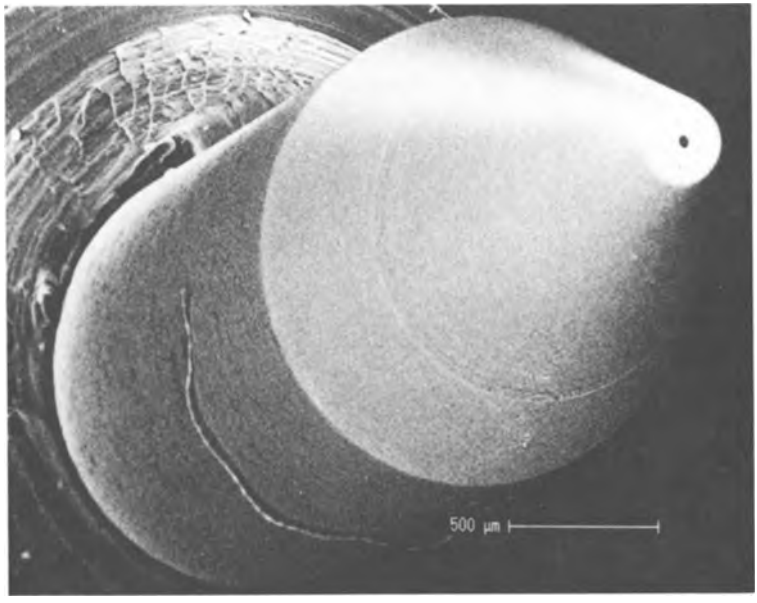


Figure 9-6a A capillary used for thermocompression bonding is shown mounted in the SEM fixtures. The size of hole for the wire is smaller than the capillary itself, yet in bonding, the capillary is not to contact previously bonded wires. The capillary diameter and not the wire diameter controls ball bond spacings.

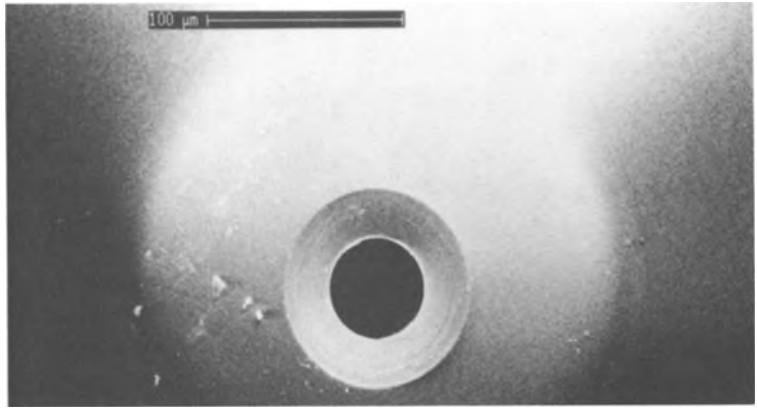


Figure 9-6b The capillary configuration at the wire exit region influences the shape of the ball bond. (Photos courtesy of Motorola.)

placed individual density limitations on each. As an example, cofired ceramic packaging technologies using screen printing have limited adjacent pad pitch to approximately 200 μm. On the other hand, chip wafer level test equipment capabilities have limited die pad pitch to approximately 85 μm. Therefore, to take advantage of the maximum densities of each, a fanout or pitch expansion method must be used. Some expansion techniques used are: multiple shelf ceramic PGAs with orthogonal and radial designs, and staggered multiple row package pads on a single shelf. Of the geometries developed, the most popular applications which use wire bonding are listed below:

- Single and multitiered cofired ceramic pin grid arrays (PGAs), single chip and multichip
- Ceramic and plastic quad flat packages (CerQuads and PQFPs)
- Chip on board (COB)

For these applications, the pad pitch on both the chip and package are being pushed downward as the wire count and I/O per device are being increased. QFP technology has been limited with this packaging technique to approximately 300 I/O, where multitiered package technology enables over 500 I/O. An example of where the high density available currently for both T/S-gold and U/S-aluminum wire has been useful is the Unisys MRAM multichip module with a 252-pin PGA package. Both the multichip module and the single chip package utilize a double shelf and radial fanout technique. Ultrasonic aluminum wedge and thermosonic or gold ball bonding can be used for the processor, which has 252 wires at 5.2 mil die pitch. The memory chips are bonded using a thermosonic gold ball bonding process.

Another example is a single chip, fine pitch 323-pin two-tiered cofired ceramic PGA package which incorporates a double shelf orthogonal design. 388 wires at 4.25 mil pitch were wire bonded on a 0.517" square CMOS die using ultrasonic aluminum wedge bonding with a 30 degree clamp tear process. The selection of a die pad pitch of 4.25 mils on the 323 PGA was based on studies using an experimental test vehicle designed to establish aluminum wedge bond process limitations. The test vehicle employed 3, 4, 5 and 6 mil die pad pitch, double shelf cofired ceramic package construction with an orthogonal wire layout.

As both MCM and single chip packaging density increase, the area surrounding the wire bond positions on the chip and substrate is reduced. This requires that the package designer and wire bond process engineer analyze both the constraints of the wire bond equipment and the process related issues with high density wire bonding. The dimensions of the wire bond machine hardware and the wire bond process motions are necessary to ensure a successful design

when developing a high density package or MCM. This information can be obtained through equipment vendors, or can be attained by direct equipment measurements. Once the machine dimensions and parameters have been established, the package designer can integrate these with the potential package variations to verify adequate clearance for a given wire bond process.

When designing an MCM, die attach area and placement tolerances should be analyzed to ensure adequate area for adhesive fillets, as well as adequate area surrounding the die. The reason for this is to provide adequate machine clearance as well as to protect the substrate or package wire bond pads from die attach foreign material contamination. Die attach material splattering, wicking or bleedout can contaminate bond pads and reduce the bondability or reliability of the surface.

When considering wedge bonding, there are several combinations of both the table tear and clamp tear processes which differ in both performance and clearance requirements. Table 9-12 shows clearance considerations for several available wire bond process combinations. Figure 9-7 shows a cross section of a typical multitiered, single chip ceramic package with the wedge-clamp-wire profile for ultrasonic wedge bonding. Wedge bonding can be used in either the forward mode (first bond on die, second bond to package or substrate), or reverse mode (first bond on package or substrate, second bond on die). The most common and preferred wedge bonding direction is forward bonding. This

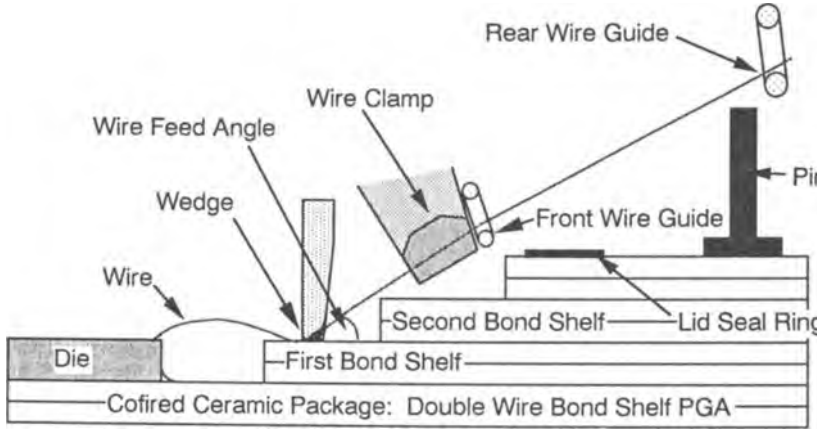


Figure 9-7 View showing wire bond clearance considerations for a typical cofired ceramic PGA.

is because forward bonding delivers wire loop shapes that provide more clearance from the edge of the die, preventing wires from edge shorting to active material or to the base silicon on the die periphery. Thermosonic ball bonding offers the most machine clearance, since there is no clamp mechanism below the transducer and the wire is fed vertically through the tool. For COB MCM applications, the spacing between devices, as well as the height of the devices, must be analyzed. If heat can be supplied through the MCM substrate, ball bonding can provide two advantages for these applications: reduction of die to die spacing because of the vertical wire feed and security from edge shorting. An example of this type of design is shown in Figure 9-8, where die are mounted on a thin film multilayer ceramic substrate. In this MCM example, thermosonic gold ball bonding is used to connect the chip pads to the to the thin film substrate pads. Also shown in Figure 9-8, are the thermosonic gold ball bonding looping profile features. A disadvantage of ball bonding with COB is the requirement and complexity of heating the board or substrate. The repairability and rework potentials of each process differ, and are discussed in a later section.

In a multitiered or multiwire length fine pitch application, wire-to-wire clearance should be analyzed to guard against shorting. Shorting may occur with one or more of the following: die shift, bond placement drift, loop variation (all due to machine accuracy and repeatability limitations) and package dimensional fluctuations. By combining empirical studies with theoretical modelling, wire-to-wire clearance can be analyzed. Wire loop shapes are determined by bonding to a test vehicle with equivalent geometry as the planned application. These wire loops can be cross sectioned, plotted and curve fitted using a representative polynomial equation. The curves then can be integrated into a three-dimensional algorithm which will calculate wire-to-wire spacing at any point along the wire. The vertical and horizontal components of the space between wires are calculated independently. The total vector is calculated, indicating the gap between wires. An example of this is shown in Figures 9-9a and 9-9b.

9.3.3 Wire Bonding Equipment

Wire bond successes owe a great deal to the dedicated efforts of equipment suppliers. The massive equipment infrastructure of wire bonding cannot be overemphasized. For example, as other connection technologies have gained popularity, wire bond equipment vendors have maintained their competitive position by continuing to offer increased bonding rates as well as the ability to decrease bond pad pitch.

Requirements are now in place for wire bonding to be evaluated statistically (high strength with low variability). Low variability is achieved and maintained

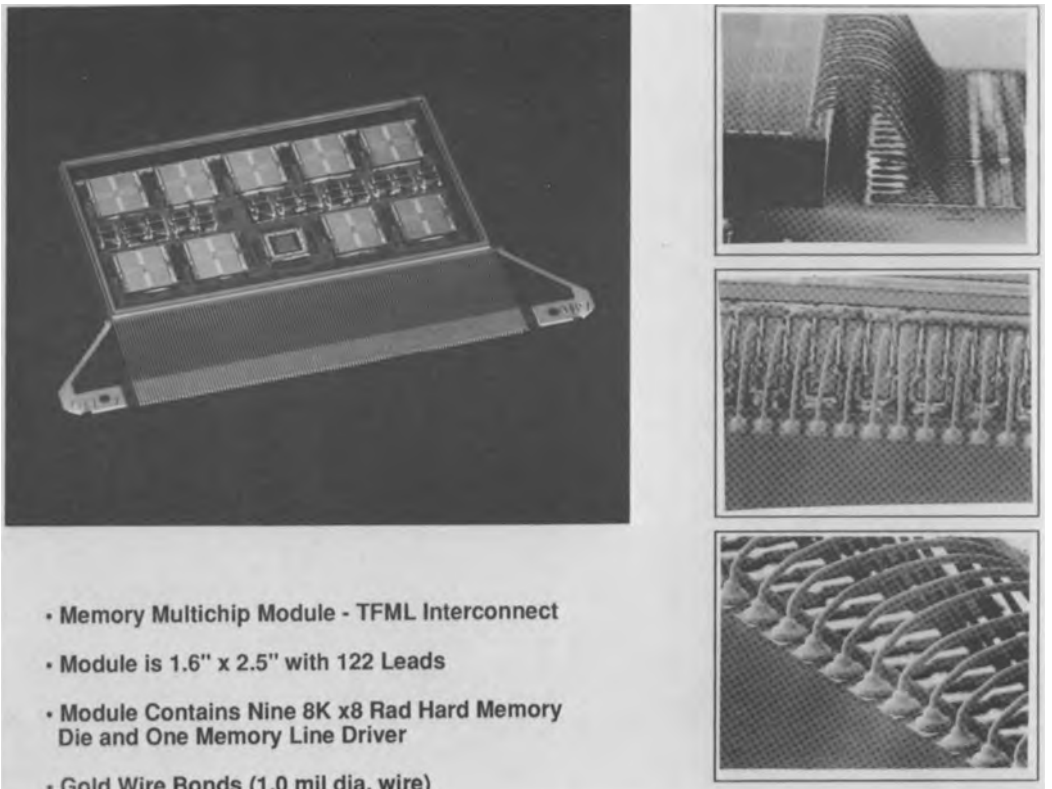


Figure 9-8 Memory multichip module containing nine 8K × 8 radiation hard memory die and a memory line driver. Package is ceramic with TFML interconnections, overall size is 1.6" × 2.5" with 122 leads. (Courtesy of C. J. Speerschneider, Honeywell.)

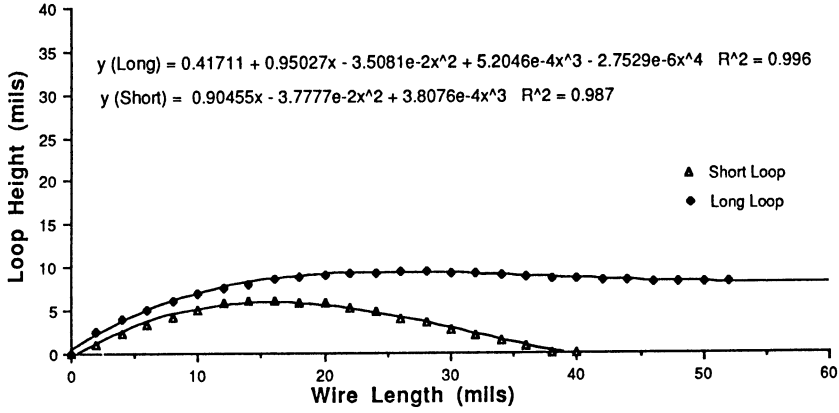


Figure 9-9a Curve fitted wire loop profiles for a typical two-tiered, wedge bonded package.

by monitoring every phase of the bonding process. Many types of analytical equipment are used to monitor wire bond machine performance and to identify undesirable conditions (often not apparent). For instance, equipment is available to measure the impedance of the bonding tool in free air and as the bond is formed [20]. These impedance measurements can be used to maximize the performance of the ultrasonic system and to troubleshoot the system.

Wire bonding equipment, in competition with the emergence of tape automated bonding (TAB) technology, has been pushed with respect to bonding speed and density. For example, it is possible in tenths of a second for a ball bonder to automatically form the ball, to position the capillary, to apply power and force for the requisite dwell time, to loop the wire to the ending pad forming that bond and then to excise the wire. Speeds of 4 wires/sec. for wedge bonding and 10 wires/second for ball bonding are common. Fully automated equipment is manufactured by several U.S., European, and Japanese companies. U.S. companies include: Hughes Aircraft, Kulicke & Soffa, and Orthodyne [21]. This automation has been made possible by the addition of microprocessor control and optical vision systems to the equipment. The vision system uses fiducials or standard features on the die and package to accurately determine their location in space. Vision and positioning systems having location accuracy within a few tenths of a mil have allowed wedge bonding of parts in the 3 mil pitch range. Vision systems also accommodate package variations inherent in cofired package processing. Another wire bond equipment feature beneficial to

VARIABLE DESCRIPTIONS	VARIABLES
Short Bond Wire Length (nominal)	40.00 mils
Long Bond Wire Length (nominal)	52.00 mils
Bond Wire Diameter (nominal)	1.25 mils
Lower Shelf Misalignment (due to artwork shift)	+/-2.00 mils
Upper Shelf Misalignment (due to shelf shift)	+/-1.00 mils
Die Placement Tolerance (X-Y)	+/-1.00 mils
Die Placement Rotation Tolerance	+/-0.50 Deg's
Die Pad Pitch (nominal)	5.00 mils
Die Size (longest side measurement)	460.00 mils
Wire Bond Placement Tolerance	+/-0.40 mils
Distance From Die Pads (for detailed error info)	12.00 mils

VERTICAL SPACE COEFFICIENTS	VALUES
Short Wire Formula (3rd order equation)	
Coefficient of x	9.05E-01
Coefficient of x^2	-3.78E-02
Coefficient of x^3	3.81E-04
Long Wire Formula (4th order equation)	
Coefficient of x	9.50E-01
Coefficient of x^2	-3.51E-02
Coefficient of x^3	5.20E-04
Coefficient of x^4	-2.75E-06

ERROR SUMMARY	ERRORS
Spacing Error Due To Bond Placement Tolerance	0.80 mils
Spacing Error Due To Upper Shelf Shift Tolerance	0.23 mils
Spacing Error Due To Lower Shelf Shift Tolerance	0.60 mils
Spacing Error Due To Die Shift Tolerance	0.07 mils
Spacing Error Due To Die Rotation	0.13 mils

RESULTS SUMMARY	RESULTS
Vertical Wire Spacing At The Critical Distance	1.12 mils
Horizontal Spacing At The Critical Distance	1.92 mils
Horizontal Spacing After RSS Analysis	2.71 mils
Total Worst Case Wire Spacing	**2.22 mils**
Total Wire Spacing After RSS Analysis	**2.94 mils**

Distance Measured From Die Pad	Wire Spacing
1.00 mils	2.86 mils
2.00 mils	2.78 mils
3.00 mils	2.70 mils
4.00 mils	2.62 mils
5.00 mils	2.54 mils
6.00 mils	2.47 mils
7.00 mils	2.40 mils
8.00 mils	2.34 mils
9.00 mils	2.29 mils
10.00 mils	2.25 mils
11.00 mils	2.23 mils
12.00 mils	2.22 mils
13.00 mils	2.23 mils
14.00 mils	2.27 mils
15.00 mils	2.32 mils
16.00 mils	2.40 mils
17.00 mils	2.50 mils
18.00 mils	2.63 mils
19.00 mils	2.77 mils
20.00 mils	2.94 mils
21.00 mils	3.12 mils
22.00 mils	3.33 mils
23.00 mils	3.54 mils
24.00 mils	3.77 mils
25.00 mils	4.02 mils
26.00 mils	4.27 mils
27.00 mils	4.53 mils
28.00 mils	4.80 mils
29.00 mils	5.07 mils
30.00 mils	5.35 mils
31.00 mils	5.63 mils
32.00 mils	5.92 mils
33.00 mils	6.20 mils
34.00 mils	6.48 mils
35.00 mils	6.76 mils
36.00 mils	7.04 mils
37.00 mils	7.30 mils
38.00 mils	7.56 mils
39.00 mils	7.81 mils
40.00 mils	8.05 mils

Figure 9-9b Three-dimensional wire spacing analysis using curve fitted loop profiles and significant packaging tolerances.

MCM manufacturing is the capability to change quickly from one product to another with minimal tooling and software changes. Software programs for a wide variety of products can be written by the user and stored on disk. A product change can be made in as little as 20 minutes. An example of a commercial ball bonder is shown in Figure 9-10.

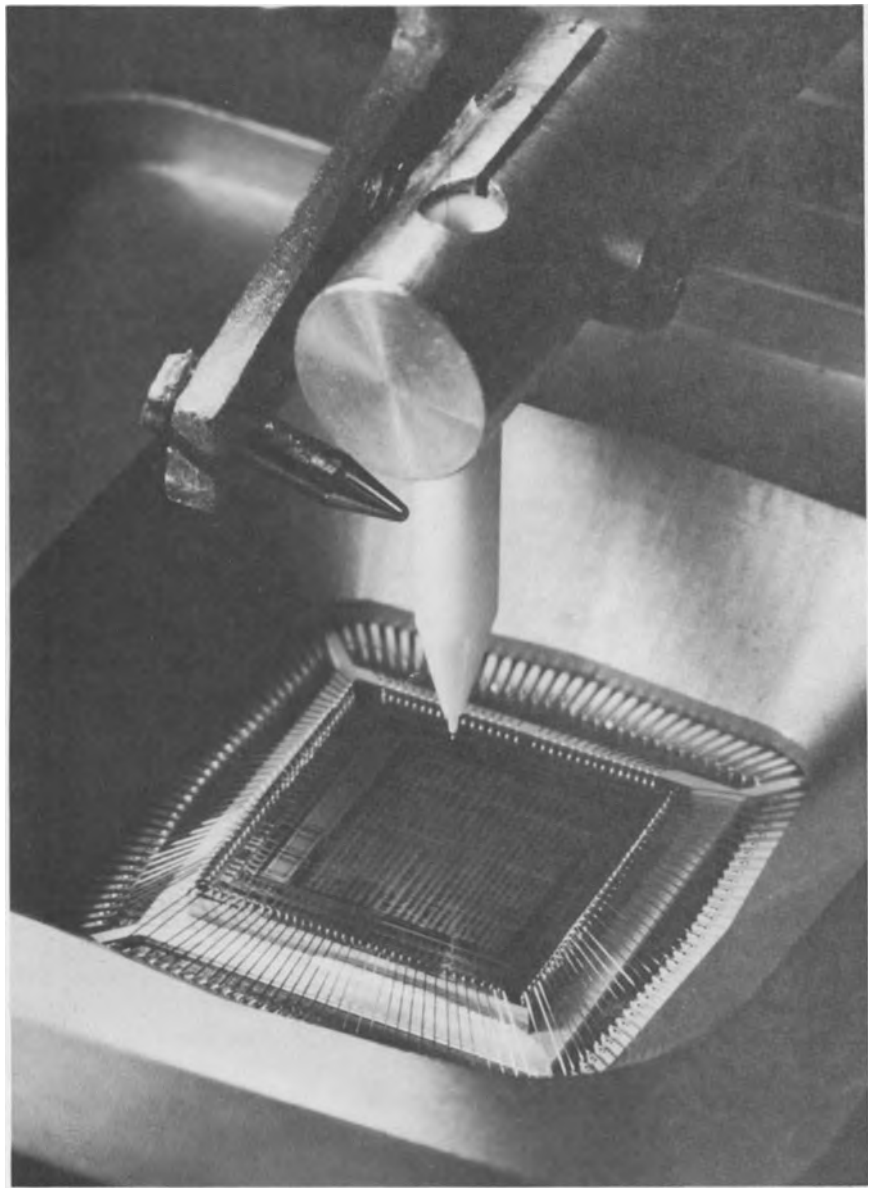


Figure 9-10 Fine pitch 132 lead device bonded in a K & S 1484 automatic gold ball bonder. (Courtesy of Kulicke & Soffa Industries.)

Table 9-12 Wire Bond Process Clearance Requirements.

WIRE BOND PROCESS	WIRE TEAR METHOD	WIRE FEED ANGLE	WIRE TEAR/FEED MOTION REQUIRED	CLAMP CLEAR-ANCE REQUIRED
Thermocompression Ball Bonding	Vertical tear	90°	Yes, vertical	None
Ultrasonic Wedge Bonding	Table tear	45°-90°	Yes	Yes
Ultrasonic Wedge Bonding	Clamp tear	30°-45°	Yes	Yes
Ultrasonic Wedge Bonding	Clamp tear with swipe motion	45°-60°	Yes, + swipe	Yes

A consideration when selecting wire bond equipment for MCM assembly is the required table travel to bond the desired module. If the working area of the wire bonder is sufficient to bond the entire MCM, production cycle time is reduced. For wedge bonding, the dimensions of the MCM and die placement on the module should be considered, since the machine must rotate the part or the machine bond head to maintain first and second bond alignment.

9.3.4 Electrical Performance

Wire bonding ranks behind TAB and flip chip bonding when it comes to high speed performance where low inductance is critical. The electrical performance of a wire bonded package or module can be optimized if the package designer understands the capabilities and limitations of the wire bond process. Wires can be shortened to the minimum length without sacrificing manufacturability. Wire geometry can be optimized to reduce inductance. If the MCM is designed creatively for short wires, the inductance of the wire bonds can be close to, if not less than, conventional TAB leads. However, flip TAB can be designed with shorter lead lengths, providing significantly less inductance than most wire bond designs [22]. A typical inductance value for wire bonds approximately 0.100" long (1.00 - 1.25 mil diameter wire, Au and Al) is on the order of 2.5 nH. A typical DC resistance value for 1.00 mil diameter wire of this length would be approximately 0.14 Ω for Al and 0.11 Ω for Au wire. In comparison, a flip

TAB lead 50 mils long designed for 4 mil pitch (0.002 sq. in. × 0.0013 sq. in. cross section Cu) would have approximately 1 nH inductance and 0.013 Ω resistance. Area array flip chip designs supply resistance, inductance and capacitance values much lower than either wire bond or TAB. This is due to the short connection lengths and high I/O capabilities without periphery connection restrictions.

9.3.5 Reliability as Applied to MCMs

A major advantage of wire bonding for MCM connections is its solid base of reliability from bond strength studies to time and temperature design factors. MCM technologies, however, bring new metallization schemes and deposition processes which may affect reliability. A diligent effort must be made to assure that any new, or previously unproven conditions (residual chemicals, different metals, or metal thicknesses) are evaluated thoroughly to ensure a reliable MCM environment.

The major reliability concerns with wire bonded structures are the intermetallic reactions occurring with time and temperature [23]. The condition of intermetallic formation between dissimilar metals, such as in gold wire with an aluminum alloy bond pad, or with aluminum wire on a gold bond pad, should be studied and understood. Intermetallic diffusion can occur in which the failure mode is an increased joint electrical resistance or low pull strengths due to eventual voiding at the interface. For the gold ball bond on an aluminum alloy pad, the thickness of the aluminum is the main concern. With insufficient aluminum, the pad can be consumed by an intermetallic formation, eventually causing voiding. With the aluminum wedge bond on a gold pad, the main concern is the ratio between the bond heel thickness and the gold thickness on the pad.

Contamination from wafer processing, plastic package outgassing or epoxy die attach outgassing and bleedout affects bondability and reliability. While these surface impurities may affect bond yields, it is the reliability factor after bonding which is of concern [24]. Contaminates accelerate failures by reducing the onset temperature or the time to failure due to intermetallic growth. Plasma cleaning using argon or argon-oxygen mixtures can be used in most cases to clean the interface prior to bonding [25]. The effects of pre- and post-processing temperature excursions, away from those involved directly in the bonding process, should also be analyzed, as they may reduce initial bondability or accelerate intermetallic failure.

Some actual reliability concerns related to the various metal systems and processes incorporated in different packaging methods are listed in Table 9-13. Cofired ceramic single and MCM packages with hermetic high temperature

Table 9-13 Intermetallic and Reliability Concerns for Various Package Types.

Package Type	Package Pad Metal	Die Pad Metal	Wire Type	Lid Sealing Method	Intermetallic and Reliability Concerns
CerDip	Al	Al	Al	Hermetic; high temperature	None
Cofired Ceramic	Plated Au/Ni	Al	Al	Hermetic; high temperature	Management of gold thickness on package.
Cofired Ceramic	Plated Au/Ni	Al	Au	Hermetic; high temperature	Management of assembly, process times, temperature, bond pad cleanliness.
Plastic	Plated Ag/Cu	Al	Au	Nonhermetic; low temperature molding	Chemical impurities, mechanical stress on wires.

sealing have been designed and assembled using gold and aluminum wire. It is necessary to accurately define the post processing and burn-in time at temperature exposures during the early stages of the package development.

Wire pull tests for wedge bonds and shear tests for ball bonds should be used to determine that complete interfacial bonding is achieved. Environmental tests, such as accelerated time temperature and temperature cycling, must be conducted to assure that long term materials compatibility is maintained in the product, especially if new materials or processes are introduced.

9.3.6 Yield and Repairability as Applied to MCMs

Wire bond yield potential and repairability factors may influence the selection of wire bonding for an MCM chip connection solution. Industry yield values exceeding 99% for single chip devices with over 300 wires have been achieved for both the ultrasonic and thermosonic bonding processes. This yield may be obtained without repair or rework, and correlates to a 34 ppm defect rate on an individual wire basis. Table 9-14 shows process ppm defect rates versus

connected chip yield for various wire counts. Rework can be performed in most cases for individual wires by manually removing the defective wire and bonding a new wire in place. In some cases, if a reworkable die attach material is used, individual die can be removed and reworked. If individual die removal and replacement is necessary, the substrate and die attach materials (FR-4, ceramic or thin film) should be carefully considered, as die rework may, or may not, be feasible.

When considering rework for wire bonds on a die, the pad dimensions and bonding process should be considered. Multiple wedge bonds can be placed on a pad if the new bonds do not overlap the old bonds, or if the new bonds only partially overlap the old bond impression. Thermosonic gold ball bonds can be stacked once or twice over previous ball bonds to rework individual wires. Military Specification 883C provides criteria for rework.

9.3.7 Wire Bond Process Development

When developing and improving a production wire bond process for single or multichip packaging, several key stages must be addressed. These stages include initial process design and development, process characterization, process control and process optimization. To refine a process, these stages form a continuous loop between characterization and control, with periodic optimization and development, as shown in Figure 9-11.

During the initial stages of process design and development, process capabilities should be understood to set achievable goals. For wire bonding, information is available through the published literature, as well as from industry and equipment vendor experience. Vendors for wire bond machines, wedge and capillary tooling, and bonding wire are excellent sources of information needed to develop a successful process.

The process characterization stage should include the installation of a data collection system, identifying specific defects on a per wire level. By breaking this down to the lowest level, and by identifying defects on a per wire basis, the major contributions to yield loss can be identified. Measures can be taken to resolve the specific problems. An example of the break down of defects (in ppm), as well as the common defect categories for a typical wedge bonding process, are shown in Table 9-15. The defects can be identified with individual machines, programs, products etc., to enable a full characterization of the process.

Process control also is important if a process is to be developed successfully. To define the performance level of a process accurately, a stable operation must first exist. Operating variables must be minimized and strict regulation of the existing variables must be established. Variables such as bond program

Table 9-14 Production Yield for Specific Wire Counts and Process Defects (ppm).

PRODUCT YIELD (%)	WIRE COUNT (CHIP OR MCM)							
	20	**50**	**100**	**200**	**400**	**600**	**800**	**1000**
99.9	50.0	20.0	10.0	5.0	2.5	1.7	1.2	1.0
99.5	250.0	100.0	50.0	25.0	12.5	8.3	6.3	5.0
99.0	500.0	200.0	100.0	50.0	25.0	16.7	12.5	10.0
98.0	1000.0	400.0	200.0	100.0	50.0	33.3	25.0	20.0
97.0	1500.0	600.0	300.0	150.0	75.0	50.0	37.5	30.0
96.0	2000.0	800.0	400.0	200.0	100.0	66.7	50.0	40.0
95.0	2500.0	1000.0	500.0	250.0	125.0	83.3	62.5	50.0
94.0	3000.0	1200.0	600.0	300.0	150.0	100.0	75.0	60.0
92.0	4000.0	1600.0	800.0	400.0	200.0	133.3	100.0	80.0
90.0	5000.0	2000.0	1000.0	500.0	250.0	166.7	125.0	100.0

Note: Allowable process defects (ppm) = (1 - desired yield) x 10^6/wire count (chip or MCM).
Entries represent 1 bad wire per defective chip (or MCM).

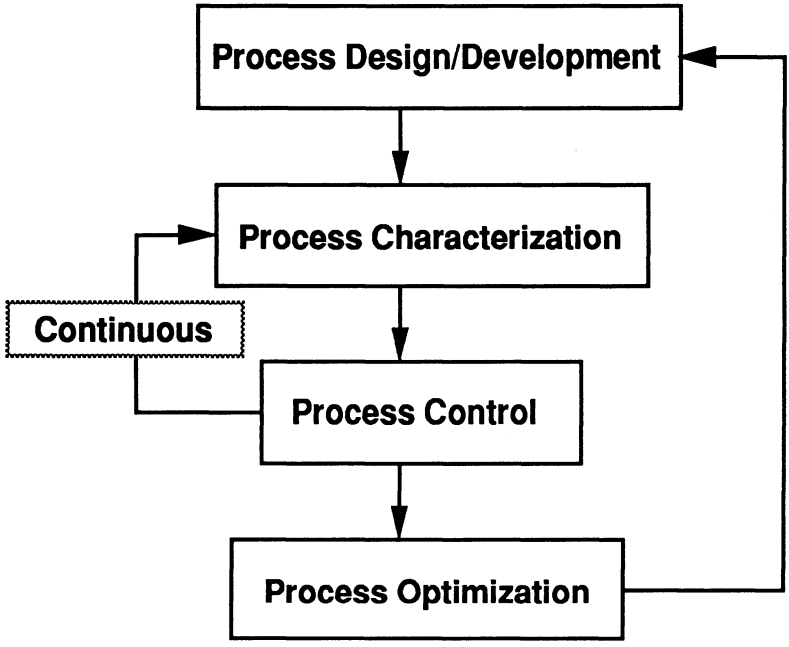


Figure 9-11 Typical wire bond process development flowchart.

parameters, machine setup and operation procedures, bonding tool installation, wire pull procedures and product change overs are examples of the areas needing focus and control. Consistency across the process, such as in the training of operators also must be established.

If the previous stages of process development are in place, process optimization can be performed using standard Taguchi or design of experiment techniques and focusing on the resolution of specific problems. Once a process is operating in a production environment, statistical process control (SPC) can be applied to such items as wire pull to monitor the process and to minimize process drift [26].

9.3.8 Wire Bond Process Costs

The cost, reliability and yield potentials of wire bonding make it a logical option when developing a MCM facility. Since wire bond processes involve no chip

Table 9-15 Defect Tracking System Summary.

				SPECIFIC DEFECTS (PPM)				
Bond Program	**Total Wires Bonded**	**Total Defects**	**Total Defects (ppm)**	**Bond Off Center**	**Bond Not Sticking on Die**	**Bond Not Sticking on Package**	**Broken Wire**	**Foreign Material**
MCM 1	200,000	4	20	5		10		5
MCM 2	300,000	7	23		10	3	10	
MCM 3	800,000	20	25	10		5		10

modifications and the equipment has an established base of competitive development, wire bonding is lowest in cost as an MCM connection method.

Current equipment costs are roughly $140,000 for wedge bonders and in the $120,000 range for ball bonders. Die attach equipment costs roughly $80,000 to $100,000. Support equipment, such as wire pull stations, plasma etchers and storage facilities, contribute to the remaining significant costs for wire bond processing. If die attachment requires very accurate and repeatable placement (±1 mil), costs rise significantly. With wire bonding, substantial non-recurring engineering (NRE) charges and tooling charges are minimized while equipment availability is maximized. In some cases, wire bond is unaffected by midstream module design changes that require redesigning TAB tape.

Cost differences become evident when competitive studies are made. In one study, a three chip module, based on ceramic substrate technology, was constructed using wire and flip chip methods. Wire bonding was done using conventional high volume, single chip equipment. An additional cost factor in using a flip chip technology, was the increased substrate costs. Tolerances required for flip chip bonding were more stringent than those required for wire bonding, therefore increasing costs. From this study, it became obvious that each application may require a separate cost evaluation.

Cost analyses include volume and individual process cycle time predictions, equipment costs, tooling costs and non-recurring tooling and engineering costs. In some cases, multiple wire bonders are set up in parallel, providing volume comparable to a single gang bonding TAB operation at an approximately equivalent equipment cost. The cost associated with the flexibility required for engineering and product design changes, which occur and should be anticipated as a part of the planning cycle, also should be evaluated.

9.3.9 Comparison to Other Connection Techniques

TAB pitch limitations are similar to those in wire bonding. However, smaller pitches in the range of 50 μm have been cited for TAB [27]. Area array flip chip solder bump and area TAB are current alternative technologies. They have the potential to exceed peripheral pitch limitations to I/O density occurring with wire bonding. Electrical performance is a key issue necessitating a switch from wire bonding to TAB or to flip chip solder bump technologies. TAB, in general, can exhibit less inductance and capacitance than an equivalent wire bonded package. Also, TAB can provide a pretest capability for die prior to installation in the package or on the module. An advantage of wire bond relative to flip TAB or to flip chip is the ability to perform a complete visual inspection of the connection after the module is assembled. The wire bond processes also offer limited abilities in repair.

Of three current alternatives for MCM chip connection applications (wire bond, TAB and FCSB), wire bonding offers the most mature, flexible and inexpensive assembly method. A mature infrastructure is in place. Extensions of the process have permitted wire bonding to meet new challenges. There is a history of reliability data and general industry experience. This base of technology and experience establishes wire bonding as a viable alternative for current as well as for future MCM development. TAB and FCSB provide benefits in electrical performance and density relative to wire bond, but at higher cost and with more extensive development requirements.

9.3.10 Summary

When selecting a chip connection method for an MCM application, several considerations are important, including cost, time to market, manufacturability, electrical performance and reliability. The applicability of wire bonding to MCM packages is dependent on the substrate material, requirements in geometry, secondary process thermal requirements, material compatibility, chip removal and repair requirements, and pre test requirements.

The optimum wire bond process needs to be determined relative to the application. For example, when the substrate is heated, thermosonic gold ball bonding offers the best method for COB-type MCM applications, where components are placed as close together as possible. Aluminum wedge bonding offers the finest pad pitch and the highest wire density, together with potentially favorable metallurgical conditions and processing at ambient temperature.

When designing an MCM, careful attention must be given to the space and clearance requirements for the wire bond process chosen, as well as to metallurgical and materials compatibility. Once a process is selected, and the MCM is designed, process development tools should be applied to enhance the process by increasing yields and product reliability, as well as reducing the overall product cost. The well established infrastructure for wire bond is utilized to reduce the product time-to-market and to maximize the process efficiency. Although the wire bond approach does not include a pretest possibility like TAB or a low impedance like flip chip solder bump, its specific advantages should warrant its consideration when developing a MCM facility or product.

Acknowledgments

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9.4 TAPE AUTOMATED BONDING

Dean R. Haagenson, Steve J. Bezuk, Rajendra D. Pendse

9.4.1 Introduction

Tape automated bonding (TAB) is a connection technique for attaching semiconductor die to a variety of packaging media, including single chip and multichip packages. The connection is made by bonding a patterned conductor to the corresponding I/O pads on the die and package (See Figure 9-12). TAB parts can be assembled (see Figure 9-13) in three basic configurations: conventional TAB, flip TAB and cavity TAB.

Conventional TAB consists of mounting the die with the backside attached to the substrate or package. Leads are formed to facilitate the connection from the plane of die to the plane of the substrate or package. Flip TAB consists of mounting the die with the active surface facing the substrate or package. The bonding pitches on the die can be equal to those on the substrate or package with little or no leadforming required. This results in leads that are short relative to

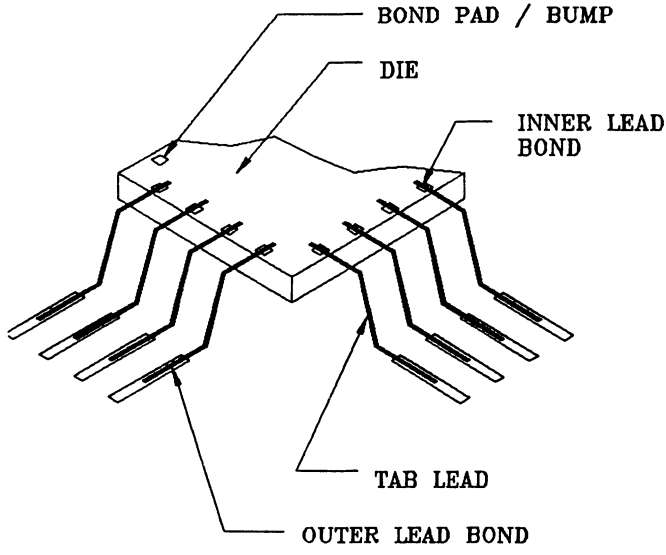
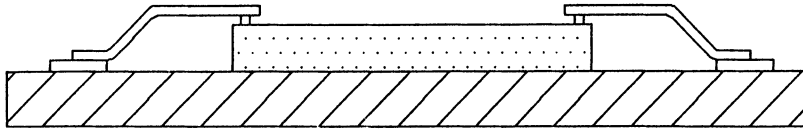
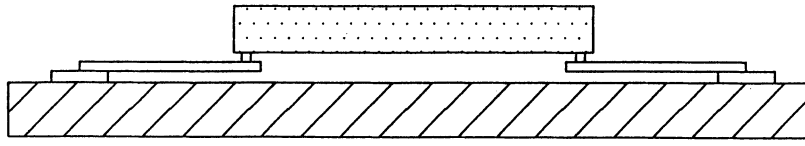


Figure 9-12 Schematic illustration of the TAB concept.

CONVENTIONAL TAB



FLIP TAB



CAVITY TAB

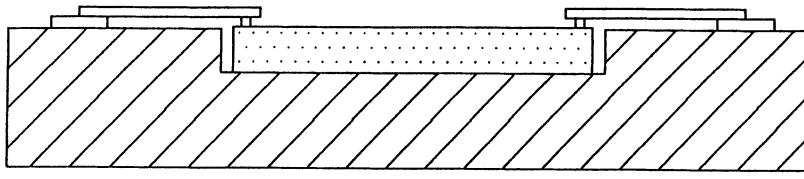


Figure 9-13 TAB assembly configurations.

conventional TAB. Cavity TAB is similar to flip TAB in that the die and package pitches can be equal with short leads. Flip TAB and cavity TAB provide for the denser TAB assembly of MCMs compared to conventional TAB.

Cavity TAB, however, is difficult to implement due to package material and design limitations. Another, more recent, TAB configuration provides for routing the leads to an array of solder bumps on the tape frame, which can then be mounted on the substrate or package. This is called array TAB.

TAB originally was envisioned as an alternative and eventual replacement for wire bonding in the 1960s. However, steady improvements in wire bond technology and the high costs associated with TAB implementation have limited the use of TAB to high volume consumer electronics products that require low profile and high density assembly.

The interest in TAB as an alternative to the wire bond and surface mount assembly of VLSI chips arises because its application eliminates a level of packaging. The TABed die can be bonded directly to a PWB or to an MCM substrate (See Figure 9-12). Additionally, TAB offers the following advantages over traditional wire bonded packages:

1. Superior electrical performance
2. Assembly of high lead count, fine pitch devices
3. Device testability prior to commitment to package
4. Repairability and
5. The dense assembly of low profile components.

Despite the inherent advantages of TAB, its implementation in the high performance and MCM areas has been slow. This is the result of an inadequate infrastructure for advanced equipment and materials needed, as well as cost. Lower volumes and custom tooling required for the die and package designs have contributed to these cost issues.

9.4.2 Basic Process Flow for TAB Packaging

Figure 9-14 shows a process flow for a typical TAB packaging application. In this section, the specific steps in the TAB packaging flow and assembly process are discussed.

Wafer Bumping

Typically, metal standoffs, or "bumps," are added to the I/O pads on an IC. These bumps are normally gold plated on the wafer, although solder and copper bumps also are used. The purpose of these bumps is to provide the proper metallurgy for the inner lead bond (ILB), to provide a standoff preventing the TAB lead from shorting to the edge of the die, and to protect the underlying aluminum from corrosion or contamination. A typical bump configuration is shown in Figure 9-15. An under bump metallization (UBM) is required to

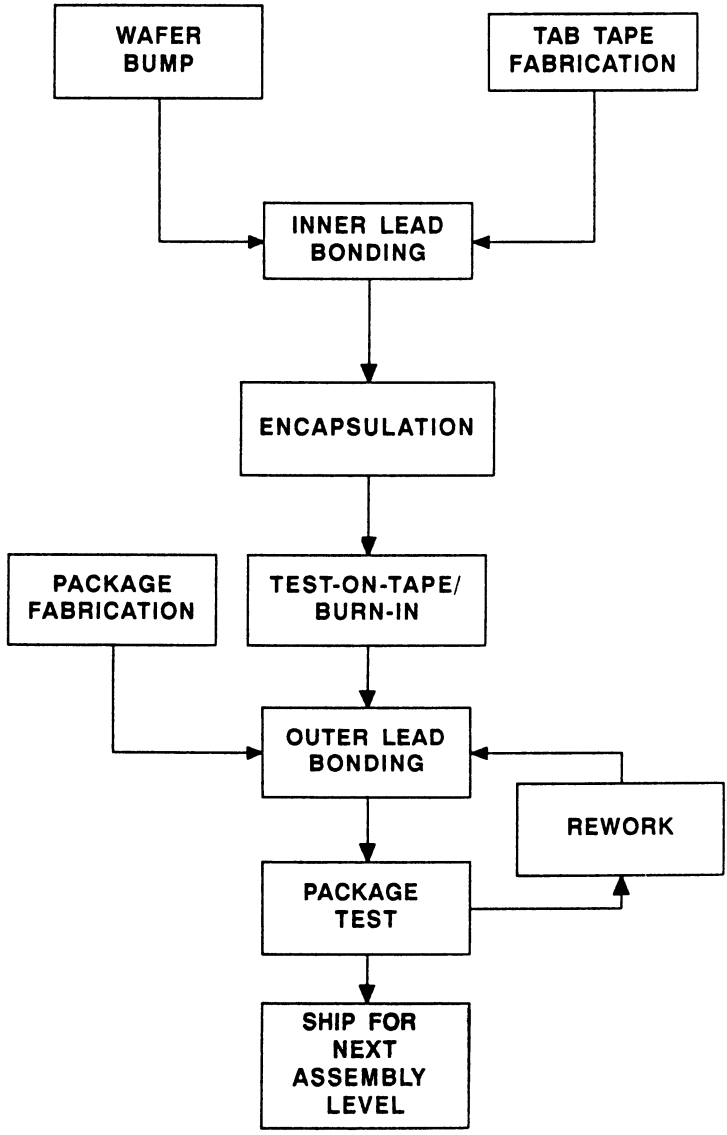


Figure 9-14 Process and materials flow for TAB packaging.

provide a diffusion barrier between the gold of the bump and the aluminum pad. The bottom metal must have good adhesion and the top metal should be inert and plateable. A typical choice of UBM is 0.2 μm Ti-W over the aluminum,

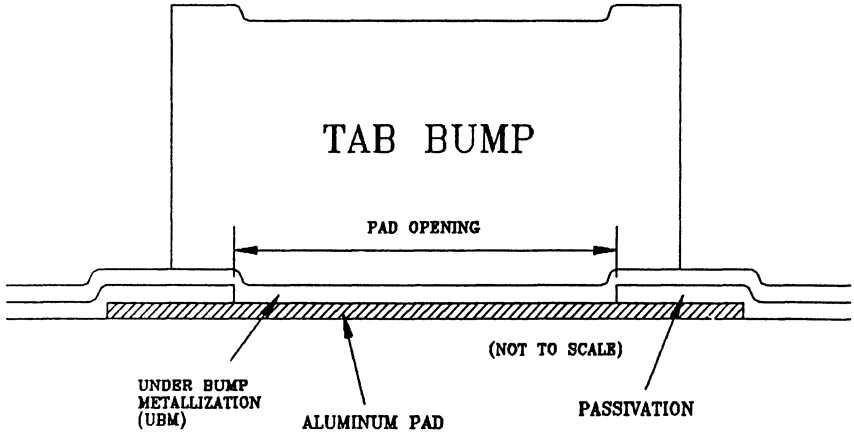


Figure 9-15 A typical bump configuration showing the pad opening and the under bump metallization (UBM).

covered by 0.1 μm Au. The bump is plated over this thin gold layer. The extension of the bump and UBM beyond the pad opening and over the passivation layer, facilitates the sealing of the aluminum pad from moisture and external contamination (see Figure 9-15). Bumping technology, and alternatives to wafer bumping, including the criteria for UBM selection are reviewed elsewhere [28]-[29]. Alternatives include bumped tape, bumps deposited by gold ball wire bonders and bumpless configurations [30]-[32].

TAB Tape Processing

The important features of a typical TAB tape design are illustrated in Figure 9-16. MCC has developed CAD tools specifically for the expeditious design of tape. Attempts have been made to standardize outer lead bond (OLB) footprints and tape formats by the JEDEC and EIAJ committees. Standardization of pad patterns for PCBs has been pursued by the Institute for Interconnection and Packaging of Electronic Circuits (IPC). Standardized pad patterns help reduce the costly tooling associated with TAB, but also can limit the advantages in density and electrical performance.

Tape is manufactured in continuous reels or in panel arrays. The tape is supplied for use on inner lead bonding (ILB) equipment in reels or singulated and mounted into individual slide carriers. Slide carriers are becoming popular, particularly for higher lead count die. The carrier format eliminates mechanical

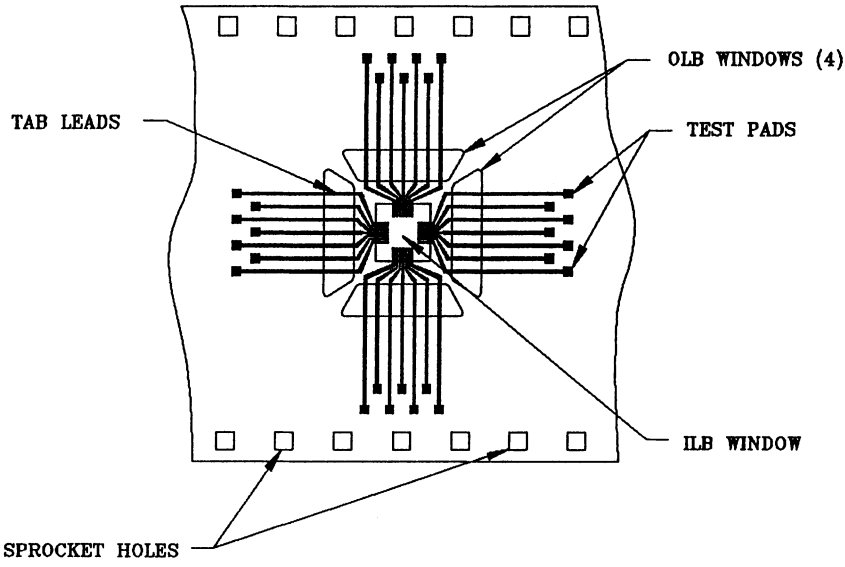


Figure 9-16 Important features of a TAB tape design.

damage resulting from the bending stresses encountered during the rolling process, and also reduces the likelihood of handling damage.

Inner Lead Bonding

The patterned TAB tape frame is connected to corresponding I/O pads on the die during the inner lead bonding (ILB) process. This process involves the metallurgical bonding of the tape leads to the bumps or bond pads. A variety of process options exist for ILB that depend on chip size, tape and bump metallurgies and other process constraints.

Encapsulation

Following ILB, the IC is typically encapsulated using one of many possible methods [28] (see Figure 9-17). The purpose of encapsulation is to protect the die chemically and mechanically. Epoxies and silicones are popular materials used for TAB encapsulation. Material properties that are important considerations for encapsulants include:

- Low alpha particle emission
- High temperature stability (governed by the glass transition temperature)

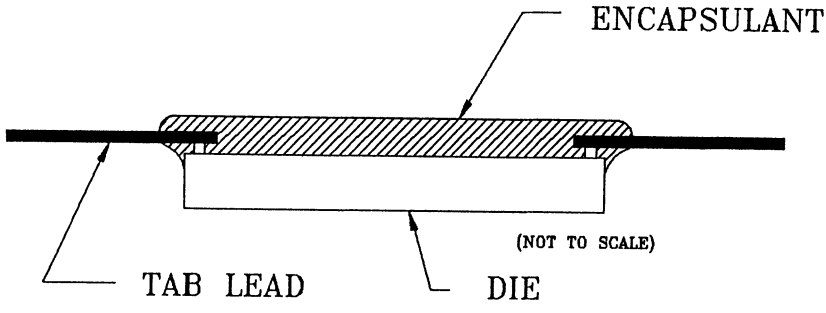


Figure 9-17 An encapsulated TAB chip.

- Minimal hardening or embrittlement at low temperatures (-55°C)
- Low moisture absorption
- Low ionic content
- Low modulus of elasticity and
- A coefficient of thermal expansion (CTE) minimizing the stress on the die or cracking of the encapsulation.

Test chips can be designed to evaluate and qualify encapsulants. A variety of machines are available for the dispensing and curing of these materials. Other encapsulation schemes include overmolding the inner lead bonded device in an injection mold, much like a wire bonded device on a leadframe [33].

Test-on Tape and Burn-in

One of the major advantages of TAB is the ability to test an inner lead bonded and encapsulated die prior to committing it to a package, especially a multichip module (MCM). A number of vendors sell TAB test and burn-in sockets designed to work with JEDEC and EIAJ standard tape and carrier designs. Use of these sockets may require a larger tape format for larger lead counts in order to fit the test pads into the standard test pad layout. This can increase the cost per frame of the tape. Alternatively, designing and fabricating custom test sockets, at finer test pad pitches than those of the standards, can increase costs.

Outer Lead Bonding

The outer lead bonding (OLB) process connects the die to the package and subsequently, to the outside world. This process is actually a set of sub-processes that includes:

- Excise and form
- Flux and die attach
- Align and place
- Actual bond process
- Clean

As with ILB, a variety of OLB bonding methods exist.

Final Test and Assembly
Following OLB, the packages are inspected and tested. Assembly errors or electrically failed die can be reworked at the OLB level, another advantage of TAB. The packages are then shipped for system assembly.

9.4.3 TAB Tape Considerations

Choosing the proper TAB tape, from among various configurations, material options and formats, is a crucial step in its application. This section explains the issues involved with tape materials and formats and their impact on the assembly options.

TAB Tape Materials
A variety of material options are available to tailor a particular TAB tape design to a specific application. Chemical, metallurgical and mechanical properties must be balanced to optimize the design with respect to the manufacture of the TAB tape, the subsequent TAB assembly processes and the predicted environmental exposures of the package.

Conductor. Copper is the predominant choice for the conductor material of TAB tape, because it best meets the primary requirements of a TAB conductor: satisfactory electrical, mechanical and chemical properties. Two types of copper are used in TAB applications: rolled and annealed (R&A) and electrodeposited (ED). The two kinds of copper have different microstructure and mechanical properties that influence the bond formation mechanism at the inner and outer leads. The use of these coppers depends on the desired application and the type of tape (see ***Tape Types*** later in this section) being used. Some important material properties of the copper are shown in Table 9-16 [34].

Dielectric. The dielectric should be resistant to high temperatures, mechanically stable, have low ionic contamination and show high moisture resistance. Polyimides have been the material of choice for the dielectric. Two variations of the basic polyimide chemistry, sold under their respective brand names, are in common use: Upilex, manufactured by Ube Industries in Japan, and Kapton, manufactured by DuPont. Upilex, a stiffer material, is not suitable

for wet etching, limiting its use to three layer tapes. The generic properties of the two are listed in Table 9-17 [35]. A range is indicated for certain properties because of the variability in data received from different sources.

Adhesive. Adhesives are used in three layer tapes to attach the copper conductor to the dielectric. Mechanical stability and compatibility with the other materials and processes making up the laminate is important, as described in Section 9.2. Electrical resistance at various relative humidities also is important. Acrylic or epoxy based materials, usually with proprietary formulations, are most commonly used.

Plating. The finish plating on the copper leads provides the desired bond metallurgy and environmental protection to the copper. Common plating metals include tin, gold and solder with tin and gold being the most popular. A nickel barrier between the copper and the cover plating also can be included as a metallurgical barrier. Selective plating of different cover materials also is a possibility, depending on tape design, and enables the user to tailor the ILB and OLB metallurgies. Gold is electroplated on the copper leads, necessitating a bus structure to connect all of the leads. Typically tin is plated electrolessly and does not require bussing of the leads.

TAB Tape Types

TAB tape is a patterned conductor, free standing or laminated to a dielectric layer. The pattern matches the I/O pattern on the semiconductor die and provides for the connection of that die to the package. These tapes are generally categorized by their number of distinct, material layers. The three most common types, with one conductor layer, are called one, two and three layer tapes (see Figure 9-18). Multiconductor layer tapes (see Figure 9-19) also exist; those with two conductor layers are becoming more common, and can furnish the package designer with enhanced electrical properties. Attempts have been made to standardize the various tape formats based on overall dimensions, socket hole pitch and OLB patterns. Overall dimensional outlines of 35 mm, 48 mm and 70 mm are JEDEC and EIAJ registered tape formats. Adoption of these standards allows the material, equipment and tooling suppliers to minimize costs.

One Layer Tape. This type of tape consists of only the patterned metal conductor (see Figure 9-18). The material is typically R&A copper, chemically etched to define the pattern. One layer tape has advantages in low cost, high volume manufacturing applications, typically molded plastic packages. The principal disadvantages, which preclude it from most MCM applications, are lack of testability on tape and the limited tape format size (usually 35 mm).

Two Layer Tape. This type of tape refers to a construction in which the patterned metal conductor adheres to a supporting layer of dielectric (see Figure 9-18). The conductor material is additively plated to a seed layer, usually

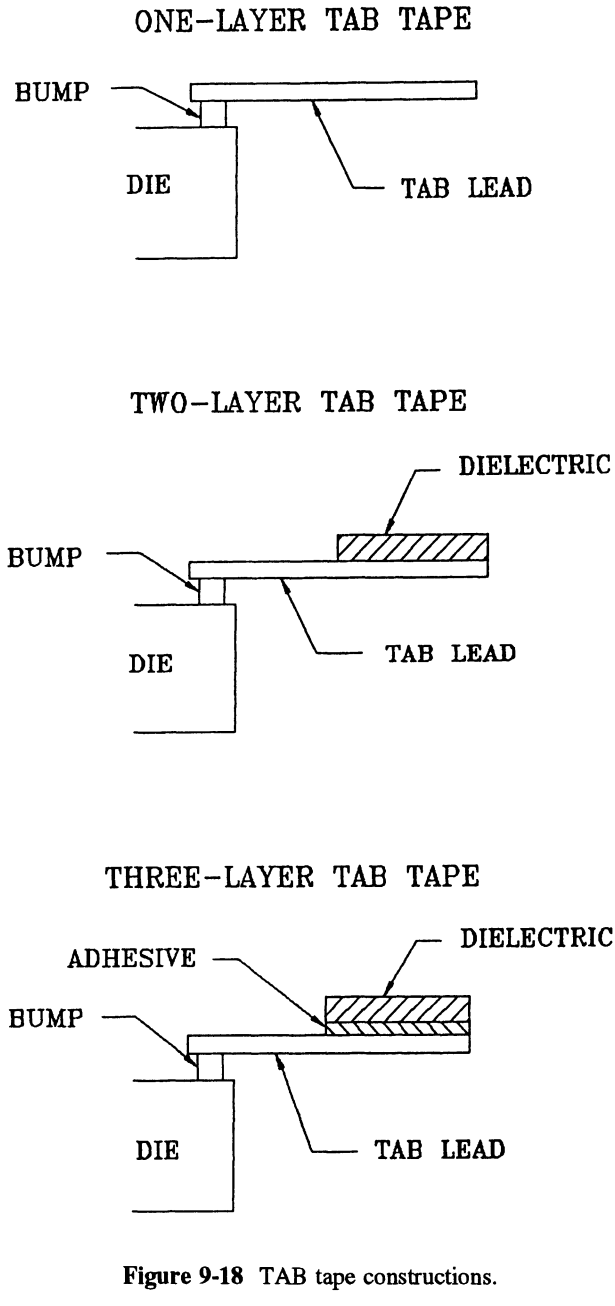


Figure 9-18 TAB tape constructions.

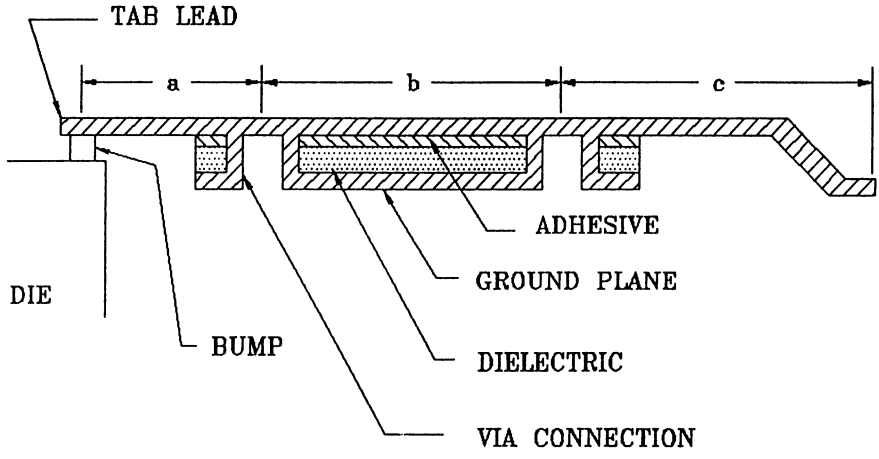


Figure 9-19 Two metal layer tape construction.

chrome, on the dielectric. The conductor can be patterned during additive plating or by using subtractive etching following a full plating of the conductor layer. Patterning while plating provides for finer pitch capability since it is free from the undercutting effects of the subtractive etch process. Conductor material in two layer tape is limited to ED copper, reducing flexibility in tailoring the tape materials to the demands of the application. Patterns in the dielectric, usually a polyimide, are chemically etched and limit the thickness of this layer to 0.002". Flexibility in choosing desirable chemical and mechanical characteristics of the dielectric are limited. The leads in two layer tape are isolated individually by this dielectric, which is not the case for one layer tape. This isolation allows for device testability. This characteristic, along with its fine pitch capabilities, make it an attractive candidate for MCM applications.

Three Layer Tape. Three layer tape is similar to two layer tape, with the exception that the adhesion of the conductor to the dielectric is accomplished by means of an obvious adhesive layer (See Figure 9-18). The dielectric, usually a polyimide, is 0.005" thick and is mechanically processed, or punched, prior to lamination of the conductor. The windows, sprocket holes and other features are formed during this process. An adhesive is applied and the conductor foil, R&A or ED copper, is laminated to the dielectric carrier. The conductor is patterned by a subtractive etch process. Three layer tape provides the user with greater flexibility in material choices, superior adhesion of the conductor to the dielectric and better flatness.

bonded by both single point and gang techniques. The different bonding methods and techniques will be explained in more detail below.

ILB Process Flow

Normally, the die is placed on a heated stage, the tape leads aligned over the bumps and the bond formed. Die can be picked up either from waffle packs or from sawed wafers on expanded tape while the tape can be fed reel to reel or in slide carrier format. As is indicated in Table 9-18, a variety of processes exist for forming the ILB. These processes are the product of mating a bonding technique with a bonding method and are discussed below.

ILB Techniques

ILB can be accomplished by two techniques. The first is gang bonding, in which all of the leads are bonded simultaneously to the die. The second is single point bonding, where each lead is bonded serially to its corresponding die pad or bump. Both techniques have advantages and disadvantages, depending on the application.

Gang ILB. ILB of all the leads simultaneously necessitates a tool that is very flat and evenly heated around the desired bonding area. Gang bond thermodes consist of two types: constant heat or pulse heated hot bar. The former is set at a specific process temperature, while the latter can be programmed to achieve a specific temperature profile during the bonding process. Constant heat thermodes are amenable to thermocompression bonding, while the hot bar thermodes are better suited to eutectic reflow. To achieve uniform bonding for both types of modes, tight temperature control, thermode flatness and planarity of the thermode to the bonding plane are critical.

A typical constant heat thermode consists of a polished diamond face, slightly larger than the die, captured in a metal shank heated by means of a cartridge heater. These thermodes hold their flatness well and generally, depending on size, have a uniform temperature distribution.

Hot bar thermodes, by design, change temperature during the bond process. These thermodes, applicable to lower temperature soldering applications, show greater deformation for the higher temperature ILB processes. This reduces the flatness of the tool and increases the temperature variability due to nonuniform contact with the part.

Single Point Bonding. Bonding one lead at a time to the die bumps eliminates the temperature uniformity and planarity problems of gang bonding, especially with larger die. Although the thermocompression, eutectic, reflow or laser methods all can be thought of as single point bond methods, the most common is thermosonic and involves the use of modified wire bonders to accomplish the task. Single point bonding requires less force per bond than

thermocompression, reduces the need for custom tooling, opens up the possibility for repair of unbonded leads and may even enable the user to bond directly to the aluminum.

ILB Methods

ILB, using one of the techniques described above, can be accomplished using one or combinations of the following four methods:

- Thermocompression
- Eutectic/reflow
- Thermosonic
- Laser

Selection of the proper method also depends upon the tape and bump and pad metallurgies (see Table 9-18).

Thermocompression Bonding. Thermocompression (TC) bonding involves the application of heat and pressure to form the metallurgical bond between the TAB lead and bump or pad metallurgy. The most common technique for accomplishing TC bonding is gang bonding. The gang bond is accomplished using a constant heat thermode, as described above. The bonding mechanism requires plastic flow of the bulk copper. The mechanical properties of the copper, particularly its tensile strength and hardness, are of critical importance. Thermocompression bonding of Au plated leads to Au bumps, probably the most popular version of the TC bonding, has the advantage of being an established process with a wide process window, although other metallurgies have been demonstrated. Typical parameters for TC bonding are 450°C - 550°C bonding temperature, 75 - 150 g/lead force, and 100 - 300 ms bond duration. The range in parameters is due to the different metallurgies.

Eutectic and Reflow. Eutectic and reflow ILB pertains to the local melting at the bond interface, induced under heat by suitable choice of tape and bump metallurgies. Tin plated tape on gold bumps, gold plated tape on tin capped bumps, as well as gold plated tape on solder bumps, are some typical combinations. Gang and single point techniques can be used, although gang is the most common. An estimate of the required bonding temperatures can be obtained by reviewing the phase diagrams for the metals involved. Bonding forces are generally less than those needed for TC bonding as force is needed only to maintain thermal contact. Thermode materials, not amenable to wetting of the liquid phase formed at the bond, are required. Temperature profilable thermodes that maintain contact pressure on the bond until solidification of the metallurgy is complete are required.

Thermosonic. Thermosonic bonding couples the heat from a die on a heated pedestal (150°C - 250°C) and the energy supplied by ultrasonics to form the bond. This method is limited to single point techniques. The single point tools are designed to scrub the lead and are made with geometries, finishes and materials enabling the tool and lead to couple during the bonding process. Less force is required than for TC bonding, although ultrasonic energy can be potentially damaging to the silicon.

Laser. Laser bonding is a relatively recent development. It uses a laser beam to locally heat the bond interface. The wavelength of light used must be chosen with regard to the specific materials to be heated. A Nd:YAG laser, operating at its fundamental wavelength of 1.064 μm, is a good choice for tin tape and gold bump or solder bonding applications because tin and tin/lead solders absorb 40 - 50% of the laser energy. The Nd:YAG laser, operating at the same wavelength, is a poor choice for gold to gold bonding since only 2 - 5% of the energy is absorbed. A frequency doubled Nd:YAG laser, operating at a wavelength of 0.532 μm, is a better choice for gold to gold since 40 - 50% of the energy is absorbed. Laser bonding, like reflow bonding, requires lower forces making it a good choice in applications for more fragile chips, such as GaAs.

ILB Equipment Issues and Availability

The predominant sources of ILB equipment supply thermosonic single point and constant heat gang bonders. The gang bonders are used predominantly for lower lead count, smaller die applications while single point bonders are popular in higher lead count, finer pitch work. Recently, laser bonders have become viable alternatives, but currently are generally limited to tin tape applications.

Gang Bonding. The major attribute of gang bonding is that it is a fast, one step process, taking only a few seconds per die irrespective of lead count. This allows for high throughputs. The major disadvantage of this process is the high tooling costs for each part type. Typically, the thermode, die holder and tape clamp are unique for each die. Process concerns include the planarity of the die, tape and thermode, as well as the temperature uniformity across the thermode. As die become larger than 10 mm, these issues become more pronounced and single point bonding becomes an attractive alternative [44].

Single Point Bonding. Thermosonic bonding is probably the most popular method associated with single point bonding. Thermosonic bonders are gaining some degree of automation comparable to their gang bond counterparts. An advantage of single point bonding is that the equipment senses the vertical locations of the lead and bump individually and, therefore, can tolerate much larger non-uniformities in tape thickness and bump height than gang bonders. Other advantages of single point bonding are minimal set up time and consistent,

controlled parameters for each bond. Changing from one part type to another involves a software change and easily realigned tooling. Single point thermosonic bonders have been, in general, derived from wire bonding equipment. The wire bond companies have marketed TAB versions of some of their wire bond platforms. Automatic alignment stages have been added to orient the tape over the bumps with minor software changes. A variety of tip configurations are available for the bonding of different lead or pitch configurations. A typical single point thermosonic system is shown in Figure 9-20 and an example of fine pitch (0.004") bonding in Figure 9-21. Metallurgies are limited to gold to gold for thermosonic single point bonders. Laser assisted (lasersonic) single point bonders are new additions to the equipment available for single point TAB. These bonders are well suited for reflow bonding (solder or tin) at their standard wavelength and frequency doubled versions are being developed. The cost of semiautomatic single point thermosonic TAB bonders is approximately $180,000 (1992 dollars) with die and tape automation adding another $100,000 (1992 dollars).

9.4.5 Outer Lead Bonding

The final TAB connection of the semiconductor die involves a process known as OLB. OLB can be performed successfully on a variety of substrate materials, including FR-4, ceramic and silicon using both metallurgical and mechanical bonding mechanisms.

OLB Process Flow

OLB can be considered as a group of sub-processes, including excise and form, fluxing and die attach, alignment and placement, the actual bonding process itself and cleaning.

Excise and Leadform. The inner lead bonded IC typically is removed from the TAB tape prior to placement and outer lead bonding in a process known as excising. Forming of the TAB leads also may take place during this step. The purpose of the leadforming is to bring the leads from the plane of the ILB to the plane of the OLB (as with conventional TAB) and to provide for thermal and mechanical stress relief. Excise and form is a critical part of the OLB process and becomes increasingly difficult as lead dimensions and pitches decrease.

Fluxing and Die Attach. Depending on the TAB application and the bonding mechanism, flux and/or die attach may be needed prior to the placement of the device. Flux can be applied to the OLB site or to the outer leads. Die attach substances can be dispensed on the package surface prior to placement to permit transfer of the package from the placement equipment to separate reflow or bonding equipment.

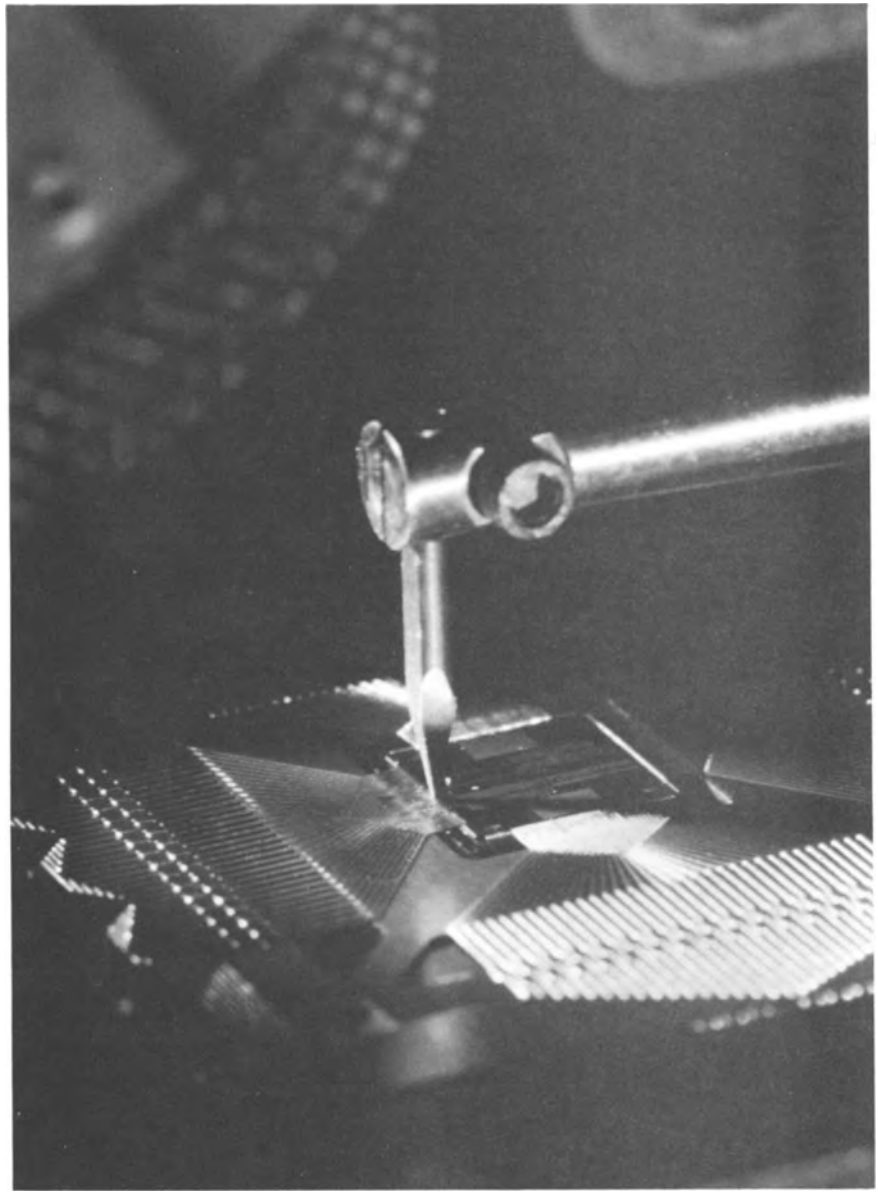


Figure 9-20 Single point thermosonic TAB bonder. (Courtesy of Hughes Aircraft Company.)

Figure 9-21 Single point thermosonically bonded TAB ILB 0.002" leads on 0.004" pitch. (Courtesy of Hughes Aircraft Company.)

Alignment, Placement and Bonding. After excise and form, the part is staged for pick up by the placement head. Alignment is critical to reliable bonding, necessitating accurate mechanical and vision systems. OLB pitches down to 0.004" need to be placed without misalignments that can cause shorting.

The bond process follows the placement of the device and can be accomplished by a variety of methods.

Cleaning. Solder OLB processes that use flux may need cleaning to remove the flux residues. This cleaning can be done using traditional surface mount technology (SMT) processes although attention should be given to the vulnerability of the assemblies to the cleaning solution.

Bonding Processes

Bonding mechanisms can generally be classified as being metallurgical or mechanical in nature. Technologies for achieving these bonds can be classified as mass, single component gang and single point bonding. Table 9-19 lists the metallurgical possibilities for the OLB and can be read for a specific process to arrive at the possible OLB and tape metallurgies. For example, using a single component hot bar gang process, only a solder OLB pad should be used and the tape metallurgy can be gold, tin or solder plate. Explanations of the process options are explained below.

Mass Bonding. Mass OLB methods refer to the IR reflow and vapor phase processes commonly associated with surface mount [45]-[46]. These processes are applicable to larger pitch devices (> 0.015") and do not require significant deviation from the existing assembly culture for fine pitch SMT. The common metallurgy for these processes is solder, although conductive epoxy dispensed at individual pad locations is another possibility. Issues, such as lead coplanarity and the ability to screen or dispense controlled amounts of solder paste, force the user of fine pitch TAB devices (< 0.015") to consider alternate bonding methods.

Single Component Gang. Gang bonding techniques for OLB include hot bar thermocompression, hot bar reflow, hot gas and focused IR. Thermocompression gang bonding, like that of ILB, uses heat and pressure to form the metallurgical bonds, generally between gold leads and gold pads, or copper leads and copper pads. Limitations of this process include planarity of the leads and substrate, tool flatness and thermode temperature control.

Hot bar reflow, currently the most popular method of performing OLB, is a gang bonding technique typically applied to solder metallurgies. Flux is used to enhance solderability. A thermode with four heated blades is brought into contact with the leads and OLB pads. The temperature of this thermode is profiled to control reflow and resolidification. Contact pressure eliminates the coplanarity problem and provides for the even transfer of heat.

Hot gas gang bonding uses a heated gas, focused on the bonding area to the device. Like hot bar reflow, the temperature is profiled. An added bonus may be the gas acting as a substitute for fluxing. Disadvantages may include controlling the effects of the hot gas on neighboring components.

Focused IR uses infrared energy focused on the bond area to achieve

and lead hold down techniques, but promise fast, clean methods of performing OLB. One of the challenges in implementing laser OLB technology is finding a method that consistently holds the leads in contact with the pad. This is needed to facilitate the energy transfer between the two and form the bond.

Mechanical Bonds. Demountable TAB (DTAB) provides an easily repairable OLB connection and is a recent development [32]. The connection is made by pressure contact directly between the leads on the TAB tape and the vias on the PC board. DTAB offers a fluxless, solderless system with the added advantage of unlimited rework. Also, no excise and form are required.

Another quasi-mechanical bond involves the use of anisotropic epoxies (z-axis conductive epoxies). These materials eliminate the need for accurate screening since lateral bridging is not possible. A bonding method that applies pressure to activate the z-axis conductivity is needed however. Currently, these methods are used only in low current applications such as LCDs, since the joints are typically highly resistive compared to solder joints.

OLB Equipment Issues and Availability

Gang hot bar reflow and single point thermosonic bonders are the dominant equipment available. Generally the gang bonders have systems integrated onto one platform, enabling the entire OLB process to be performed on one piece of equipment, while the single point bonders perform only the bonding portion. The ability to place fine pitch components is critically dependent on both the motion and vision systems [47]-[48]. OLB pitches down to 0.004" pitch require linear accuracies of ±-0.0002" and rotational accuracies of ±-0.003°. The vision systems that drive such robotic placement systems have submicron resolution and should have the ability to make alignments based on pad locations, as opposed to fiducials. When selecting TAB OLB equipment, level of integration, placement accuracies and bonding capabilities must be considered.

Single Point Thermosonic. Thermosonic outer lead bonding is performed using modified wire bond equipment to bond the Au-plated TAB leads to the Au-plated OLB pads. These bonders, designed primarily for ILB applications (see Section 9.4.4), perform only the bonding step and do not have the capabilities integrated on one platform to perform the previous steps in the OLB process. This dictates that the excise and form through alignment and placement steps take place on a separate station. The device can be die attached or tack bonded on pick and place or gang bond equipment and then transported to the single point bonder and bonded. The die attach, or tack, prevents movement of the device during the initial bonds and transport. Table travel on these bonders, originally designed for objects the size of semiconductor die, can cause problems for multichip users with larger package sizes. Tool life and slower production cycle times are also issues. The equipment infrastructure for single point ILB

exists, but is somewhat immature for OLB applications. The cost of manual or semiautomatic thermosonic TAB bonders is around $200,000. The cost for placement, excise and other tooling needed for a complete OLB process can easily triple that amount.

Gang Hot Bar Reflow. The gang hot bar reflow method of performing OLBs is the most common technique of accomplishing OLB. Solder is the metallurgy of choice. This has allowed an infrastructure of bonding equipment vendors to supply fully integrated OLB machines based on this method. The most capable of these machines, equipped with component feeders, excise and form stations, fluxing, die attach dispensing and hot bar reflow thermodes, are integrated on precise, accurate robotic systems, capable of placing devices with pitches down to 0.004" (see Figure 9-22). Thermode improvements have been made, allowing the user better flatness and temperature control. Mechanisms are integrated into the bonding head, allowing for real time planarity adjustments, resulting in better solder joint consistency. The most advanced of these machines costs between $400,000 and $500,000 (1992 dollars).

9.4.6 Single Chip and MCM Implementations of TAB

Implementations of TAB in electronic packaging are classified into three broad categories: TAB as a buried interconnection, TAB on board and TAB in MCMs.

TAB as a Buried Interconnection

In a buried interconnection scheme, the ILBs and OLBs are buried inside a conventional package such as a plastic dual in-line package (PDIP), plastic leaded chip carrier (PLCC), plastic quad flat pack (PQFP) or pin grid array (PGA) similar to that shown in Figure 9-13 for cavity TAB. The TAB tape is inner lead bonded to the chip and outer lead bonded to a leadframe (PDIP, PLCC and PQFP) or to a metal land (PGA). The TAB part of the assembly is invisible to the final user of the package. National Semiconductor Corp. successfully used this approach in the 1970s as an alternative to wire bonding for the high volume production of low lead count PDIPs. Presently, this approach is envisioned as a way to overcome the pitch limitations of wire bonding without changing the external outline of packages such as PQFPs. This application has been called the TAB interposer.

TAB-on-Board Single Chip Packages

The TAB-on-board is basically a chip-on-board (COB) application. The TAB tape essentially comprises the package itself as the outer leads are directly attached to matching pads on the PWB. The most extensive application of this packaging scheme has been in the field of consumer electronics, such as LCDs, watches and calculators. Several proprietary packages have been developed by

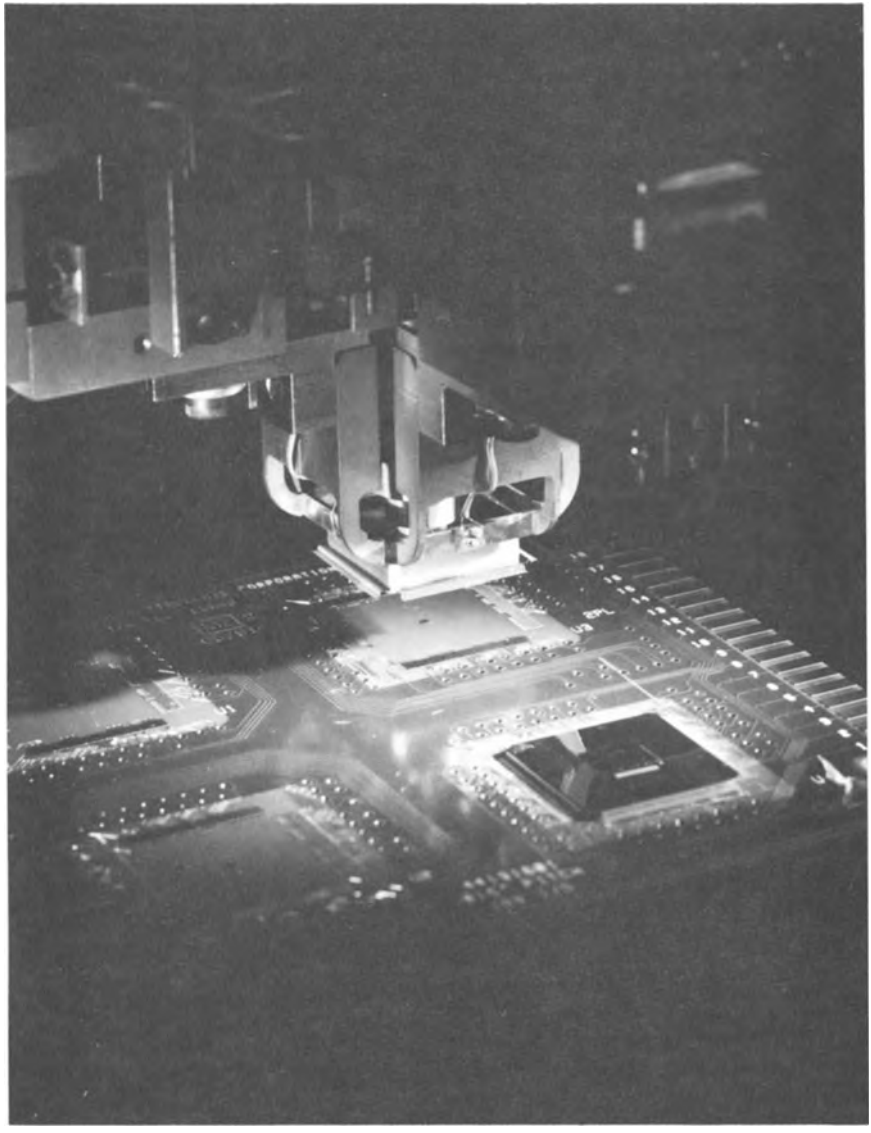


Figure 9-22 Hot bar OLB gang bonder. (Courtesy of Universal Instruments.)

companies for packaging high pin count VLSIs. The following are examples of TAB-on-board applications:

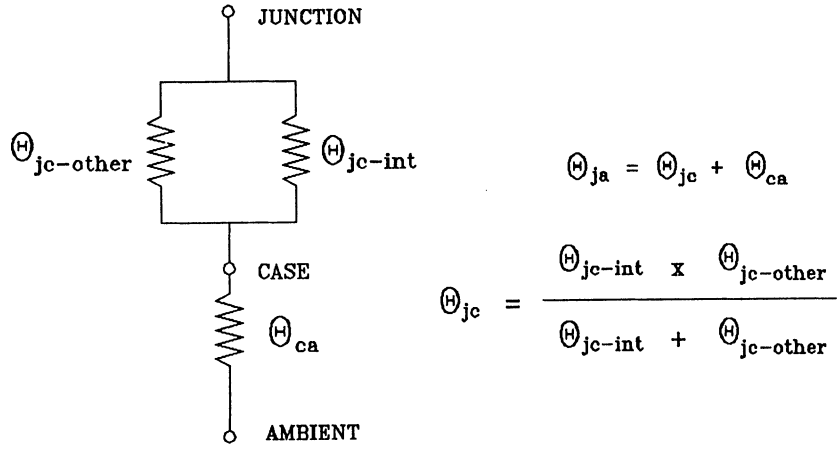


Figure 9-23 The role of interconnect in the thermal performance of a package.

1. Tape Pak™, National Semiconductor
2. Micropack™, Siemens
3. Tape Quad Flat Pack (TQFP), LSI Logic
4. TAB Pak™, Texas Instruments [33]
5. "Clamshell" ceramic package, Digital Equipment Corp. [39], [49]
6. TAB package with thermal spreader, Hewlett-Packard [50]
7. Demountable TAB (DTAB), Hewlett-Packard [32]

TAB MCM Implementations

Bull Corp., in France, first used TAB to package low lead count devices to thick film substrates. Honeywell reported the use of TAB with copper thick film substrates in the early 1980s, using a flip TAB format. Later work by Honeywell utilized a copper/polyimide thin film technology (TFML) and conventionally mounted TAB devices, discussed in Chapter 7.

A recent TAB application for MCMs is the DEC VAX-9000, discussed in Chapter 17. This application utilizes a copper/polyimide interconnect on a base substrate and tin-plated tape with solder OLB joints.

9.4.7 Thermal and Electrical Performance

The techniques used for thermal analysis and for thermal management of conventional single chip packages apply to TAB packages as well. Thermal

performance can be analyzed and enhanced using the same general techniques described in Chapter 12. One feature unique to TAB is the presence of copper beam leads that are massive when compared to wire bonded leads. These copper leads influence the heat flow out of a chip. As an example, the effective thermal resistance of a copper lead 0.050" long, 0.002" wide and 0.0014" thick is approximately 29 times lower than a looped gold wire 0.001" in diameter and 0.100" long. A simplified thermal resistance model of a TAB bonded chip is shown in Figure 9-23 [51]. The connection is shown as a separate heat flow path in parallel with other existing paths. The beneficial effects of TAB are realized in cases where Θ_{jc} dominates the overall thermal performance and $\Theta_{jc\text{-}int}$ is much smaller than $\Theta_{jc\text{-}other}$. The performance of two metal tape is slightly better than single metal tape since as the ground plane acts as an additional path for heat flow.

The general techniques for improving thermal performance, such as the use of heat spreaders, heatsinks, forced air flow and liquid cooling apply to TAB packages in much the same way they would any other package. Extremely high performance TAB packages, both in single chip packaging and in MCM implementations, have utilized one or more of the above techniques [32].

Thermal characteristics are specific to the particular TAB configuration (conventional, flip, etc.) selected for a particular MCM application. Conventional and cavity TAB conduct heat out of the back side of the die and through the substrate material, similar to that of wire bonding. Flip TAB, on the other hand, requires more elaborate heat dissipation structures since the back side of the die is not directly attached to any thermal conduction path. These structures include finely toleranced and expensive heat spreaders as well as liquid cooling methods.

Electrical

The electrical performance of any IC package is analyzed in terms of the environment it presents to signal transmission and to the distribution of power, as discussed in Chapter 11. The electrical characteristics of a TAB package also are best presented in this form. A schematic illustration of the signal environment presented by a TAB lead is shown in Figure 9-24 [52]. It is assumed that the TAB lead terminates in a controlled impedance transmission line representing the environment outside the package. The lead represents an uncontrolled impedance between the chip and the outside environment. The values of relevant electrical parameters applicable to the case of a typical TAB lead (assuming a 48 mm TAB tape format, copper leads 0.002" wide and 0.0014" thick at 0.002"/0.002" line and space in the ILB area) are shown in Table 9-20. The values have a range based on the longest and shortest leads typical for this tape format. Table 9-20 also shows a comparison between one and two metal tapes. In two metal tape (see Figure 9-19), a substantial portion

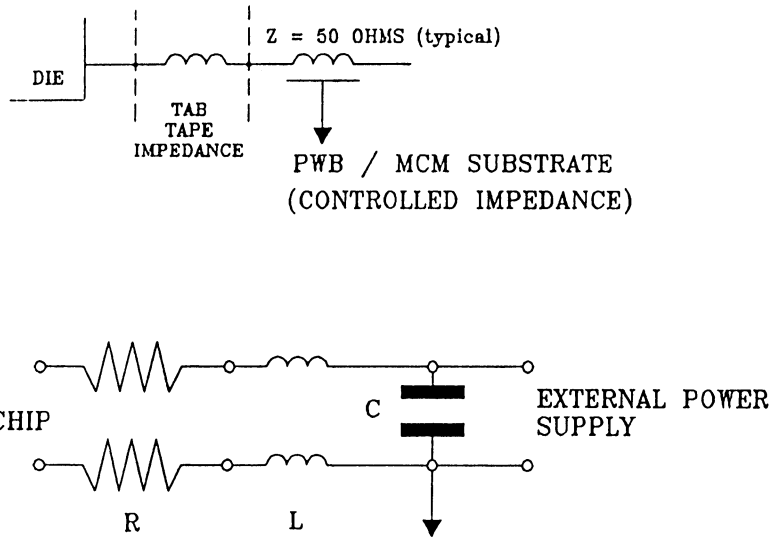


Figure 9-24 Electrical characteristics of TAB: (a) signal environment, (b) power environment.

failure mode is that of the TAB lead itself and the OLB joint. These failures are mechanically induced by temperature cycles [53]. Transient stresses result from rapid temperature excursions and steady state stresses from the inherent differences in the CTEs among the principal materials. Failures are investigated using liquid to liquid thermal shock (LTS) or thermal cycling tests. Finite element analysis has identified regions of high stress in given outer lead configurations. These studies reveal the TAB leads as the apparent weak link in the mechanical assembly. This is due primarily to the relatively smaller cross sectional area of the TAB lead compared to that of surface mount leads. Mechanical stresses from shock and vibration result in similar failure modes. When performing shock and vibration testing, it is important to perform such tests in the final box configuration, since the failures are particularly sensitive to resonant frequencies that may be specific to the design of the box. Other mechanical areas of concern, with regard to reliability of the TAB tape are metal to dielectric delamination and dielectric expansion. Chemically caused failures may relate to the moisture absorption of the dielectric or plating inconsistencies. These are closely related to ILB and OLB failures and discussed below.

ILB Joints

Failures occur due to the gradual degradation of the ILB. A variety of modes are possible:

- Separation between the bump and die pad due to insufficient cleaning of the Al prior to the deposition of the bump metallization
- Failure of the under bump metallization to prevent interdiffusion between the Au and Al
- Separation between the bump and TAB lead due to contamination at the bump and lead interface and
- Separation between the TAB lead and bump interface due to intermetallic formation, particularly in reflow bonded joints.

Physical causes may be induced by assembly process issues (such as very restrictive process windows) and material issues (such as poor lead frame design and material selection). Chemical corrosion can be induced by moisture penetration through the encapsulant or passivation and is largely due to the presence of halides, remnants of the encapsulation or OLB (flux) processes. Moisture is absorbed by the dielectric material during tape manufacturing and handling. Plating issues, such as contaminants, variable thicknesses and shelf life also contribute to the ILB failures listed above. The majority of the above failure modes is characterized using HAST (highly accelerated stress test) and LTS testing. The HAST test uncovers chemically induced failures while the LTS uncovers mechanical failures.

OLB Joints

OLB metallurgies are predominantly solder or Au to Au. As mentioned previously, studies have determined that the TAB lead is more likely to mechanically fail than the solder joint [28]. The point of issue is the quality of the solder joint itself. Gang reflowed solder joints show non-uniformity based on thermode temperature variations or planarity and flatness problems. This can result in good reflowed joints, as well as incomplete reflowed solder joints on the same device which, in turn, can result in mechanical failures in the poor quality solder joints. Chemically, the choice of tape plating effects the quality of the solder joints. Tin-plated tape is subject to shelf life and oxidation concerns and results in poor solder joints if used beyond it's expected life or is not stored properly. Gold plated tapes used with tin-lead solder systems can form brittle intermetallics in the solder joint. This necessitates control of the gold content in the solder joint and may even preclude the use of gold solder OLB systems in finer pitch TAB devices. The maturity of gold to gold thermosonic bonding for OLB is low and reliability information comparable to that available for solder OLB is scarce, if not nonexistent.

Another interesting failure, chemical in nature, involves the migration of metal between adjacent leads under an applied potential, leading to low resistance leakage paths or even complete electrical shorts by bridging. This phenomenon

has also been identified in the field, caused presumably by the existence of constant voltage across adjacent leads in certain logic devices. The failure has been found to occur profusely between leads with exposed copper over a polyimide surface. It can also occur in tin plated leads and is termed tin migration. Metal migration can be largely prevented by suitably plating leads to seal any exposed copper and by close control of the polyimide quality during tape manufacture. Generally, the finer the pitch and the higher the voltage gradient between adjacent leads, the higher the probability of metal migration failure. Potential failures due to metal migration can be typically uncovered using the HAST test with the application of a bias across nearest neighbor leads while monitoring any leakage currents. Tin plating also causes a potential reliability problem due to a phenomenon known as tin whiskering. Needle-like whiskers grow from the plating as a result of stresses introduced during the plating process. Especially on fine pitch devices, this can potentially cause lead to lead shorting.

9.4.9 Reworkability

The failure of even one device on a MCM can render the package useless; the high cost of an assembled MCM prohibits simply throwing it away. This necessitates processes that can rework TAB assembly errors and actually remove and replace failed TAB devices. This rework effort is usually focused on the OLB level of the assembly. ILBs are, generally, not considered candidates for repair unless the high cost of the die necessitates it. Even then, rework is limited to repairing open leads using single point methods. Considerations prior to deciding whether and what is to repair include the effort and costs involved, the equipment and methods available and the effects on neighboring die on the MCM.

Reworking Assembly Errors

The rework of TAB OLB assembly errors usually involves the bonding of unbonded leads, removing solder that is shorting between two pads, removing solder balls and repositioning misaligned leads [28]. Although methods and equipment are available for making these repairs, with regard to solder OLB metallurgies, the processes for these corrective actions may be labor intensive. Solder joint inspection systems, in some cases, can be integrated with single point reflow equipment to perform some of these repairs. Correcting assembly problems related to gold to gold thermosonic bonds can be more difficult. While repairing an open lead may be a relatively easy task for the single point thermosonic bonder, repositioning misaligned leads may prove challenging due to the nature of the gold to gold bond.

Removal and Replacement

The process of removal and replacement of failed TAB devices is justified, especially in MCM applications, when the cost of the remaining good die and package outweigh the cost of discarding the assembly. Solder OLB systems and mechanically bonded MCMs present the greatest potential for repairs of this type. The general process flow for this type of process involves: removing the component, cleaning and dressing the OLB pads with new solder and positioning a new component.

Removing the Component. With regard to solder OLB systems, removing the component involves mass reflow of the OLBs followed by the lifting of the device when the solder is at a liquid state. The die attach bond (epoxy), if present, also has to be broken during this process. The TAB leads separate from the OLB pads and, together with the die, are lifted from the package surface, preferably intact. The removal process can be viewed as a reversal of the original gang bond process and is done with hot bar, hot gas and infrared heating. Hot bar is currently the best option, due to it's superior thermal transfer and reduced effects on neighboring devices.

Redressing OLB Pads. Following the device removal, the OLB area must be cleaned and re-dressed. This may include reflowing the solder left on the OLB pads or actually replacing solder removed with the leads of the original TAB device. Various methods, some proprietary, have been proposed for redressing the solder pads and the choice depends on the package types and OLB pitch [54].

Component Replacement. The new component can be bonded to the repair site following the clean and redress step using the original OLB process.

Rework Issues

Critical decisions made early in the design phase of MCMs should include the TAB configuration (conventional, flip etc.) and tape and substrate metallurgies. Flip TAB designs lend themselves to an easier repair strategy since the use of a die attach material is usually absent. Conventional TAB designs, on the other hand, require the added step of breaking the bond of the die attach material. This can be a difficult and messy task. Metallurgical problems can also make the removal process difficult. Tin plated tapes contribute copper-tin intermetallics to the solder joint, raising the reflow temperature of the solder and making the removal difficult and sometimes impossible after high temperature/time exposures. Gold plated tapes form a brittle gold-tin intermetallic when soldered, not only affecting the reliability of the joint but raising the reflow temperature of the solder. The removal and repair of gold to gold thermosonic bonds is a more difficult process. Reasons relate to the original bonding methodology (single point) and the related bond metallurgy.