Table 3-3 Performance and Cost Factors.

PERFORMANCE FACTORS
1. Size and weight 2. Interconnection capacity within each interconnection level 3. Connection capacity between interconnection levels 4. Electrical delay and noise 5. Power consumption 6. Heat dissipation
COST FACTORS
1. Production cost: a. Manufacturing cost (setting up the manufacturing line and buying the required materials) b. Manufacturability costs (running the manufacturing line, mainly the impact of test and yield) 2. Post production costs: (mainly replacing failed units—the effect of field reliability) 3. Design and prototyping costs 4. Time-to-market

process can be broken down into steps, some of which are carried out simultaneously:

1. Determine requirements and goals of the system.
2. Express requirements and goals in terms of performance and cost factors.
3. Determine partitioning and packaging alternatives.
4. Evaluate performance and cost of design alternatives in terms of performance and cost factors.
5. Decide on alternative that best meets the system's aims.

These are discussed and an example given in the next section.

3.7 DETERMINING SYSTEM REQUIREMENTS AND GOALS

The requirements of the system are the "must haves," those aspects of

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performance and price that the system must achieve. These become constraints on the performance and cost factors. The goals of the system are the "want to haves," those aspects of performance and price where maximization is highly desirable. Satisfaction of the goals must be judged in terms of tradeoffs between the performance and cost factors. One of the first steps in system design is to determine the requirements and goals and to determine the relative weight or importance of each one. These requirements and goals should closely match those of the end customer.

Six categories of electronic systems were identified in Chapter 1: consumer, aerospace and military, computers, biomedical and telecommunications and instrumentation. Each of these system types has different requirements and goals related to packaging performance and cost.

For example, most consumer products have a requirement that they be passively air cooled (no fan). Their goals are heavily weighed towards minimizing production cost, followed by maximizing customer satisfaction (minimizing post production costs) and minimizing size and weight. Rarely, is minimizing electrical delay an important goal.

Aerospace and military products tend to emphasize performance and post production cost factors in their goals. However, they often are given minimum requirements in terms of these factors. For example, a radar signal processor might be required to resolve a target with a 1 meter squared radar cross section at 100 miles, fit into one electronics bay, and the technician must be able to locate and repair a fault within half an hour. They usually must be air cooled. A recent trend has been to pay increased importance to minimizing production cost.

The requirements and goals of a computer system depend on the application. For example, a desktop workstation might have requirements that it be air cooled with a quiet fan, be software compatible with previous models and meet federal EMI standards. The goals of the system are to maximize computation performance while controlling cost. Marketing studies determine suitable minimum targets for these goals. It is shown in Section 3-10 how workstation performance depends on interconnect capacity and delay. On the other hand, a notebook computer must be passively air cooled and must be able to use a certain chip set. Ergonomics and price drive the goals of the system. Total system size, weight and user friendliness, together with battery life (power consumption) and selling price, all are given similar weight.

At the other end of the scale, supercomputer and mainframe applications require high performance, while cost is secondary. These applications require high interconnection capacities throughout the entire system. Designers need to avoid the low interconnection capacities usually associated with the higher levels of the packaging hierarchy. Thus, they tend to make extensive use of MCM

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technology. An unusual performance goal, sometimes appearing in large systems such as a supercomputer, is the need for scalability-the ability to make the same system in several different sizes without redesigning the system for each size. An example is being able to expand a system with 512 processors to one with 1024 processors, without having to slow down the system to compensate for the larger size.

The aims in biomedical systems vary widely according to application. However, they have tended to emphasize performance and post production cost factors over production cost.

In main telecommunications switches, international standards dictate many requirements for performance. The need to minimize system down time for maintenance and failures often is translated into a set of post production requirements and goals. For example, it is a common requirement that the switches be air cooled to simplify maintenance and repair. It also must be possible to run the system on batteries if main power fails. The goals of the system then are to maximize bandwidth (a function of interconnect capacity and electrical delay) and minimize life cycle cost.

High end instrumentation systems, such as test equipment, often must operate at higher speeds than the systems they are designed to test. The pin counts of the high speed bipolar and gallium arsenide parts used usually have been low. Thus, hybrid packaging has been a common solution. Recently, the sizes and pin counts of chips made in these technologies have increased dramatically. As the pin counts climb, it becomes necessary to use packaging technologies that combine high interconnect capacity and high speed, such as an MCM technology.

3.8 DETERMINING AND EVALUATING PACKAGING ALTERNATIVES

Currently, the process of determining a set of suitable packaging alternatives requires that the designer have some insight into the broad range of alternatives available and how their relationship to the requirements and goals of the system. No general methodology for generating these alternatives exists today. Often, the alternatives are discovered during the evaluation process, so the current emphasis is on making this evaluation process as efficient as possible. Partitioning alternatives usually are generated on the basis that functions should be grouped into chips and packages to minimize the need for high cost connections between the different levels of the packaging hierarchy.

There are two levels of evaluation possible. First order evaluations use simple performance and cost measures and models, such as substrate efficiency

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and time of flight delay, to quickly evaluate a large number of alternatives [1], [8] and [9]. Computer aided engineering (CAE) tools, such as SPEC [10] and PEPPER [11], are becoming more available to help with this task. These first order evaluations often are useful in weeding out unsuitable alternatives. It often is necessary to conduct detailed evaluations to make the final decision and to determine the system parameters (such as the clock frequency). Detailed evaluations might be necessary when the possible options could violate a specific systems requirement (if the heat density is so high that air cooling might be difficult). CAE tools are helpful in this task (MetaSim [12] for electrical delay and the routability estimators included in commercial tools). SPEC and PEPPER have some of these detailed evaluations built in.

3.9 IMPACT OF SEMICONDUCTOR TECHNOLOGY

The designer must decide which semiconductor technology to use: CMOS, bipolar, BiCMOS (bipolar and CMOS mixed together) or gallium arsenide, and which chip design style to use. The design style has two elements: circuit style (TTL or ECL logic families) and implementation style (gate array or full custom design). The choice affects the decision making process as follows:

1. Determines the delay within each chip, both due to the circuits within the chip and the on-chip wiring.
2. Determines how many functions can be provided within one chip. This is highest with CMOS technology. Large CMOS chips also tend to have high pin counts.
3. Determines the on-chip interconnection capacity. This is generally high.
4. Determines the power dissipated by the chip. This is high now, even for CMOS chips. There is a speed/power tradeoff to be considered.
5. Determines semiconductor technology to use. Bipolar chips have lower test escape probabilities than CMOS chips.
6. Determines cost. Large, complex chips have a cost usually greater than the first level package cost.

3.10 EXAMPLE OF THE SYSTEM DESIGN PROCESS

In many computer products, particularly workstations, packaging technology has a main influence on system performance through its impact on memory access bandwidth. The memory is structured as a hierarchy (Figure 3-16), usually with

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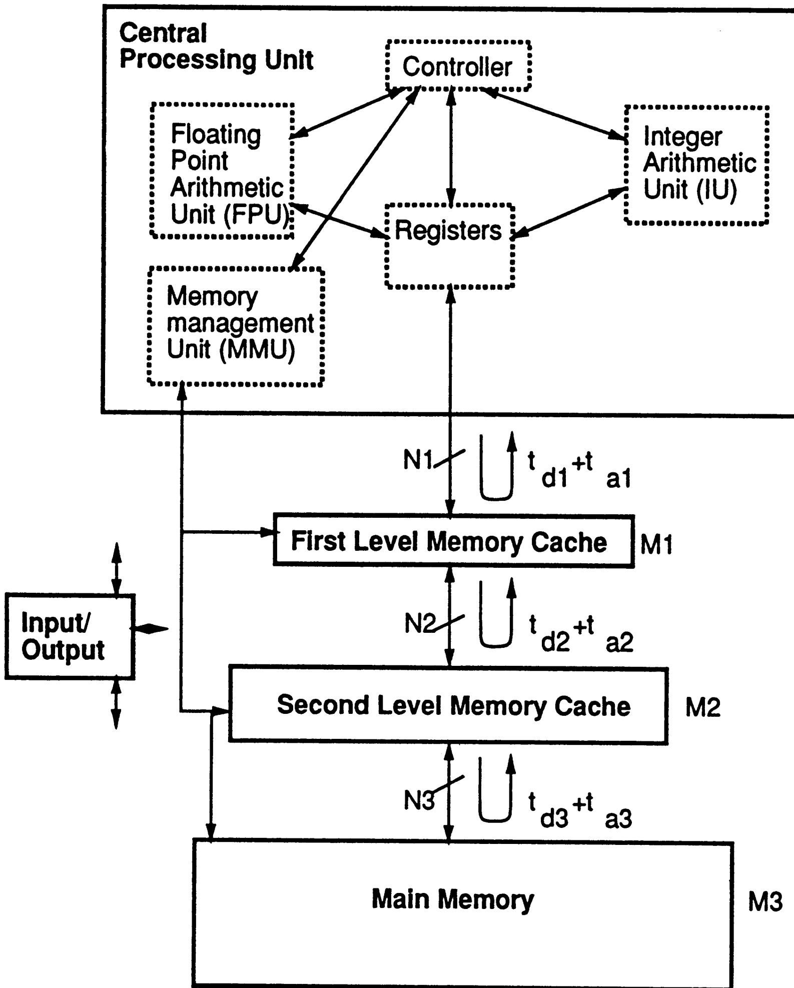

N_i = Number of bits fetched each access

$t_{di} + t_{ai}$ = Total round trip delay to fetch bits

M_i = Number of bytes at each level

Figure 3-16 Block diagram of the main elements in a single CPU computer. Packaging affects workstation performance through the widths and speed of the data paths between each level of the memory hierarchy.

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a small amount of fast memory (first level cache) at the top of the hierarchy and a large amount of slow memory (main memory) at the bottom. This is part of the system organization. It is possible to write expressions that relate the computation performance of the system to the number of bits communicating between each level of the memory hierarchy (also called the fetch size, N1, N2 and N3, as shown in Figure 3-16), the interconnect delay between each level (t_{d1}, t_{d2}, t_{d3}), the memory access time of each level (how long it takes to fetch a memory location for each memory chip t_{a1}, t_{a2} and t_{a3}) and the number of memory locations at each level (M1, M2 and M3). The performance is expressed as a function or model:

$$\text{Memory Performance} = f(N1, N2\ N3, t_{d1} + t_{a1}, t_{d2} + t_{a1}, t_{d3} + t_{a3}, M1, M2, M3) \tag{3-16}$$

The elements in this expression relate directly to packaging performance factors [13], [14] and [15]. This function tends to be most sensitive to the attributes $t_{d1} + t_{a1}$, M1 and N2 (N1 is usually fixed), and reasonably sensitive to M2 and $t_{d2} + t_{a2}$.

The choice of partitioning and packaging style has a large influence on the fetch sizes and interconnect delays. For example, the first level cache often is packaged with the CPU on one chip, allowing a minimum $t_{d1} + t_{a1}$. However, in 1992 technologies, this limits M1 to 8 - 16 kBytes, which really is too small. This is the case assumed here.

The progress of the IC technology (and the ability to integrate a fast, large, first level cache onto the CPU chip with good yields) must not be neglected. In particular, a company may decide not to pursue developing an MCM technology for its computer chips if an anticipated small chip MCM product would only have a two year performance lead on the equivalent function packaged entirely within one chip [16].

With the first level cache placed on the CPU chip, packaging determines performance mainly through its effect on N2, M2 and t_{d2}. Three options are presented and discussed here: a single chip package/PWB option, a laminate MCM option and a flip chip thin film MCM option.

If the CPU is packaged in a PGA, N2 is typically limited to 32 bits to 128 bits, to limit the PGA pin count, and t_{d2} might be as large as 23.1 ns. (Delays used here are based on the evaluations provided in reference [17].) This option provides the worst (though not bad) performance at the least cost.

The simplest MCM alternative is to package the CPU chip(s) as bare die on a fine pitch laminate MCM, either with TAB or wire bonded chip attach, and then connect the memories as single chip packages. This reduces the fanout and CPU footprint, decreasing t_{d2} and allowing for a modest increase in N1. The

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memories are left in their single chip packages because their footprint is barely larger than that of the bare die (they only require 20 or so pins). This also simplifies memory testing. t_{d2} is decreased from 23.1 ns to 17.9 ns, a 5.2 ns decrease. With the increased interconnect density it is possible to increase N1 to 128 bits or more. Based on assumptions beyond the scope of this text, a computation performance increase of around 11% is gained over the single chip package option.

With this laminate, the impact of thermal considerations is likely to be low. Thermal vias are used beneath the CPU but, if the chip is designed so that few signals run underneath this chip, then the impact on interconnection capacity is small. Manufacturing costs are low, possibly lower than the cost of using ceramic PGAs on a PWB, and the manufacturability cost also is low. In particular, the memory chips are easy to rework. It also might be possible to avoid reworking the CPU if it is a single die. The CPU can be tested after mounting it on the laminate, before mounting the memories, and scrapped with the low cost laminate if it fails. Other cost impacts also can be kept low. Sealing the bare chips in epoxy delivers sufficient environmental sealing at a low cost, and adequate mounting to the next level of packaging is through an standard edge connector. Overall, the price premium over the conventional option is small.

The most aggressive MCM alternative, in terms of performance, is to use flip chip solder bumps on a thin film MCM. With this approach, N2 can be very high and the shortest possible interconnection delay, short of using some three-dimensional technology, can be obtained. Then t_{d2} is decreased further 3.1 ns delay over the laminate approach when the memories are packed in short lead TAB frames and mounted on a thin film substrate [17]. The fetch size, N2, can be substantial, possibly even 512 bits or more. The overall computation performance increase over the single chip package option is about 20%.

The price premium is several hundred dollars however, and the risk of delayed time-to-market moderate unless close relationships had been established with parts suppliers and a carefully worked out test plan is used. If a silicon substrate is used, the cost of the package (typically a large ceramic PGA) can be higher than the substrate itself, possibly even $200 to $300. Manufacturability costs are higher as all the difficulties of working with bare die must be incorporated. An offsetting factor is that solder bump technology is the easiest bare die attach technology with which to do rework. If there is insufficient experience with flip chip thin film MCMs in the company, the risk and time-to-market impacts might be high. These considerations should be balanced against the performance gains.

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3.11 SUMMARY

System design may be driven primarily by performance, by cost or by the desire to maximize the ratio of performance to cost. Due to continuing rapid advances in chip technology, as well as advances in customer's needs, the lowest cost packaging alternative often does not return satisfactory performance. This has led to a growing need for advanced, customized packaging. MCM technology represents the high performance end of advanced packaging technology.

The use of MCMs leads to improved system performance through the ability to pack the chips close together. This ability arises from the tight line and via pitches possible with MCM technology. These tight pitches reduce the impact of chip fanout on chip footprint, and results in sufficient interconnect capacity being available in a small area. This ability results in a reduction in interchip delay as compared with the conventional package alternatives. The reduction in delay is largest if the chips being packaged have high pin counts, as such high pin counts normally require a large fanout package and create a strong demand for wiring. For example, the size difference between a multiple 500 pin PGA mounted microprocessor array and the equivalent MCM mounted array is large, while the size difference between a surface mount packaged memory array and the equivalent MCM mounted array is small. In the former case, if system performance is very dependent on reducing interchip delays, the performance advantages of using MCMs are large. A further gain in performance comes about because the MCM-based solution fits onto fewer PWBs, reducing the need for higher levels of packaging in the packaging hierarchy. This allows the parts of the system to be more richly interconnected. The advantage is greatest with thin film MCMs, least with laminate MCMs. In all cases, however, the use of MCMs reduces size, weight and interconnect delays, and increases the total number of connections available.

The above discussion applies to the use of both large and small (< 10 chip) MCMs. Sometimes an alternative to a small MCM is to fabricate a single large ASIC chip. This is reasonable if the chip can be produced with sufficiently high yield. However, it is unreasonable if the production volume is too small to justify the extra design cost, if the time-to-market requirements are too short to justify the extra design time or if different semiconductor technologies have to be integrated.

There are a number of potential disadvantages to using an MCM solution. The heat density is higher, possibly requiring a more expensive heat dissipation solution. The manufacturing cost is likely to be higher, more so for thin film and high layer count cofired MCMs than for laminate MCMs. The test cost almost certainly is higher when bare die are packaged on MCMs rather than in

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easily tested, single chip packages. At the time of writing the risk of increased time-to-market is also greater with a bare die MCM solution due mostly to some infrastructure deficiencies. However, the infrastructure situation is improving rapidly.

Thus, the engineer must select the most appropriate technology mix for each system. This must be done by evaluating different packaging and partitioning alternatives against the system cost and performance goals. This is best done through the use of clearly identified cost and performance factors. For an advanced system, a large number of alternative courses of action should be generated, evaluated and compared using suitably detailed models and simulations. Only then can it be determined if the extra cost of advanced packaging can be justified by the system's needs. This process also enables the designer to determine which functional blocks in the system benefits most from the use of advanced packaging. As a general rule, the most highly connected functional blocks tend to benefit more from advanced packaging than lowly connected functional blocks, such as memories.

A somewhat idealized approach has been presented in which the system's cost and performance aims are clear and can be modeled numerically, as can the performance and cost of the different options. Unfortunately, this is not always the case. The customer's requirements might be vague and ill formed. In this case, scalability and flexibility of the solution becomes an important factor. Also, all of the models needed to do the evaluation might not exist. Quantifying time-to-market and test costs might be difficult. Nevertheless, by qualitatively understanding how the different performance and cost factors relate packaging alternatives to the systems aims, it is still possible to arrive at a sensible solution.

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4

MCM PACKAGE SELECTION: COST ISSUES

Lee Hong Ng

4.1 INTRODUCTION

In the design of electronics packaging systems, there is rarely a single "best" solution; the final design is usually a tradeoff between different performance attributes (system speed, thermal constraints or size) and cost. In many cases, tradeoffs between cost and performance are the most important. Unfortunately, the analysis of cost and performance tradeoffs is a very complex task. On the performance end, the vast variety of design options available today to the packaging engineer precludes an exhaustive analysis of all viable alternatives. On the cost end, the treatment usually is even more cursory because of the complexity and uncertainty of cost before actual production.

While many may argue that performance analysis is more important in the design phase, one must be aware that cost is very dependent on the product design. In fact, up to 80% of the cost of a product is determined in the design phase [1]. If a design decision is based primarily on performance, one may discover, after the decision is made, that a slight modification might have lowered the cost drastically without an appreciable degradation in performance.

Obviously, both cost and performance issues must be addressed at the design phase to minimize sub-optimization. The designer must be able to think across the boundaries of different packaging approaches to optimize cost and

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performance for a specific design. In the previous chapter, cost was divided into four factors: production cost, post production cost (reliability, repair and maintainability), design and prototyping cost and time to market cost impacts. In this chapter, details about how to model production cost and examples of the cost considerations of all of these cost factors are given. Sections 4.2 to 4.5 present technical cost modeling (TCM) and its application to making cost-based decisions for MCMs and PWBs. The cost modeling approach presented in these sections is a process-based cost model. Section 4.6 discusses an alternative form of cost modeling used by a design bureau when it does not have access to manufacturing process information but does have access to vendor pricing information. This model is referred to as a design activity-based cost model.

4.1.1 The Importance of Cost

Product costing is important for strategic decisions, cost and performance evaluation, product pricing and product design, as well as to improve and manage existing operations. For example, product cost information is used by management to decide which products the company should drop to be more profitable, or it may be used to formulate a strategy for the company based upon its cost advantages in certain products. If the product cost information is inaccurate or biased, insensible decisions may result.

Product costing also is important in material and process selection, as well as to target areas for cost improvement and optimization. A consistent product costing framework also can be used to assess the cost position of suppliers, competitors and customers, and to evaluate "make versus buy" decisions.

Accurate product costing is especially important at the design phase where more than 80% of the cost of a product is determined. To be useful, cost evaluation at the design phase must incorporate the effects of design and manufacturing processes. This ensures that the design offering the optimum combination of cost and performance is selected. In many cases, process selection decisions also are made at the same time using product costing information. Thus, errors in product costing at this stage results in non-optimum designs being selected.

In many applications, the direct manufacturing cost is only a small part of the total system costs. The total system costs include operational cost such as fuel and power consumption, cost of cooling, prototype design and testing, repair and higher level connections. Again, all of these must be included in the cost analysis to minimize sub-optimization at the system level.

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Table 4-1 Example of Equations for Traditional Cost Estimation.

$$\textit{Cost} = \textit{Materials} + \textit{Labor Cost} \cdot (1 + \textbf{BURDEN}) + \textit{Tooling}$$

$$\text{Material Cost} = \frac{\text{Part Weight} \cdot \text{Material Price}}{(1 - \text{Scrap})}$$

$$\text{Labor Cost} = \text{CycleTime} \cdot \text{Labor Wage}$$

$$\textbf{BURDEN} = \text{Other Costs (Depreciation, Energy, Indirect Costs)}$$

$$\text{Tooling} = \text{Cost of Tooling and Setup}$$

4.2 TECHNIQUES FOR COST ANALYSIS

There are many methods available today to analyze the cost of products. They are broadly categorized into three methods: traditional cost analysis, activity-based cost analysis and technical cost modeling.

4.2.1 Traditional Cost Analysis

Traditionally, the task of cost analysis has been delegated to accountants, who are more familiar with the financial rather than the manufacturing aspect of a product. Traditional cost accounting systems, invented in the early 1900s, typically calculate the cost of a product based upon the labor content required for the product. Burden or overhead then is added to the product as a percentage of direct labor (or touch labor). Table 4-1 shows an example of the equations used in traditional cost estimation, and Table 4-2 shows an example of how burden or overhead rate is estimated [2].

In multi-step operations, the cost of a product is the sum of all the unit operations, each of which is estimated from the labor hours and materials required, adjusted by yield. Table 4-3 shows an example of the traditional cost analysis as applied to the assembly of a MCM [3]. In Table 4-3, the total material cost per module is $4,214.84 and total labor hour is 10.66 hours. Assuming that the overhead is 500% of direct labor cost of $12/hr, the total variable cost per module is $4,854 ($4,214.84 + 10.66 × $12 × 500%).

Traditional cost analysis works well when labor cost is the most influential cost driver. As manufacturing becomes more complex and automated, labor cost

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Table 4-2 Variable Burden Calculation.

General Ledger

#	Item	Date	Materials	Labor	Energy . . .
1	Memory Chips	1/1/90	$200,000		
2	National Electric	1/1/90			$5,000
3	Resistors	1/5/90	$30,000		
4	Circuit Boards	1/10/90	$90,000		
5	National Electric	1/15/90			$6,000
6	Monthly Salaries	1/31/90		$50,000	
7	FICA Payment	1/31/90		$6,000	
.			$320,000	$56,000	$11,000

Monthly Costs

	($000)	(%)
Direct Costs		
Materials	$320	60.2%
Direct Labor	$56	10.5%
Energy	$11	2.1%
Depreciation Costs		
Equipment	$108	20.3%
Building s	37	7.0%
	$532	100.0%

Variable Burden = "Other Costs" ($11+$108+$37) / Labor Cost ($56) = 279%

Table 4-3 Traditional Cost Analysis for Assembly of MCMs.

Assumptions	
Glue Logic Die /Module	29
VLSI Die/Module	12
Sub. Test Socket Cost	300
Good Die /VLSI Wafer	40

Wafer Cost	$4,000
Substrate Cost	$313
Packaged/Lid Cost	$234
Passive Cost	$0.85
Cost/Logic Die	$1
Passives/Module	25

Task	Lab. Hrs./ Module	Mat'ls/ Module	Yield	Yielded Hrs/MOD	Yielded Mat'l/MOD
Attach Glue Logic	0.50	$342.00	99%	0.56	$386.20
Wirebond Glue logic	1.00		99%	1.12	$0.00
Logic Test/Repair	0.50	$1.90	96%	0.55	$2.10
Passives Attach	0.50	$21.00	100%	0.53	$22.31
Attach VLSI Devices	0.12	$1200.00	99%	0.13	$1,274.98
Wirebond VLSI Devices	0.60		99%	0.63	$0.00
VLSI Test/Repair	3	$1110.00	97%	3.12	$1,155.89
Scrap	3	$1137.00	100%	3.00	$1,137.00
Substrate-Pkg Attach	0.50	$234.00	100%	0.51	$236.36
Wirebond	0.20		100%	0.20	$0.00
Bond Monitor	0.10		100%	0.10	$0.00
To/From Test			99%	0.00	$0.00
Package Seal	0.20		100%	0.20	$0.00
Environmental Test	0.00		100%	0.00	$0.00
To Test			99%	0.00	$0.00
Subtotal				10.66	$4,214.84

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becomes a smaller and smaller percentage of the total cost, while overhead becomes a larger and larger percentage. In fact, it has been reported that direct labor cost may be as low as 10% of product cost today [3], and yet more than 75% of the cost reduction effort reported was directed towards reducing labor cost. Since overhead typically is spread across the company or department arbitrarily, the cost calculated using such a method can be misleading [4]-[7].

Consider the case of a product manager trying to reduce the cost of a product using traditional cost accounting. Since the cost of the product is tied to direct labor, his or her first instinct is to reduce labor, which is equivalent to increasing throughput. By purchasing more automated equipment, the direct labor, and hence product cost, can be reduced. But a few months later, the overhead for the department increased because of the investment in the new equipment.

While the example is simplistic, it does illustrate how traditional accounting methods can mislead management decisions. Other shortcomings of traditional cost accounting methods include an insensitivity to production volume, tooling cost and other important manufacturing parameters. More important, it is difficult to justify approaches, such as Just-In-Time (JIT) manufacturing where inventory is kept to a minimum, Computer Integrated Manufacturing (CIM), manufacturing flexibility or automation using a cost estimation method based upon labor [8].

4.2.2 Activity-Based Cost Analysis

One way to overcome the problem is through the use of activity-based cost accounting (ABC) which traces costs to products according to the activities performed on them. The basic steps in establishing an activity-based cost system are listed below [9]:

1. Relevant activities (receiving, production, etc.) are identified.
2. Activities are organized by activity center.
3. Costs of the activities are determined.
4. A "cost driver" or allocation basis that relates the consumption of activities by product is identified.

Table 4-4 compares the allocation bases for the traditional and ABC systems [1]. In Table 4-4, the cost of purchasing is allocated to a product based upon the number of purchase orders (POs) issued for the product instead of the usual labor hours allocation. In this way, a product requiring multiple parts, and hence multiple POs, will cost more than one with fewer parts. Similarly, the cost of production setup is allocated based upon production changeovers rather than labor hours to better reflect cost.

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Table 4-4 Allocation Bases for Traditional and ABC Systems.

INDIRECT COST	TRADITIONAL	ABC
Production Control	Labor hours	Parts planned
Inspection	Labor hours	Inspection
Warehousing	Labor hours	Store receipts and issues
Purchasing	Labor hours	Purchase orders
Receiving	Labor hours	Dock receipts
Production Steps	Labor hours	Production change overs

The key feature of ABC is that it indicates what products, customers, processes and product attributes create overhead cost. Since only traceable costs are controllable, the biggest benefit of using ABC is overhead control. ABC also can be used for cost justification for automation, total quality management (TQM) and just-in-time (JIT) manufacturing.

While ABC clearly improves the accuracy of product cost estimates, it has been argued that ABC may not be appropriate for strategic planning because it is an accounting system designed primarily for external financial reporting purposes [10]. In strategic planning and product design, it is important for managers to understand how manufacturing processes and technologies affect product design and cost. One way to do this is through the use of Technical Cost Modeling (TCM), a concept developed at M.I.T. [11]-[12].

4.2.3 Technical Cost Modeling

Unlike ABC, which is an accounting system, TCM is a process-based model which simulates the manufacturing operations to estimate cost. Thus, it is an *a priori* cost model based upon manufacturing simulation, rather than an *ex post* cost model based upon historical accounting data. As such, it can be used to estimate cost for hypothetical processes and product before actual production, and in designing the product for minimum cost (design-for-manufacturability).

Technical cost models can be probabilistic (stochastic) or deterministic. A probabilistic model requires the key input variables to be specified as probability distribution. Since the distributions are rarely vigorously measured, they are

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frequently assumed to correspond to common analytical functions, for example, uniform, Gaussian, Poisson, Weibull. The simulated cost in this case also is a distribution that results from the interaction of the random input variables. A deterministic model replaces all the distribution of the input variables with the expected value and calculates the expected value of the output variables. This results in a computationally more efficient analytic model.

4.3 TECHNICAL COST MODELING

TCM, also known as process-based cost modeling, is an extension of engineering process modeling with particular emphasis on capturing the cost implications of process variables and economic parameters. It approaches cost estimation by considering the individual elements that contribute to total cost. These individual estimates are derived from basic engineering principles, from the physics of manufacturing process and from clearly defined and verifiable economic assumptions. Since the cost estimates are grounded in engineering knowledge, critical assumptions, such as processing rates and materials consumption, interact in a consistent and logical manner to provide an accurate framework for economic analysis. Technical cost modeling can be tailored to a wide range of operating conditions, thus enabling new processing options to be investigated without extensive expenditures of capital and time.

A technical cost model does not make any assumption about the overall size of the operations. It assumes the existence of a facility capable of producing a specified number of products. In that regard, the cost model is *a priori* model which allows cost estimation before the product is actually made; it does not attempt to model any existing facility, although it can be modified to do so when necessary.

One advantage of TCM over simpler cost estimation techniques is that it not only provides an estimate of the total cost and its breakdown, but it also supports sensitivity analyses, which allow the cost consequences of yield, process rates, multi-shift operations, equipment utilization, downtime and other process variables to be investigated. Technical cost models have been used to prioritize investment, optimize designs, evaluate alternative processes and direct efforts at cost reduction and yield improvements.

4.3.1 Principles of Technical Cost Modeling

A technical cost model can be developed on any spreadsheet program and its general layout is shown in Figure 4-1. The power and flexibility of using a computer spreadsheet facilitates rapid data storage, data manipulation and output

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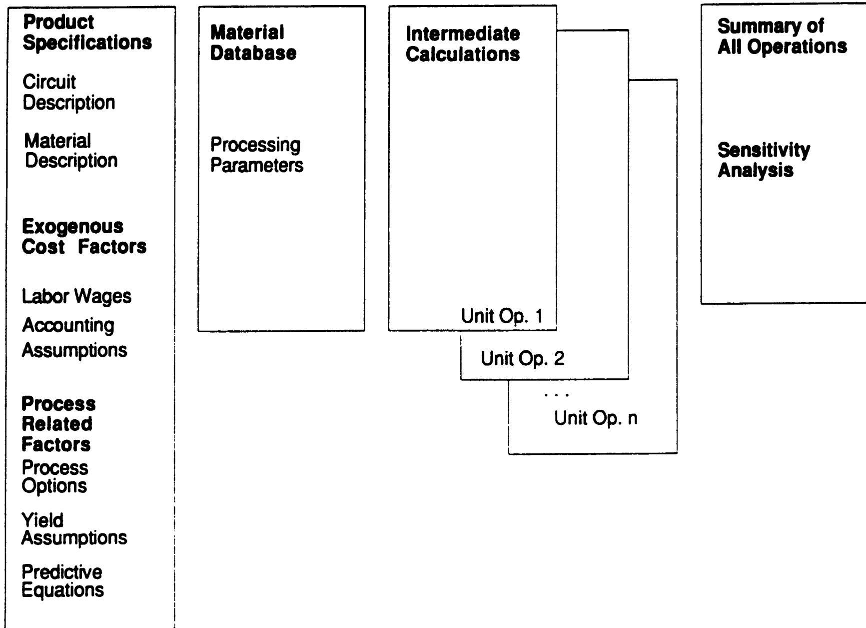

Figure 4-1 Layout of technical cost model.

recalculation. The models are composed of three distinct sections: inputs, intermediate calculations and cost summaries.

The input section of the TCM is divided into four segments: product specifications, exogenous cost factors, process-related factors and materials database. Product specifications vary depending upon the material and geometric configuration of the part being modeled. The exogenous cost factors reflect the economics of the work place and therefore vary with time and location. Process related factors are used to embody the mechanics of the process as it exists in industry. The final group of inputs, the materials database, contains currently available materials, their prices and properties and other material specific information.

The intermediate calculations sections display internal calculations for each unit operation in the process. The cost summary sections present a breakdown of cost into the variable and fixed cost elements. Variable cost elements include materials, utilities, direct labor and variable overhead, while fixed cost elements include capital equipment, tooling and fixed overhead. A detailed description of

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the estimation of fixed and variable cost and the methods for distributing them over the total number of components manufactured can be found in Busch [11].

The key principles of technical cost analysis are:

1. The total cost of a process is made up of many contributing elements that can be classified as either fixed or variable, depending upon whether or not they are affected by changes in the production volume.

2. Each cost element can be analyzed to establish the factors that affect its value. Depending on the process, the factors that affect cost may differ. For example, the firing time of a ceramic is dependent upon the material, while the screen printing time may not be affected by material.

3. Total cost can be estimated from the sum of the elements of cost for each contributing process. TCM essentially reduces the complex problem of cost analysis to a series of simpler estimating problems, and brings engineering expertise, rather than intuition, to bear on solving these problems.

Although a technical cost model embodies a number of simplifying engineering assumptions, the level of technical detail in the model far exceeds that of other more common cost estimation techniques. By improving the engineering analysis, one may improve the cost estimate further, but there are limits to the value of such modifications, as shown in Figure 4-2. Figure 4-2 shows that while a very accurate cost simulation model may produce minimum errors, its development and maintenance cost far outstrip its potential benefits.

While the ability to estimate production costs on the basis of a set of manufacturing and engineering assumptions is an attractive consequence of constructing a technical cost model, it is the framework for the calculation that provides the greatest benefit. By enforcing a discipline upon the cost estimating process, a consistent and easily justifiable cost estimate can be rapidly computed. Furthermore, the consequences of alternative processing and engineering assumptions can be evaluated on a consistent basis.

4.3.2 Applications of Technical Cost Modeling

Technical cost models can be applied to any manufacturing process. Because it is derived from manufacturing data, it is easy for engineers to understand and use. It has been successfully applied to the automotive [11]-[12], aerospace [13],

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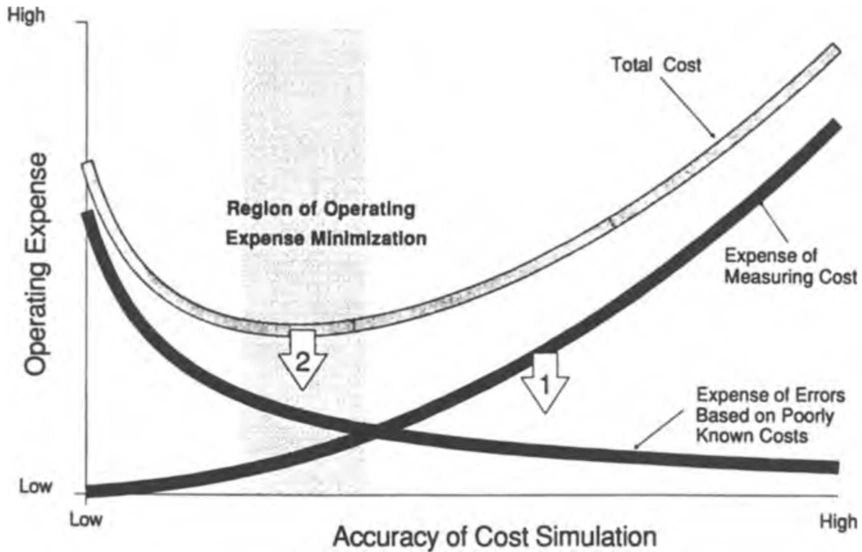

Figure 4-2 Optimization of cost simulation.

recycling [14] and electronics industries. TCM can be used to accomplish the following tasks:

- Estimate costs of products for guiding price quotation
- Establish direct comparisons between process alternatives
- Investigate effect of changes in manufacturing on overall cost
- Identify limiting process steps and parameters
- Determine the merits of specific process improvements
- Compare the merits of functionally equivalent designs
- Identify areas for future R&D

The next section presents some results on the estimation of cost for printed wiring boards, thick film and cofired substrates, thin film MCM and the cost of assembly and testing to illustrate the application of TCM to electronics packaging. *It must be emphasized that the results presented are intended to show the application of the models and the impact of materials and packaging technologies. The results encompass a large number of implied assumptions which are specific in the context they were analyzed and should not be taken as broad based cost projections.*

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4.4 RESULTS OF TECHNICAL COST MODELING

4.4.1 Printed Wiring Boards

One of the first areas of application of TCM to electronics packaging was in the area of printed wiring boards (PWBs) [15]. In this section, only high density multilayer boards are discussed; the cost of double sided boards is reported elsewhere [16].

One of the issues facing the engineer is the tradeoff between the cost and the density of the board [17]. In the design of a PWB, it is possible to decrease the layer count by increasing the per layer interconnect density of the board. Suppose a board requires a total interconnect density of 120 in/sq. in. Using 7 mil lines, 2 lines per 100 mil grid, six signal layers are required. Alternatively, using 5 mil lines, 3 lines per 100 mil grid, only four signal layers are required. Assuming that one ground and one signal is required, the two alternative board configurations require an eight and six layer boards respectively.

Faced with these options, the design engineer needs to know the economic impact of the two designs. This can be accomplished by using the PWB technical cost model to simulate the production of the two boards. Figure 4-3 shows the cost of a finished board for both options as a function of both panel and inner layer yield, assuming a board size of 8.5" × 9.5". The top curve shows the cost of the eight layer board at an inner layer yield of 90% and the two shaded curves refer to that of the six layer board at different inner layer yields.

Figure 4-3 shows that the cost of the 7 mil line, eight layer board at 90% inner layer and overall yield is comparable to that of the 5 mil line, six layer board at 80% inner layer and 85% overall yield. It is expected that both the inner layer and panel yield for the two boards would be different in actual production, but the technical cost model allows the designer to find the breakeven point for each board. Alternatively, if yield as a function of the process capability of individual steps is available and coded into the technical cost model, the model will estimate the overall yield and the expected cost of the board for the designer.

Another common dilemma is the specification of materials. While epoxy glass is the cheapest option, its low glass transition temperature (T_g) limits the repairability of the board during assembly. In the case of boards populated with expensive components, repairability is very important. Several materials with higher T_g are available, but they are all more expensive. To investigate the cost penalty of using different materials, the technical cost model is used to simulate the manufacturing cost of the same board using different laminates, taking into account the differences in processing parameters such as drilling, oxide treatment, lamination time, and others for different materials.

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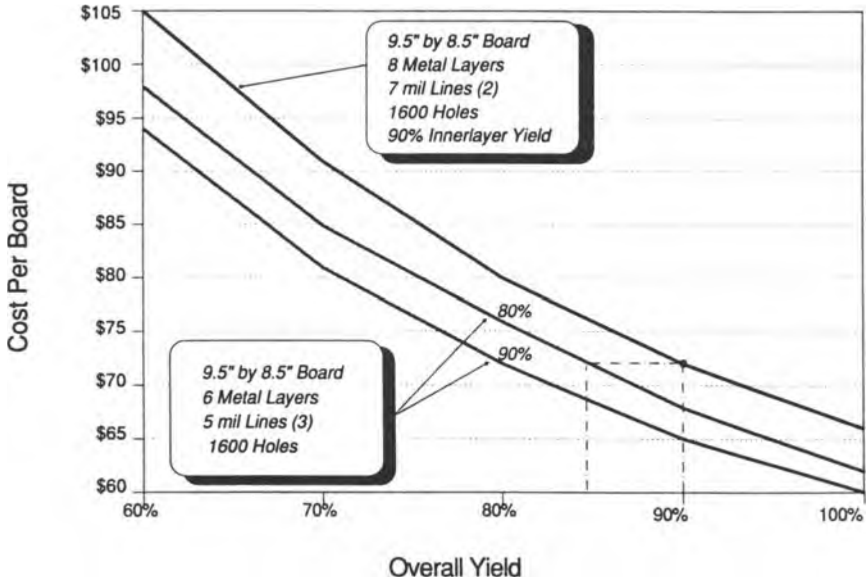

Figure 4-3 Cost tradeoffs between layer count and line width in PWBs.

Figure 4-4 shows the cost of the same eight layer board using different materials simulated using the technical cost model. At $2.50/sq. foot for the laminate, epoxy glass is the cheapest material. Using bis-maleimide triziane (BT) at $6.50/sq. foot, the same board would cost 25% more at the same yield. Finally, if polyimide (highest T_g) is used, the cost of the same board goes up by 60%, assuming an 80% overall yield due to the difficulty of processing polyimide. In all cases, although the raw material cost may be 2 to 4 times more than epoxy glass, the difference in the cost of the finished board is less than 100%. Thus, using raw material cost as the basis of material selection is very misleading.

In the analysis of the cost of the board using different materials, it was found that the cost penalty of going to a higher T_g material is not prohibitive. Therefore, in the case of expensive components mounted onto a circuit board, the use of a higher T_g material to ensure the success of rework may be well worth the additional board cost. Again, the PWB technical cost model allows these tradeoffs to be quantified. Of course, there are other performance variables, such

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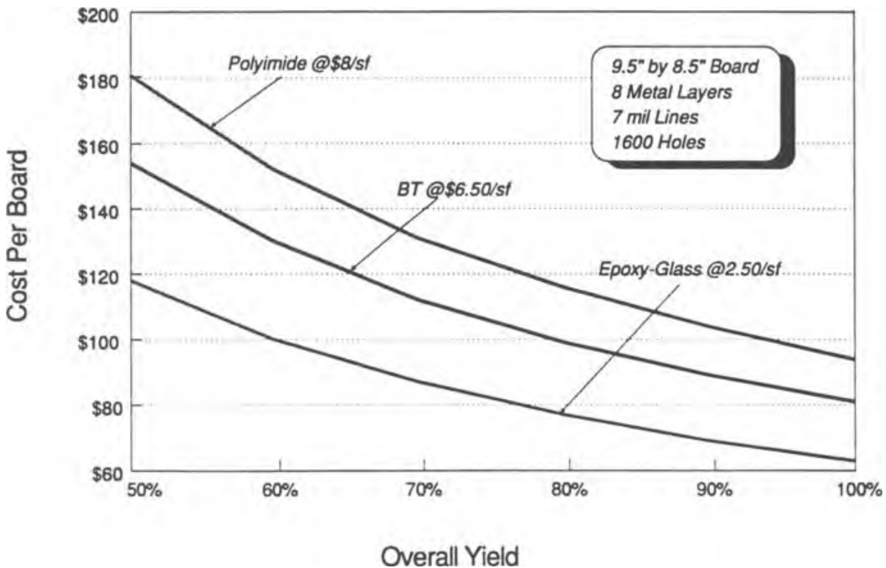

Figure 4-4 Effects of different materials on board cost.

as dielectric constant, CTE, dimensional stability, moisture adsorption, which must be considered in selecting an optimal board material.

Aside from density, another design option that has attracted much controversy is the use of buried vias. By providing an internal path to an adjacent signal plane, the use of buried vias can significantly improve the routability of a PWB design, thereby reducing the total number of signal layers required. There are, however, ramifications to buried via boards. Considerable additional plating and drilling time is required, since each signal layer must be drilled and plated, then printed and etched prior to lamination of the final board, which is again drilled and plated, printed and etched. Because these yields are cumulative, they can increase cost rapidly if not well controlled.

The PWB technical cost model has been used to assess the tradeoffs between through holes and buried vias [18]. In a case study using a board for a computer application (see Figure 4-5), the cost of a 22 layer PTH board is compared to an equivalent 18 layer board with 2,310 buried vias per laminate on three inner layers. Figure 4-5 shows that there is a broad range of yield for which the buried via construction might be cost competitive with the PTH board. Therefore, if the attainable yield of a buried via board in a specific facility falls

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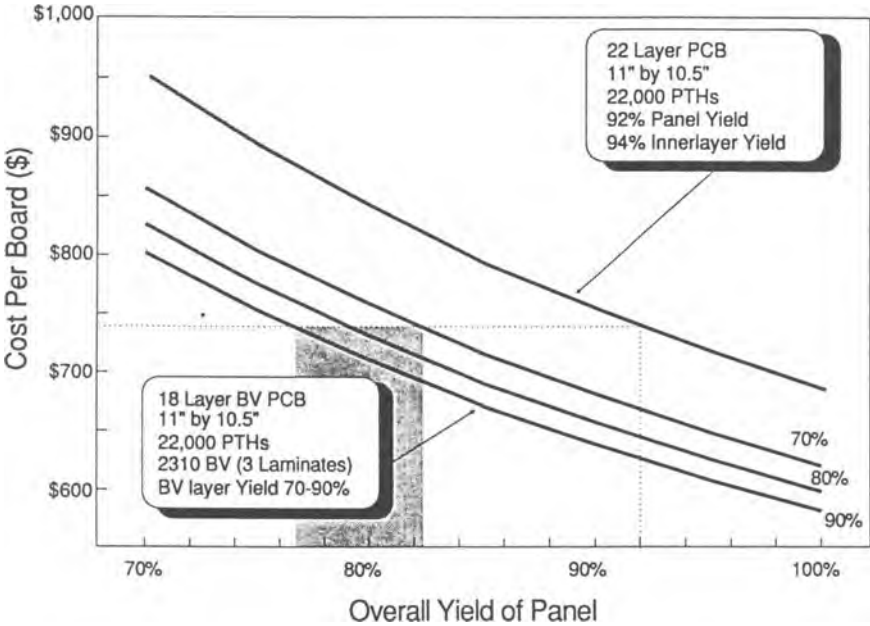

Figure 4-5 The cost impacts of buried vias in PWB.

within the shaded region, the designer can switch to the buried via construction without paying a cost penalty. Conversely, if the indicated yield is not achievable, the designer must decide if the improved performance is worth the additional cost.

4.4.2 Thick Film Substrates

Thick film technology was originally developed to interface and interconnect bare ICs on a hybrid circuit, which is essentially a multichip module. As chip density and complexity increase, the need for higher density and reliability in thick film boards has resulted in the development of better pastes and tighter process control. It now is possible to produce multilayer thick film substrates with 2 - 3 mil lines, although most thick film circuits produced today have line widths in the range of 6 - 10 mils.

Traditionally, thick film substrates are believed to be an expensive option particularly when compared to PWBs. However, studies have shown that they

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Table 4-5 Cost Breakdown of SEM "E" Thick Film Substrate.

	COST	PERCENT (%)
Materials	$59	32
Labor	66	36
Overhead	20	11
Capital Equipment	13	7
Utilities	13	7
Tooling	13	7
Total	$184	100%

can be a cost effective option in some applications. Because of the small size of the thick film market and the fact that it is heavily military, the cost of multilayer thick film varies widely. In this section, some general cost results are discussed.

A six metal layer circuit 4" × 5" with 10 mil copper circuitry (SEM "D" format) is selected for detailed cost analysis. There are approximately 2,000 vias of 12 mil diameter per layer. The circuit has been fabricated in the industry and prices are available on these circuits. Using a thick film TCM and assuming an overall yield of 90%, the cost of the SEM "D" circuit with copper conductors is simulated and the cost breakdown is shown in Table 4-5.

Table 4-5 shows an estimated cost of $184 for the circuit, which translates into $1.53 /sq. in. per layer. Product materials comprise a hefty 32% of total cost, and labor makes up 36%. Note that the tooling in the model refers to the screen mesh and other tools; it does not include artwork generation or test fixtures for the circuit. For comparison, quotations obtained from the industry indicated a price range of $600 for a SEM "D" circuit. While this price is three times that estimated by the model, it is not surprising because of the levels of engineering support required for a military specification board and, of course, profit, risk premium and corporate overhead, all of which are not included in the TCM. The model estimates the production cost for the circuit, not the price at which it can be bought in the market.

The materials used for the thick film circuit affect the processing parameters. While different materials suppliers recommend different processing parameters for their materials, the main difference in processing is the type of atmosphere used for firing. The firing atmosphere is dictated by the type of conductor used: gold and other noble metals can be fired in air, but copper requires nitrogen firing.

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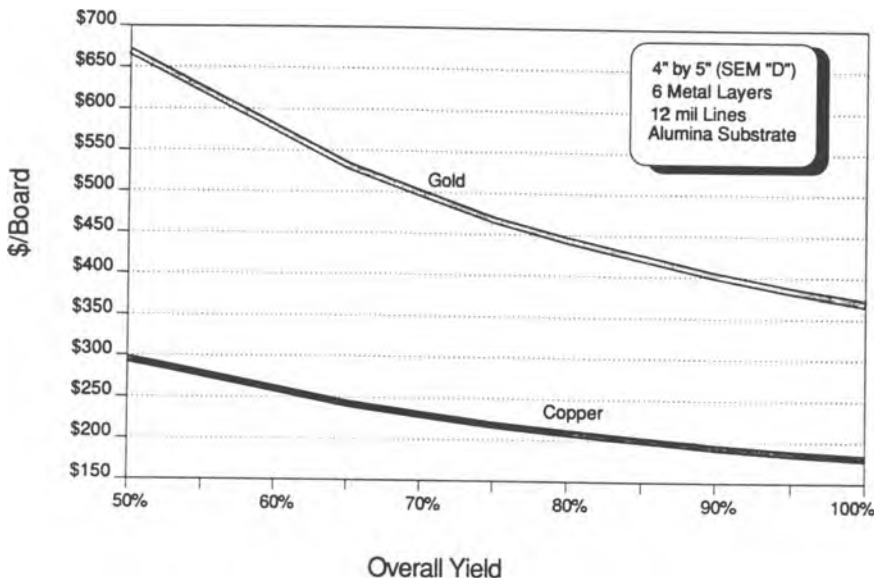

Figure 4-6 The cost impacts of conductors for thick film substrates.

Figure 4-6 shows the effects of conductor choice on the cost of the finished circuit as a function of yield. Since gold paste is 25 times more expensive than copper paste, raw material makes up about 68% of the total cost of the gold circuit, compared to only 26% for the copper circuit. At 90% yield, the gold board costs three times more to manufacture than the copper board.

4.4.3 Cofired Multilayer Substrates

Multilayer cofired ceramic technology has been used for microelectronics packaging since the 1950s. For MCM applications, two types of substrates have been evaluated: high temperature cofired ceramics (HTCC) and low temperature cofired ceramics (LTCC). In HTCC, the alumina green tape used has to be fired at above 1500°C, which allows only refractory metals such as tungsten and molybdenum to be used as conductors. This results in a circuit with high electrical resistance, which may not be suitable for high performance circuits. To overcome these shortcomings, newer materials that alleviate the requirement for refractory metals have been developed. These materials, called glass-ceramics, require a much lower firing temperature (800°C - 900°C), allowing

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Table 4-6 Cost Breakdown of HTCC and LTCC.

	COST	HTCC (%)	COST	LTCC (%)
Materials	$16	41	$57	82
Labor	5	14	5	8
Capital Equipment	13	31	5	7
Overhead	3	8	1	2
Others	2	6	1	1
Total	$39	100%	$69	100%

noble metals such as gold, silver/palladium, and even copper, to be used in the circuit.

The incorporation of a new technology, however, often comes at a price. Currently, the cost of green tape for LTCCs is very high. Additionally, the yield of the finished circuit is highly uncertain at this time due to the small volumes in production today. Given the differences in processing parameters and the uncertainties in yield and material prices, it is difficult to assess the economic competitiveness of LTCC, but such an assessment has important implications for users and manufacturers of cofired substrates [19].

To analyze the economics of LTCC versus HTCC, a hypothetical substrate 2.5" × 2.5" with an eight metal layers for a MCM is used. It is assumed that the substrate has 8 mil lines and spacing, and there are an average of 800 8 mil vias per layer. It is assumed that both the finished HTCC and LTCC circuits have the same set of circuit attributes as listed in Table 4-6, and four circuits are produced on one 8" ceramic card (4-up). It is further assumed that the HTCC system uses alumina green tape with tungsten conductors and the LTCC system uses glass-ceramic tapes with silver/palladium conductors.

Using the circuit as the basis for cost simulation and making optimistic assumptions about production volume (10,000 per year) and conductor yield (95%), the cost of the HTCC circuit is estimated to be $39 ($0.80/sq. in. per layer). The cost breakdown (Table 4-6) shows three major elements: materials (42%), capital equipment (31%) and, to a lesser extent, labor (14%). Using the same circuit attributes, the cost analysis for LTCC circuits yielded a total cost of $69 ($1.40/sq. in. per layer). The overwhelming cost is in the product material (82%). From this cost breakdown, it is apparent that the material cost should be the first focus of any cost reduction efforts.

From Table 4-6, it is apparent that HTCC substrates are cheaper to produce at this time. However, it must be emphasized that the assumptions used for the

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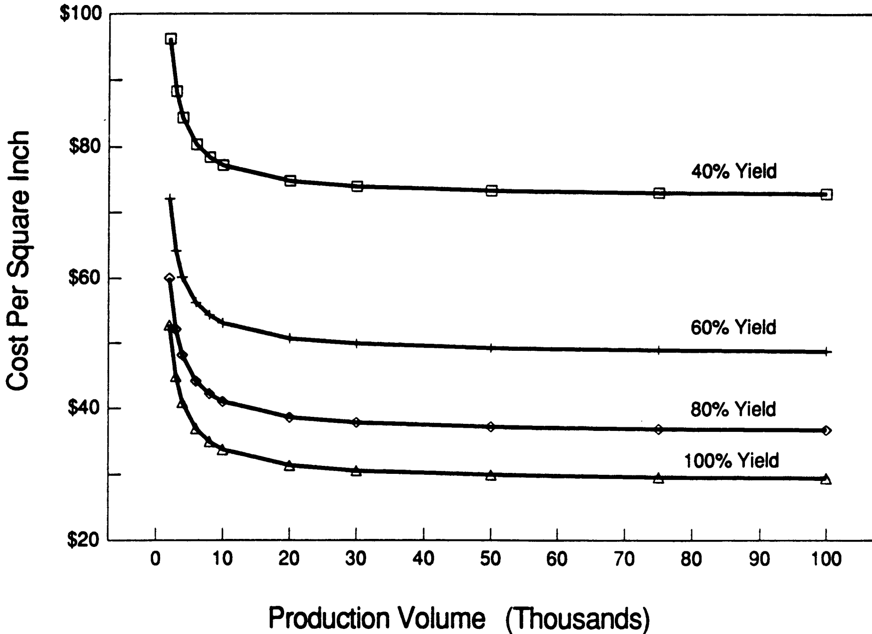

Figure 4-7 The impact of cost on the volume and yield for thin film MCMs.

analysis of LTCC represents industry averages for today. These assumptions, including material prices, yield and even the types of conductors used, are expected to change as the technology matures.

4.4.4 Thin Film MCMs

In the past few years, thin film MCM technology (MCM-D) has become the focal point of the electronics packaging industry. Currently, the cost of thin film MCM substrates is quite high, ranging from $40 to $70/sq. in., but has been predicted to fall to around $14/sq. in. in 1993 [20].

The biggest cost drivers for thin film MCMs are volume and yield [21]. Figure 4-7 shows the volume-yield relationship as generated using information collected from the manufacturers, material suppliers and equipment manufacturers. Figure 4-7 shows that the cost of fabricating thin film MCMs will level off at $30/sq. in. at high volume and reasonable yield for most manufacturers using current materials and processing technologies. However, that does not mean that the prices will not fall below $30/sq.in. in the future.

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With improved materials and processing technologies, the cost should come down even further.

To better understand the potential for cost reduction, consider the cost breakdown of a high volume, high yield substrate [22]. Using a five metal layer substrate as the basis, the cost breakdown shows that capital equipment is the largest cost element, making up 45% of the cost of the circuit. This analysis assumes that all of the equipment is new and uses the capital recovery formula (similar to loan payment calculations) as the basis for distributing capital cost. Materials use makes up 21% and labor makes up 17% of total cost. In terms of processes, metallization makes up 46% of the total cost, while polyimide deposition and via formation takes up another 30%. From this cost breakdown, it is apparent that improving the metallization technology should be the first focus in any cost reduction efforts, with polyimide deposition and via generation coming a close second.

It has been reported that using photosensitive (PS) polyimide to generate vias can reduce the number of processing steps. However, the cost of PS polyimide is high and the yield may be low. Thus, the question as to whether the use of PS polyimide is economical depends on the tradeoff between material cost, processing parameters and yield, assuming that the performance of both dielectrics is acceptable. Figure 4-8 shows the cost of a finished circuit as a function of the cost of a polyimide, assuming an overall yield of 80% and high volume production [23]. The darkened lines show the current price range for photosensitive and non-photosensitive polyimides. Given the current price range, the use of PS polyimides does not result in any cost savings at the same yield. If, however, the prices of PS polyimides were to fall below $1.20/g, it could become cost competitive.

4.4.5 Cost of MCM Assembly

In the design and fabrication of the MCM, the chip-to-substrate connection technology is an important consideration. Unfortunately, there is no universal connection technology suitable for all applications. The connection choice depends upon a myriad of factors, ranging from the requirements of the application to the internal manufacturing and design capabilities. Currently, many of the high density MCMs produced are prototype modules, and wire bonding is favored in these applications. However, as these companies move from prototype to production, the choice of connection technology and its impact on the cost of the finished module will become critical to both the users and manufacturers of these MCMs.

In surveying the industry, little consensus was found in several critical parameters in chip assembly: chip yield, bond yield, repair and testing cycle time

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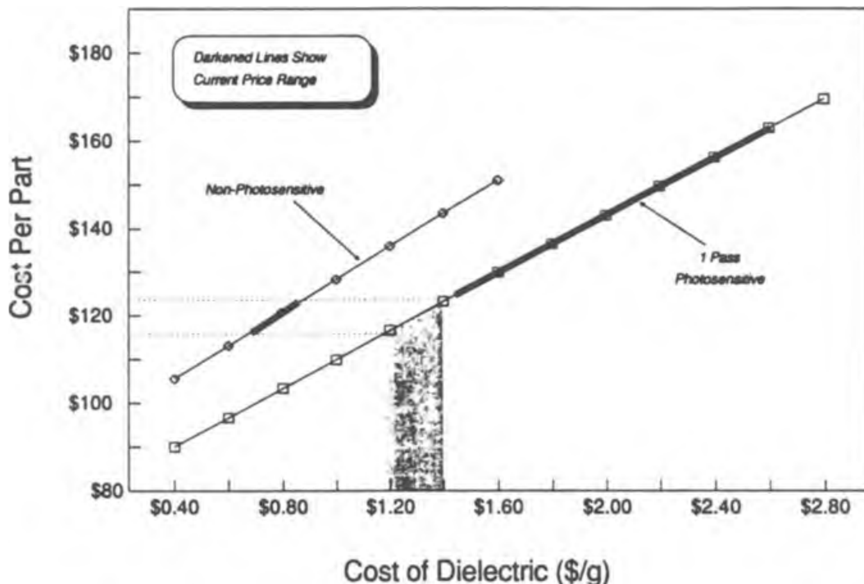

Figure 4-8 Substrate cost versus cost of polyimide (photosensitive and nonphotosensitive polyimides) for thin film MCMs.

and yield, and nonrecurring engineering (NRE) cost. This is an indication of the immaturity of the industry at large. Therefore, this section shows specific results and a sensitivity analysis for a given set of assumptions; the results are not intended to be representative of the industry.

The cost of assembly for any module, as presented in this analysis, is the sum of the cost of all the chips, the cost of bumping the chips and mounting them onto a TAB frame, if necessary, the cost of all the necessary materials (enclosures, adhesives, wires, TAB tapes, scrap), the cost of the assembly process (wire bonding, TAB and flip chip), the cost of electrical testing (functional structural test), the cost of repair and rework, and the cost of final inspection.

In this analysis, two cases of chip technologies are assumed: state-of-the-art and mature chip. When mature chips are used, the test escape rate (a defective chip not detected by testing) is low because the design and process are proven. When using state-of-the-art chips, however, the test escape rate can be very high. In this case, the use of TAB to pre-test and burn-in the chips can reduce the test escape rate and lower the cost of rework. The assumptions used for this analysis are discussed elsewhere [24].

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Using a chip assembly technical cost model and the assumptions listed in Table 4-7 with mature chip technology, the cost breakdown for an MCM using wire bonding and TAB is tabulated in Table 4-8. As expected, the cost of the chip (at 85% of total cost) dominates the cost of the finished module. There is only a small percentage of difference in the connection costs between TAB and wire bonding when mature chip technology is used. Therefore, the connection choice in this case should not be driven by cost alone, but rather, the capability of the manufacturers and future requirements.

However, if state-of-the-art chips with a higher test escape rate are used, the use of TAB mounting reduces system cost substantially. Assuming that chip costs remain constant and the percent of known good die is improved from 60 - 95% for the ASICs and from 85 - 98% for memory devices, the cost of the same module is $223 lower when using TAB. The cost savings results from the need for less rework or repair and fewer scrapped chips.

The assembly cost module can be also used to investigate the effects of yield per bond on overall cost. The results of the cost breakdown for the different connection schemes as a function of yield per bond is shown in Figure 4-9. At 99.95% yield per bond for TAB, the cost of the system is estimated at $2,700. At the same yield, wire bonding is expensive. However, if the yield of wire bonding is 99.98%, the cost of TAB and wire bonding become comparable.

4.5 APPLICATIONS TO SUBSTRATE SELECTION

Thus far, this chapter has presented an extensive analysis on the cost of different substrates under a specific set of assumptions. For example, it is estimated that the cost of a thin film MCM will level off at $30 sq. in., for a given manufacturing line, while the current cost of a 22 layer PWB is $7/sq. in. While this information is useful, it does not provide a common metric for substrate technology selection; a design implemented on thin film MCM is likely to be smaller than the same system on PWB.

To compare different substrate technologies, it is necessary to reduce all the different packaging technologies to a common metric. Some common metrics suggested in the industry includes cost per interconnection density [25] and cost per substrate pad [20]. An example of the price/density plot is given in Figure 3-6 where the vertical axis is the cost/sq. in. and the horizontal axis is the available density in in./sq. in. The plot has been used in a number of tradeoff studies of packaging methods.

While these price/density metrics are very useful for general macroscopic comparison, they may not be a good selection tool at the microscopic level when actual design constraints are considered. TCM can be applied to substrate

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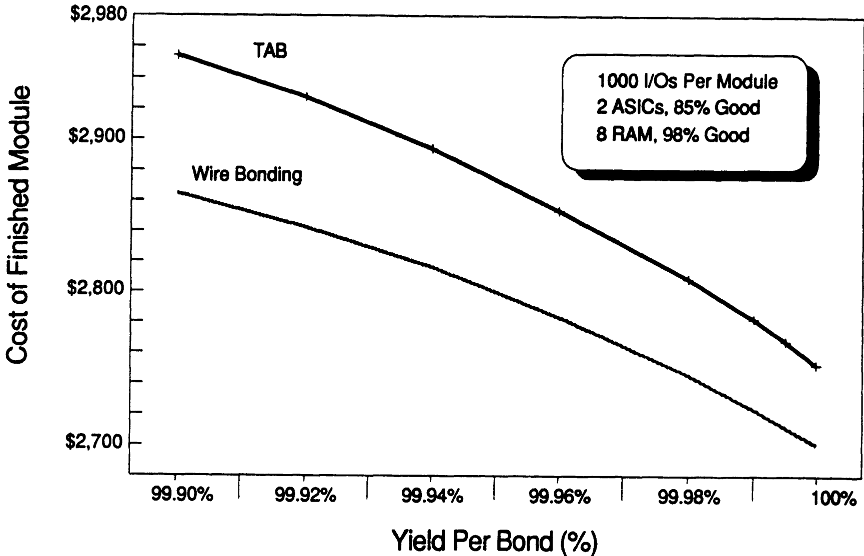

Figure 4-9 The impact of cost on the bond yield of MCMs for TAB and wire bonding.

technology selection when actual design constraints are available. Before the cost models can be used, however, it is necessary to have a procedure to translate a design from one scheme (such as DIPs on PWB) into another (bare chips on ceramic substrate), given a set of constraints and assumptions for each packaging scheme.

A simple way to do the translation is to first set the area so that it can accommodate the required chips, with a suitable space provided for the leads. The number of layers is then calculated so that the routing density is the same in each option [26]. These results then can be fed into the different substrate technical cost models for substrate cost estimation.

As an example, consider a system consisting of two 4.9" x 4.6" piggy-backed PWBs using through-hole packages on one side, and surface mounted discrete components on the other side. The two boards each use 10 mil lines and have 10 and 8 layers respectively. Table 4-9 estimates and tabulates the requirements of the same system using different packaging schemes and needing the same area for the die, the discrete components and the unpopulated area.

Table 4-9 shows that it is possible to reduce the two boards into one board of the same size by using surface mounted devices (SMDs) on both sides. For

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Table 4-9 Attributes of Different Substrates for Cost Comparison.

	PWB	THICK FILM	THIN FILM
Length (in.)	4.9	4.9	3.3
Width (in.)	4.6	4.6	3.3
Line Width (mils)	7	8	1
Via Pitch (mils)	100	16	4
Pad Layers	2	1	1
Total Layers	10	5	4

this example, it is assumed that the original board size is preserved for compatibility reasons when using thick film substrate and PWBs. In the case of a thin film MCM, it is assumed that bare chips are used instead of SMDs. The minimum required size is 3.3" square, and only four metal layers are required because of the high connectivity of thin film MCMs.

Using the attributes listed in Table 4-9, the costs of the different substrates estimated by the technical cost models are plotted in Figure 4-10. Note that because yield varies greatly from one facility to another, it is used as a variable in the figure with the darkened sections indicating the expected yield ranges. In Figure 4-10, there are two curves for the PWB, one using polyimide (PI) and the other using epoxy glass (FR-4). The curve for the thick film substrate is for copper conductors.

Figure 4-10 shows that the lowest cost option is achieved by using conventional PWB technology. However, if CTE mismatch is a problem, then epoxy-Kevlar or copper-Invar-copper boards may have to be used. In that case, ceramic boards, at 2 to 3 times the cost of conventional boards, may be attractive. Although the bare chip on thin film option offers greater potential for improved performance, it is considerably more expensive given the yield and volume levels existing today. However, the thin film substrate can be cheaper than thick film with gold, if its yield is better than 65%. Conversely, thick film with gold is cheaper if its yield is better than 76%. As can be seen in this example, the competitive position of each substrate technology is very dependent on the design constraints and manufacturing, especially yield.

Once the cost of substrates has been estimated, the cost of assembly and backplanes also can be estimated to provide the cost at the system level. This approach not only provides a good framework for cost comparison of different packaging options at the design phase, but it also allows the designer to understand what drives the cost in each of the packaging options, leading to improved and more economical design.

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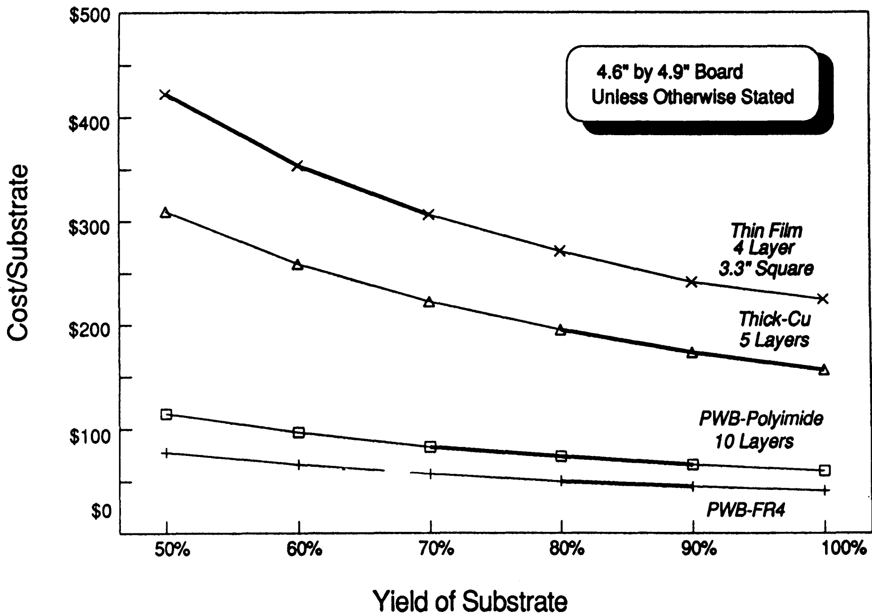

Figure 4-10 Example of cost of different substrates.

4.6 DESIGN ACTIVITY-BASED COST MODELING[1]

In Section 4.2.3 technical cost modeling was defined as a cost model based on a simulation of manufacturing operations. Doing this requires detailed knowledge of those operations. Many applications design companies do not manufacture the components themselves and, thus, do not have sufficiently detailed knowledge. The manufacturing costs are determined by the prices set by the vendors who manufacture their parts for them. Their total cost also includes the cost of supporting design, prototyping, vendor interfacing and customer support. Such companies need a design-based, not a manufacturing-based cost model.

It is worth noting that an applications company might have valid use for a manufacturing activity-based TCM. If such a model includes a set of good assumptions about cost, then it can be used to form a first estimate of the cost

[1] Contributed by Paul D. Franzon

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Table 4-10 Cost Elements that Comprise a Design Activity-Based Cost Model.

Recurring Manufacturing Costs	
R1	Substrate Cost = Panel Cost/Number of substrates per panel
R2	Cost per part of other components: heatsink, connectors, frame, box, etc.
R3	Chip cost (might be untested, partially tested or fully qualified)
R4	Cost of TAB frame
R5	Cost of assembly for each subsystem
R6	Cost of testing each subsystem
R7	Percentage of test escapes and assembly-related failures
R8	Average cost, per part, of rework
R9	Final subassembly yield
R10	Cost of components of higher levels of packaging (hermetic seals, MCM-PWB connectors, PWBs, backplanes, cabinets, etc.)
R11	Cost of assembly for system
R12	Cost of test for system
R13	Percentage of assembly-related failures
R14	Average cost, per system or rework
R15	Final system assembly yield
Nonrecurring Design and Prototyping Costs	
N1	Designer time for analysis and design
N2	Management and support staff time including time spent on vendor interfacing
N3	Cost of computers, CAE/CAD tools, other design equipment as apportioned to project
N4	Cost of offices, electricity, etc.
N5	Designer time for generating test plan
N6	Time to debug prototype and improve design for manufacturing
Recurring Post-Production Costs	
P1	Customer support services and repair
P2	Impact on customer satisfaction

for different alternatives without having to obtain detailed vendor quotes. It also might be useful when vendor cost information is uncertain. For example, current vendor pricing of thin film MCMs do not anticipate the future improvements discussed in Section 4.4 above, Also, current vendor pricing of bare chips is uncertain. Knowing the basis for these costs would allow a designer to anticipate future prices and also would provide bargaining power.

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The inputs that are needed to construct a design activity-based cost model are given in Table 4-10. There are three types of inputs in this model: recurrent manufacturing costs, nonrecurrent design and prototyping costs, and recurrent post-production costs. Recurrent costs are incurred for each unit manufactured. Nonrecurrent costs are incurred only once for each design or sometimes for a set of designs.

Most of the recurring manufacturing costs (R1-R15) are obtained from vendor quotes and require the provision of preliminary design information (such as layer count, feature size, production volume). The most straightforward way to investigate alternatives is to obtain quotes from vendors for these alternatives. One approach to generating this preliminary design information for different substrate technology alternatives was given in Section 4.5. Often, technology decisions (such as selecting from substrate alternatives) can be made on the basis of rough cost estimates which are themselves based on rough design data.

Typical current high-volume quoted prices for different substrates are given in Table 4-11. Such quoted prices usually include the expected effect of yield. A proviso is needed, however, when working with this type of data. Despite the mainly per unit inch prices shown in Table 4-11, vendors actually work in terms of the cost per complete panels (or complete substrate), not the cost per part. For example, PWBs typically are made in 24" × 18" panels, usually of which 22" × 16" is usable usually. MCM-Ls are made in smaller panels. Cofired MCM-Cs are made in 9" squares (which shrink by 15 - 20% during firing). MCM-Ds usually are made in 5" or 6" diameter wafers or "rounds." It is up to the designer, in conjunction with the vendor, to maximize the number of individual components manufactured on each panel or wafer. If N components are made, the number of parts per panel often is referred to as "N-up." The prices given in Table 4-11 were generally rough panel per unit area prices. They do not include the effect of wastage if all of each panel cannot be used.

There are other components besides the substrates, including the chips, connectors, heatsinks, power supply, frames, boxes. It is straightforward (though sometimes time consuming) to obtain vendor quotes for all the physical component alternatives being considered.

Some of the recurring costs, such as test cost and rework need might be difficult for the vendor to estimate when presented with only preliminary design data. it might be necessary for the designer to estimate these cost factors and work with the vendor to estimate their impact. This can be done by using Equation 3-16 in Chapter 3, repeated here:

$$\text{Final Cost} = \frac{MC + TC + (P(TE) + P(AF)) \times (RC + ATC)}{\text{Final Yield}}, \tag{4-1}$$

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Table 4-11 Some Typical Vendor Substrate Prices.

TECHNOLOGY	TYPICAL COST ($ PER SQUARE INCH)	TYPICAL PANEL SIZE
PWB 5-6 mil lines 2 layers Each additional layer pair	 $0.1 $0.2	 24" x 18"
MCM-L per layer 3 mil lines 12 mil PTHs	$1.50	12" x 18"
MCM-C (cofired) 4 mil layers 6 layers 10 layers 30 layers	 $15 - $20 $25 - $30 $50 - $75	 9" x 9" 9" x 9" 9" x 9"
MCM-D 5 layer	 $400-$500 per round	 6" diameter rounds

where MC is the total IC and MCM manufacturing cost, TC is the total IC and MCM test cost, P(TE) is the test escape probability, P(AF) is the probability of an assembly fault, RC is the rework cost and ATC is the cost of retesting the assembled substrate.

The cost model in Table 4-10 assumes a two step process: MCM assembly and test, followed by system assembly and test. Thus, in Equation 4-1, the manufacturing cost MC for the MCM assembly is the sum of R1 to R5, and the manufacturing cost for the system is the sum of R10 and R11. Many manufacturing processes would be expected to have more than two steps.

The design costs (N1 to N6) are nonrecurring costs. Designer time has to be estimated upfront in the design cycle. This is a difficult task, particularly given the propensity of some managers to underestimate how long it takes someone else to do something. An example of the impact of the design time (and incidently manufacturing cost) for different cooling approaches is given in Table 4-12.

Also contained in the model are two post-production cost elements: customer service costs and the cost impact of customer satisfaction. These were discussed in Chapter 3 in terms of maintenance, reliability and repair. To estimate these costs, reliability models and maintenance effort models are necessary. With the use of these models, it is possible to judge the life cycle cost impact of maintenance, repair and replacement.

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Table 4-12 Impact of Different Cooling Techniques on Design Time and Production Cost per Part for a Signal Processing MCM. (Courtesy E-Systems, Melpar Division.)

TECHNOLOGY	ANALYSIS	DESIGN	PROCURE	MATERIAL
Natural convection with no finned heatsink	80 hours	0 hours	0 hours	$0
Natural convection with finned heatsink	120 hours	40 hours	40 hours	$25
Forced air convection with no finned heatsink	80 hours	20 hours	10 hours	$100
Forced air convection with finned heatsink	120 hours	70 hours	40 hours	$200
Liquid cooled	160 hours	100 hours	40 hours	$500

Often the designer has to weigh one cost factor against another and make a decision as to the route that will minimize total cost. For example, it is necessary to balance the cost of fully testing the chips against the cost of extra MCM rework because of chip failures (test escapes), or, alternatively, the cost of procuring TAB frames and testing the chips. This was discussed earlier in this chapter and in Chapter 3.

Another example is to consider the cost impact of putting extra features in the design so that faults on the assembled substrate can be located easily and then diagnosed. Though these features might increase size and manufacturing cost (MC) they might also reduce test cost, rework cost and reduce the time required to debug the prototype. This would involve considering boundary scan techniques (see Chapter 13) if the design team also is designing the chips. On the other hand, if the chip design is fixed, testability could be enhanced by bringing certain internal signals within the MCM to the edge connector just for test purposes. For one module, produced by E-Systems, this was done by adding multiplexer chips to the MCM for test signal injection and monitoring. Despite a resulting increase in substrate size of 20% and an increase in I/O of 10%, they considered this extra cost to be well worthwhile because of the resultant savings in prototyping time.

The designer also should consider tradeoffs that make the module easier to assemble with standard equipment. The vendor should be able to indicate what

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cost savings can be passed on to the designer by doing this. The vendor should also indicate what design features will maximize yield (and hopefully pass these savings on to the designer).

4.7 SUMMARY

As this is a book mainly about MCM components, this chapter has focused on MCM cost at the component level. Two types of model were presented. Both of the models required a fair level of detail in their inputs. For example, they require a good idea of the substrate size, number of layers etc. In the early phases of design for a large system (large being larger than a single board), this level of detail often is not available. Thus, the inputs to a cost model at the system level will look different than the inputs to the models above.

A system level model is important because it is easy for the system designer to be sidetracked by the fact that an MCM will be more expensive than a similar PWB populated by the same chips in packaged form. As an MCM-based system allows multiple racks of boards to be reduced in size to one rack, the system wide cost savings on the higher levels of packaging can be substantial. This is discussed further in Chapter 18.

Two approaches are commonly used to make decisions early in the system design phase. The first approach is to use a system level cost model, similar in concept to the models presented above, that can use summary and estimates, rather than detailed, information as its inputs. Typical inputs to such a model would include summary information for each MCM such as number of chips per substrate, substrate types, number of MCM signal I/Os and power density. The system level cost model would then estimate substrate cost, heat dissipation cost, test overhead cost etc. to arrive at a system cost estimate. By estimating these inputs for different system implementations, cost estimates can be generated.

The second approach is to compare different system implementations through the use of a set of system metrics that can be easily translated from one implementation to another. For example, if the required interconnection density for a single chip packaged version is determined first then the size and cost of a thin film version can be estimates by considering its interconnection density. Consider the case where the required PWB interconnection density was 51 cm/cm^2 and the interconnect density of an MCM alternative is 100 cm/cm^2. Then the substrate size is expected to be one-half the latter and the system is costed appropriately.

In this chapter, however, two component level cost models were presented. One model, called technical cost modeling (TCM), was manufacturing-based to make manufacturing-related decisions when the designer knows the manufacturing details (usually only the case when the manufacturing activities

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are in-house). The other cost model was a design activity-based model for use when the only manufacturing-related information available to the designer are the vendor's quoted prices.

Through the application of technical cost modeling to different substrate technologies, it was found that the cost of thin film technology will likely remain high unless the volume hurdle can be overcome. It also was found that though the use of photoimagable polyimide can save on the cost associated with extra via processing steps, it will remain more expensive overall until the cost of this polyimide comes down. Thus, the TCM can be used to judge tradeoffs for minimizing manufacturing costs.

The design activity-based cost model can be used to compare vendor alternatives and also to judge tradeoffs to minimize total cost. For example, a comparisons of the cost involved in adding chips to improve testability versus the cost and time saved in testing and debugging the MCM as a result of this shows that doing this is worthwhile.

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Part B—The Basics

The White Rabbit put on his spectacles,
"Where shall I begin,
please your majesty?" he asked.
"Begin at the beginning," the King said,
"and go on till you come to the end:
then stop."

Alice in Wonderland
by Lewis Carroll

Part A - The Framework was like preparing the reader for a race. We defined the course and alerted the reader to most of the important decisions. Now we are at the starting line!

The nine chapters in **Part B - The Basics** provide an understanding of the technical fundamentals in the design and fabrication of multichip modules. Two broad topical areas are covered. Chapters 5 to 10 describe the physical components of multichip modules and their fabrication. These include first and second level connections, for which Chapters 9 and 10, respectively, present the available alternatives. Chapters 11, 12 and 13 cover the design sciences (electrical, thermal and test, respectively) that must be understood in order to make a successful MCM product.

Chapters 5, 6 and 7, respectively, describe in detail the three basic MCM fabrication technologies: MCM-L (based on laminate structures), MCM-C (based on ceramic materials) and MCM-D (constructed with deposited films). Typical fabrication sequences are described, along with the available major technical alternatives and the strengths and weaknesses of the possible choices. These chapters seek to answer such questions as: "*What portions of the technology are the strongest and most mature (useful for reliable design)?*" and "*What are the limitations in current fabrication sequences, and how may they be overcome?*"

Chapters 11 to 13 concentrate on what makes an MCM different from a design science point of view. Chapter 13 also concentrates on important manufacturing aspects associated with testing.

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The chapters in this Part can be read either to extend knowledge gained in another area into the area of MCMs, or to learn about an entirely new subject. For example, the reader who is already familiar with electrical design of printed wiring boards can extend his knowledge into the area of MCMs by reading Chapter 11. He can also gain from Chapter 5 an understanding of printed wiring board fabrication technologies and how they are used in MCM-L structures. Alternatively, the reader who is not familiar with these topics will gain a complete understanding from Chapters 11 and 5. All chapters are intended to be accessable to nonspecialists.

Thus, the aim of these chapters is to be tutorial in nature, as well as to provide specific information that will assist the reader in the transition to MCM technology. For example, the chapter on dielectrics (Chapter 8) provides a concise but complete picture of the important new area of dielectric materials for thin film MCMs (MCM-Ds). These chapters are not intended, however, to provide an exhaustive treatise on all aspects of their topics. Guidance is given to other sources as required.

Specific guidelines are given where appropriate. For example, the test chapter (Chapter 13) ends with specific guidelines on how to reduce test cost and effort. The practicing test engineer, for example, will be able to use these guidelines for help in designing MCM products. However, other engineers should not be deterred from reading this chapter, since it provides an excellent understandable tutorial on this important topic.

For the first time, this Part permits the reader to gain a clear understanding of the following:

- The factors that differentiate the MCM technologies and, thus, how to choose between them.
- The important issues related to dielectric selection.
- The relative merits of different chip connection and MCM connection alternatives.
- The importance of testing, and guidelines for controlling its cost.
- The basic issues and available alternatives in electrical and thermal design.

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For the first time, this Part gives

- A complete presentation of the important MCM-L technologies and alternatives.
- A complete and consistent presentation of first level (die to MCM) and second level (MCM to PWB) connection alternatives.

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5

LAMINATE-BASED TECHNOLOGIES FOR MULTICHIP MODULES

Leo M. Higgins III

5.1 INTRODUCTION

Subsystems based upon ICs wire bonded directly to printed wiring boards, have been important constituents of electronic products since the early 1970s. The density of these early systems was quite low and frequently did not connect many unpackaged die. Systems built with this process were said to be based upon chip-on-board (COB) technology. The term multichip module (MCM) has been widely used since the mid-1970s, but was not applied to modules based upon PWBs until the end of the 1980s. In the most common phraseology, the term MCM-L has come to imply an IC assembly comprised of multiple wire bonded die on a PWB. Other types of connection technologies, TAB and flip chip also are practiced in MCM-L systems, but COB assemblies have been the most common. COB involves the use of wire bonding and epoxy glob-top encapsulation, which are usually the lowest cost connection and sealing methods. These systems have typically been tested and burned in at the module level, and defective units are disposable. Higher cost, higher performance die often must be tested and burned-in prior to assembly, and the system cost forces planning for MCM repair. These higher performance die often have higher I/O counts, driving a higher module interconnect density than with the lower cost, disposable modules. Thus, COB modules have developed into a subset of MCM-L, where

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the modules are disposable and built with untested die. The range of MCM-L technologies has widened considerably in the areas of the materials and methods of substrate fabrication, and in the types of die connection to the board. In all instances, the minimum set of MCM-L attributes is the connection of unpackaged die on a substrate, whose manufacture is based upon laminate process technology [1].

5.1.1 MCM-L Amid the Spectrum of MCM Substrate Technologies

While the definitions of MCM substrates are discussed in Chapter 1, a cursory review of MCM substrate technologies is useful in view of the broad range of technologies available with laminate structures.

PWBs are known as organic boards since the primary constituent of the board dielectric is an organic polymer. The dielectric layers are supported most often by a reinforcing fabric, usually based upon woven glass fibers. Usually, there is no substrate underlying, or supporting, the laminate structure, as there is with MCM-D substrates where the typical dielectric (organic or inorganic) is very thin and would be structurally inadequate if not formed upon more rigid substrates such as Si, ceramic, metal or an organic laminate (PWB/MCM-L).

All MCM substrate technologies offer a wide range of material and structural options. Conductor options also are available with MCM-D (Cu, Al), and with MCM-C (W, Mo, Cu, Ag, AgPd). MCM-L conductors primarily feature Cu, but in certain structures Al and polymer thick films are used. MCM-D has numerous organic dielectric possibilities, and while silicon dioxide is the prevalent inorganic dielectric, other possibilities such as silicon nitride and spin on glasses are possible. MCM-C similarly offers a wide range of ceramic dielectric materials. MCM-L allows the use of many polymer dielectrics and reinforcing structures and materials (woven fabric, random matt, porous thermoplastics, particulates such as glass, graphite, fused silica).

Laminate boards can attain a high degree of rigidity after lamination due to the presence of the high modulus of elasticity fibers in the reinforcement phase, while particulate fillers are not as effective in imparting stiffness to laminates since they are not a continuous phase in the xy-plane. When dielectric layers use no fiber reinforcement, the resulting laminate can be quite flexible, leading to the term flexible ("flex") circuits. Combining both types of laminates in a single laminate product leads to structures called "rigid-flex." Thin film-type processing on MCM-L surfaces has been reported by several companies. Such processing includes fully additive and subtractive processing of conductors as well as the processing of dielectrics from liquid precursors or from supported or unsupported films. This creates a hybrid structure which takes advantage of the low cost of MCM-L and the enormous interconnect density provided by thin film

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technologies. Development work, and low volume manufacture of laminate structures formed on a more rigid base (metal and ceramic), is underway. This type of structure may be necessary in order to use the very thin dielectric layer film materials (≤ 50 μm) which have been developed recently.

5.1.2 MCM-L Attributes

MCM-L has a broad range of desirable attributes, with the primary set including low cost for one and two conductor layer structures for interconnecting a few die, forming a *few chips module* (FCM) and multilayer PWBs with a high interconnect density for the interconnection of many die. The FCM is a type of MCM-L where the interconnect density requirements usually do not push the envelope of process technology. Rather, this type of MCM-L provides a very low cost means to increase interconnect density for a small set (~≤ 4) of die. An FCM may be described as an MCM on which the number of chip to chip interconnections is less than the total number of MCM I/Os. This type of MCM-L may make novel use of vias, solder masks, encapsulation and finishing metals to achieve the primary objective of low cost.

Higher density MCM-Ls require an engineering effort to focus on the achievement of higher interconnect density and performance, which includes smaller drilled holes, buried vias, finer lines and spaces, thinner dielectrics, low loss dielectrics and thermal management. Other desirable features include two-sided assembly, large area substrates and the elimination of connectors through the use of flex or rigid-flex structures.

The primary shortcoming of MCM-L has been the limitation of interconnect density due to the use of plated through-holes (PTH) for layer to layer interconnections, and the relatively coarse line widths (compared to thin film processing) and spacings commonly practiced (typically ≥ 0.075 mm). New circuit definition technologies, the increasingly widespread use of blind and buried vias, improved drilling technology (use of 0.2 mm diameter bits is nearing production capability in some companies), the use of punching instead of drilling for small vias in thin dielectrics and the coupling of thin film surface layer processing with MCM-L structures, continue to permit the increase of MCM-L interconnect densities.

Another problem which MCM-L technology must address is the relatively high coefficient of thermal expansion (CTE) of the substrates. The use of large die on MCMs is forcing critical evaluation of the reliability of die to MCM interfaces, including both die attach and electrical connection. This reliability is critical, especially when the die connection is made by flip chip or short lead flip tape automated bonding (TAB) due to the low, thermally-induced stress compliance afforded by these techniques. Flip chip connection is seen as the

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ultimate MCM connection method, but it offers the least compliance. MCM-D and MCM-C offer the use of low thermal expansion substrates. MCM-D can be offered on Si and metal substrates for a near perfect CTE match to bonded die. MCM-C can be made from aluminum nitride, mullite, cordierite, lithium alumino-silicates and glass ceramics. These all offer near perfect CTE matches. Since the die temperature is usually more than the substrate in actual use environments, due to transient effects and the thermal resistance through the die to substrate interface, the ideal MCM substrate should have a CTE slightly higher than that of silicon. The development of new, low CTE dielectric systems for MCM-L and the emerging technology of dielectric layer lamination on low CTE base substrates offers the promise of MCM-L solutions for this thermomechanical strain problem.

Despite the delay in recognition of laminates as MCMs, especially conventional high density PWBs, demand for cost effective MCM solutions for emerging electronic systems has pressed MCM-L into the mainstream. Due to the low cost of MCM-L (relative to other MCM substrate technologies) and the wide diversity of materials, properties and manufacturing process technologies used with MCM-L, it has become a very popular type of substrate for high density, high performance MCMs. The broad vendor base, and the extensive use of PWBs in almost all current electronic systems, indicates the wide range of application functions and system frequencies supported by MCM-L.

This chapter begins by describing the standard construction process for an MCM-L or PWB. This is the process most widely used in the industry. Following that, the desirable properties of the materials used in this process are presented together with a discussion of their limitations. Because of these limitations, a number of alternatives are being pursued actively. These alternative materials and processes are presented. Bare chip mounting creates some unique requirements on MCM-Ls. These are discussed in the section on connection and repair. Finally, some examples of MCM-L configurations are given.

5.2 STANDARD MCM-L CONSTRUCTION PROCESS

Five basic process steps are used in the manufacture of MCM-Ls and PWBs. They are:

1. The preparation of individual copper foil clad dielectric layers.
2. The photolithographic patterning and etching of conductors on those layers.
3. The drilling of vias through individual layers or partial laminates to form blind and buried vias, and drilling through the total laminate

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thickness to form plated through-holes (PTH).

4. The lamination of the individual layers and sublaminates onto each other form a multilayer MCM-L. Multiple lamination steps are needed to form blind and buried via structures. A single lamination step is usually used if the board has no blind or buried vias.
5. The plating of drilled holes in single layers or partial laminates, or through the entire board thickness, to create blind and buried vias, and PTHs, respectively. The plating of the surface metallurgy follows.

Each of these basic processes consists of several steps, which are summarized in Figure 5-1. For more information, the reader is referred to PWB handbooks by Coombs [2] and Clark [3].

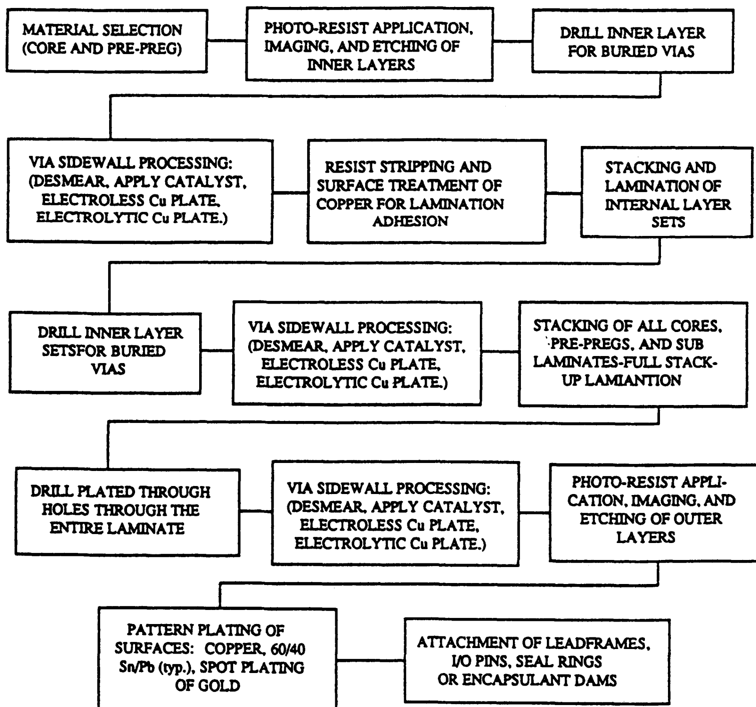

Figure 5-1 Typical substrate process flow.

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5.2.1 Dielectric Material

Two types of dielectric layers are used in typical PWBs: cores and prepregs. In both cases, the dielectric reinforcement material or fabric, typically fiberglass with the E-glass composition, is run through a coating process to impregnate the material with the selected polymer. The fiberglass may be woven in many different weaves to allow the formation of layers with various thicknesses and glass to polymer ratios. Core material is fully cured, while the prepreg material is partially cured before the material is cut to size. Core and prepreg thicknesses are selected to meet mechanical and electrical performance criteria, for example, to provide the correct value of characteristic impedance. The core layers have copper conductors patterned on one or both sides. The prepreg layers are then placed between the core layers to cause adhesion of the various layers in the stackup during the lamination period, when temperatures are elevated and pressure is applied.

5.2.2 Copper Foil (Conductor) Processing

The primary PWB conductor usually is electro deposited (ED) or rolled annealed copper foil. The foil is treated on one surface (or both, for internal Cu planes) to enhance adhesion to the polymer impregnated core or prepreg layers. Often, this surface is cleaned with mechanical abrasion, chemically microetched to increase surface topography and area, and chemically oxidized to form a thin, passivating adherent layer of CuO, further increasing foil surface area. In many instances, copper is coated with a very thin layer of tin for passivation, and laminate adhesion. The immersion tin process is less sensitive to copper material cleanliness, and protects the copper in subsequent etch processing [4].

The copper foil is roll laminated (to the dielectric), after which the full, or B-stage, dielectric curing takes place. The dimensional stability of the core and prepreg layers can be affected by the manufacturing process and storage conditions (temperature and humidity). The prepreg layers are particularly sensitive, and are stored under refrigerated, atmospheric control conditions for best results. If refrigerated, the pre-pregs should be brought to room temperature in the absence of water, especially when hygroscopic materials, such as polyimide, are used.

5.2.3 Inner Layer Photolithographic Processing

The type and thickness of copper used is based upon the specific layer function and the fineness of the features to be etched (for example, 110 μm and 19 μm

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thick Cu may be used for ground planes and fine feature layers, respectively). The core and pre-pregs surfaces are processed as described in Section 5.2.2, and photoresists (PR) then are applied. PR films are laminated to the layers or liquid PRs are applied by roller coating, spraying, screen printing or curtain coating. Resists also may be applied with electrostatic spraying or by electrophoretic deposition techniques (which refer to electroplating of organic materials in this case). Liquid resists and advanced deposition techniques often provide finer etch resolution than the older PR film lamination process.

Proponents of film PRs claim the fixed film thickness permits a more readily controlled process for etching of fine lines than the use of liquid PRs, where the user's process must provide the resist thickness control. Pattern exposure, resist development and the copper foil etching follows. Copper etchants are usually cupric chloride or alkaline ammonical based systems. The photoresist is then removed chemically and the copper surface is processed to form the desired CuO layer needed for adhesion to the overlying layer during lamination [5].

The artwork used to expose the photoresist frequently is not an exact geometric replica of the desired etched pattern geometry. The layers are subject to xy-shrinkage or expansion, but in a well characterized process, the xy-dimensional stability of the core and prepreg layers during storage, processing and lamination is controlled and well quantified. The stability data are used to modify the artwork, expanding or contracting the dimensions of the layer pattern. This modification may be graded uniformly across the entire layer, or it may vary from dimensionally insensitive to sensitive regions.

5.2.4 Blind and Buried Via Formation

Standard PWBs utilize holes drilled through the entire multilayer board thickness to electrically connect the desired metal planes. After drilling, these holes are copper plated to affect the electrical connection, forming plated through-holes (PTH). Most high density MCM-Ls utilize layer to layer electrical connections which do not span the entire board thickness. Blind vias extend from the surface into the desired layer(s), while buried vias only interconnect internal planes. After the pattern etching process, the blind and buried vias are drilled through individual layers, or sub-laminate stackups formed by the lamination of the desired inner layers. The side walls of the drilled holes, and any exposed, etched copper features are then plated with copper. Then final board lamination is performed upon the stackup of the single layers and sublaminates which form the board. The drilling and plating of the total board thickness PTHs follows.

Blind and buried vias also may be formed by precisely drilling part way through the formed laminate or sublaminate. After drilling, the laminate structure is plated to form the interconnection from the underlying layer to the top layer. This process often is considered more difficult, but may be necessary for some structures.

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The blind and buried via process is considered expensive in many circumstances, due to the difficulties in handling thin core and prepreg layers and the multiple drilling, plating and lamination operations required. This reality is mitigated somewhat by the ease with which the drilling and plating operations are performed. Small via drilling and plating of single layers and thin sublaminates is simple when compared to full laminates PTHs since via aspect ratios are smaller than those of PTHs. This greatly facilitates hole drilling, cleaning and plating. Also, the use of blind and buried vias in a high density MCM-L reduces significantly the number of PTHs needed. If the density of the MCM-L is very high, there is great design pressure to use small diameter PTHs. Since the PTHs are drilled through the entire board thickness, small diameters result in high aspect ratio PTHs. This also can have a major effect on production throughput and yield. If the use of these vias reduces the number of layers needed to achieve a circuit, there is a cost benefit of fewer layers to offset the added blind and buried via cost.

5.2.5 Lamination

The purpose of the lamination step is to "glue" all of the layers together. The pressures and temperatures which are used must be carefully controlled to drive out entrapped air, absorbed water, and solvents retained in the prepreg. The B-staged (partially cured) pre-pregs, which are placed between the cores, are the adhesive layers. During lamination, the partially cured polymer in the pre-pregs softens, flows and wets the adjoining surfaces, effecting the bond [6].

In the first step of the lamination process, the etched core and prepreg layers are stacked in precise registry using mechanical tooling and alignment pins. Laminating the type of high density PWBs used for MCM-L with vacuum presses permits the use of lower pressures, temperatures and times. The vacuum assists in the removal of entrapped air, retained solvents and water, permitting the use of less aggressive lamination parameters. These conditions also aid the control of the thickness of prepreg layers, improving the control of electrical properties such as capacitance, crosstalk, and characteristic impedance (Z_0). The optimum lamination time, temperature and pressure are interrelated. They are highly dependent upon the polymer system used in the prepreg and core, the ratio of polymer and reinforcing fabric volumes, the fabric weave, the thickness of the copper planes, the presence of blind and buried via layers or sublaminates and the dimensional control required.

5.2.6 Drilling

Computer aided design (CAD) data from the design software used to create the

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artwork also is used to create a drill list, which defines the sizes and locations of the holes to be drilled. This information is downloaded to high speed, multi-spindle drilling machines which determine the location of the next hole to be drilled by use of the mechanical data.

There are many sources of drilled hole location errors. To increase production throughput, it is common practice to stack the boards on the tooling under each drill spindle. Drilling through multiple boards with each drill stroke increases productivity, but increases the risk of hole position errors. New drill bits are available which utilize advanced materials and which incorporate well designed flutes in the drill. Improved drill bits are important, but not sufficient to solve stack drilling problems. The registration tooling, and the registration features drilled and routed in the boards prior to layer processing, must be accurate and consistent. Since each board may not have contracted or expanded identically in processing, the stack tooling must be able to accommodate these dimensional differences while providing suitable dimensional registry to the xy-program driving the positioning system on the drill machine [7].

Another major source of drill position error is wandering of the drill, which implies drill tip movement in the xy-plane during the z-axis excursion through the board. This can be caused by inaccuracies in the drill head (vibration, precession, worn bearings, nonorthogonal z-axis motion), but many errors are due to characteristics of the board stack. Typically, special cover and back up sheeting materials are placed over and under the stack. These entry and backup materials are intended to act as drill guides and to reduce drill breakage. Three layer laminates of special aluminum alloy foil with a cellulose core and aluminum alloy about a thin wood core are used widely as entry and backup materials, respectively [8].

In general, features which increase drill position errors and drill breakage are thick board stacks, high aspect ratio holes (~ > 3:1), high glass content, excessive drill rates, loosely stacked boards and dull drills. Core and prepreg layers measuring 100 μm thick are commonly used in the fabrication of high density, low thickness PWBs. High volume production use of 200 - 300 μm diameter drill bits for these structures is ongoing, while the most widely used drill diameters are as large as 500 μm.

Drill hole quality also is critical for the construction of the highest density surface layers. In these cases, the drilled hole is equal to, or smaller than the width of the surface feature it electrically connects to internal conductors. This reduces the surface area required to fanout the surface conductors from the die to vias, or PTHs. Drills as small as 50 μm diameter are being used in development work, while 100 - 150 μm drills are being used in prototype manufacture of MCM-Ls.

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5.2.7 Plating of Drilled Holes

During drilling of vias and PTHs, the frictionally heated drill bit causes polymer residue to smear and coat the hole wall. This residue must be removed to allow plated copper to bond to the structurally sound bulk dielectric and to the cross section of the copper features through which the hole was drilled. This operation is referred to as desmear and is commonly performed using concentrated sulphuric acid, alkaline permanganate solutions or oxygen plasma cleaning. The solutions used also must make the hole walls hydrophilic to enhance wetting by electroless Cu plating solutions and to eliminate bubble entrapment in the holes. The desmear process difficulty increases with increasing hole aspect ratio and decreasing hole diameter [9].

After desmear, the polymer and glass surfaces of the drilled holes must be treated to permit plating and good adhesion. The units are immersed in a palladium-tin compound solution for surface activation, permitting deposition of both the palladium and tin. It is necessary to remove the tin in a subsequent post activation cleaning step. The board is then placed in an electroless Cu plating bath where the bath chemistry, temperature and mechanical agitation are critical to ensure uniform Cu deposition, good Cu adhesion, and proper Cu microstructure for good mechanical properties [10]. Electrolytic Cu plating follows to build the copper thickness to the desired levels. The copper surfaces of the inner layers are then photolithographically processed and etched to form the desired conductor patterns. The surface of the conductors are then cleaned, etched and oxidized to enhance adhesion to neighbor layers. A schematic cross section of an MCM-L/PWB structure is shown in Figure 5-2.

5.2.8 Processing of Surface Layers

The final plating of the MCM-L surface defines perhaps the greatest difference between conventional PWBs and MCM-Ls. Conventional PWBs are made for the surface mount or through-hole soldering of packaged devices which usually possess metal leads. Thus, the copper attach pads on the PWB surface are plated typically with Pb-Sn solder, suitable for the mass reflow of surface mount devices, or for the attachment of through-hole components with wave soldering. The surface metallurgy of MCM-L often requires multiple process steps to permit selective plating of gold on some sites and lead-tin solder on others. These steps involve the application of plating resists, imaging, developing, plating, resist stripping and a repetition of this sequence for each different metal finish to be applied. Soft gold plating may be desired for wire bond pads, while hard gold is needed for edge connectors, and 60/40 tin-lead solder may be required for soldering of TAB leads.

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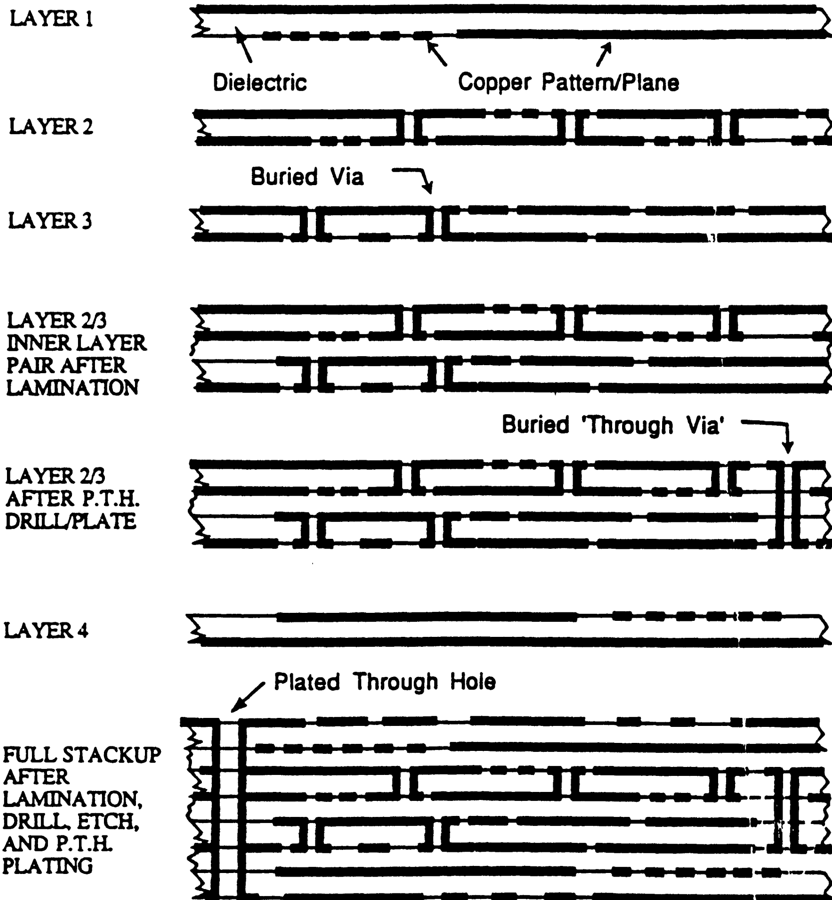

Figure 5-2 Cross section of an MCM-L printed wiring board. The schematic drawing shows construction of a typical MCM-L substrate, exhibiting blind and buried vias and a typical lamination sequence.

After the PWB is fully laminated, the PTHs are drilled through the entire board thickness, and plated using processes similar to those described above. A PR is applied to the copper foil surface, and is imaged and developed. The PTH sidewalls and the copper exposed on the surface is then plated with Cu/Ni/solder (typically 63/37 Sn/Pb solder). The PR then is stripped and the newly exposed

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Cu is etched away, effectively using the solder as an etch resist. The surface is PR coated again and patterned to protect the regions where solder plating is desired. The exposed solder is etched away. At this point, the solder may be reflowed. The surface then is coated with a photoimageable solder mask, imaged and developed, exposing the solder plated pads. This procedure is called solder mask over bare copper (SMOBC) [11]. Alternative SMOBC process flows are possible. Areas requiring future Ni/Au plating or other non-solder treatment, are to be masked off through much of the SMOBC process. The wire bond pads typically are plated with 5 μm of Ni, and 0.5 - 1.0 μm of high purity (~ 99.99%) soft Au. The use of 0.2 - 0.3 μm of electroless gold for wire bond pads is increasing in Japan.

Additional applications of PRs and more photolithographic processing are often required to permit the final spot plating of the Ni/Au regions. Reflowing of the solder, before or after Ni/Au plating, improves resistance to oxide formation, but it causes the pad surface to dome due to the surface tension of the molten solder. This domed surface can cause lead alignment problems during TAB outer lead bonding (OLB).

Selective, or spot plating, is a critical process for MCM-L since it is very common to connect wire bonded and TABed die on the same MCM. In the near future, flip chip attachment on MCM-L will become common, so it may be possible that three distinct bare die connection methods (wire bond, TAB and flip chip) will be practiced on a single MCM. This is likely to require even more sophisticated selective plating procedures.

Electrolytic plating is commonly used for the deposition of Ni, Au and Pb/Sn solder finishes. This requires that the features to be plated are connected to a plating bus. The need for connections to fanout to the bus can interfere with circuit routing design. If the fanout nets are not on the surface, they will not be etched away after plating. High frequency systems will encounter signal integrity problems if plating bus connections remain after removal of the plating bus. These useless nets act like signal stubs and can contribute to circuit noise due to increases in driver loading, crosstalk, reflections, radiated noise and coupled radiation. Electroless plating does not require the use of plating bus connections, but usually does not permit the deposition of the desired thicknesses of Au and solder.

5.3 MATERIAL CONSIDERATIONS

There are four types of materials used in the fabrication of a laminate:

1. **Core dielectric layers**. These layers are rigid materials, usually comprised of reinforcing fiberglass fabric and a fully cured epoxy matrix. Some core dielectrics use no reinforcement.

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2. **Prepreg dielectric layers**. These layers are flexible materials, usually composed of a fiberglass reinforcement fabric and a B-staged epoxy matrix. This material attains rigidity with full cure during the lamination and post lamination bake processes.

3. **Conductor materials**. The typical conductor material used for power distribution and signal interconnection is etched copper foil.

4. **Finishing materials**. Typically tin-lead solders or nickel-gold, are plated on the external surface copper bonding pads to permit die connection.

The epoxy-glass dielectric described above is referred to as FR-4 material. In the following sections, the ideal material properties are discussed and alternative materials are presented and compared.

5.3.1 Dielectric Layers

MCM-L dielectric layers are usually composite materials consisting of a reinforcing material and a continuous polymer matrix phase. Flexible circuits, and some advanced MCM-L substrates, use unreinforced polymer dielectric layers. In this section, the various polymers, reinforcement media, and the resulting dielectric layer products are discussed in terms of their physical and electrical properties, and their effects on MCM-L processing. Table 5-1 provides a listing of the physical and electrical properties of a wide range of materials used in MCM-L fabrication.

The laminate structure of the typical PWB is a ternary composite of phases: resin, reinforcement fiber or filler and copper conductor. The dielectric constitutes the major volume of the MCM-L. The copper conductor planes are commonly 9 - 105 μm thick, while the dielectric layers typically range from 25 - 500 μm in thickness. All three phases contribute to the electrical and mechanical properties of the final board. Polymer and reinforcement phase effects are discussed in the following section.

With standard types of laminates, both the fiberglass fabric and the matrix resin are continuous in the xy-plane, while only the resin is structurally continuous along the z-axis. Thus, laminate structures exhibit anisotropy, where the macroscopic properties of laminate structures are quite uniform in the xy-plane, but different in the z-axis. The differences in the basic material properties of the resin, reinforcement and the conductor lead to stresses in the laminate

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Table 5-1 Properties of Materials Used in MCM-L Fabrication.

Materials	xy-Plane Thermal Expansion (ppm / °C)	z-Axis Thermal Expansion (ppm / ° C) (<Tg)/(>Tg))	Tg; Glass Transition Temperature (°C)	Thermal Conductivity (W / m ° K)
FR4 (epoxy-'E' glass)	16-18	60 / 320	125-140	0.16-0.4
Polyimide (PI)-E glass	13-15	40 /190	225-260	0.3-0.6
High Tg epoxy-E glass: Risho CS-3665	13-14	50-220	200	
Teflon-E glass	20		75	0.26
Epoxy-aramid (PPDETA)	6.5		172	0.18
PI-Kevlar 108	5.0-8.0	85	250	
Epoxy-fused silica	6.0-12.0		125	
PI-fused silica	6.0-12.0	30	250	
BT epoxy-Kevlar 120		73.7		
High Tg epoxy-fused silica #525	6.0-12.0	65		
'Gore-Ply' (cyanate ester-expanded PTFE)	55		190	
PI-unwoven Kevlar 'ROHSI 2800' (Rogers)	16	24	Thermoplas.	
PI film: Kapton H	20-25			
Upilex S				
Polyester film	25-30			
Epoxy resin (#5010)	55			
PTFE	224	224		
'E'-glass	5			
'S'-glass	2.3			
Aramid fabric	-2			
Unwoven Aramid / PI	1.35-2.25			
Fused silica fabric	0.54			
Copper (CDA 102)	17.3	17.3		393
Aluminum (elemental)		22.1		240
Aluminum (6061)		21.1		200
Molybdenum	5	5		146
Kovar		5.3		17
Cu/Invar/Cu: 20/60/20	5.5			169 (Z=23)
12.5/75/12.5	3.15			114 (Z=18)
Cu/Mo/Cu: 20/60/20	6.7 (20 C)			141(Z=113)
13/74/13	5.8 (20 C)			122(Z=98)

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Table 5-1 Properties of Materials Used in MCM-L Fabrication (continued).

Materials	Tensile Modulus (10E6 psi)	Tensile Strength (10E3 psi)	Dielectric Constant (1 MHz, 25°C)	Volume Resistivity (Ω-cm.)	Dissipation Factor (%)
FR4 (epoxy-'E' glass)	2.5	40	4.0-5.5	4.00E+14	2.2
Polyimide (PI)-E glass	2.8	50	4.0-5.0	4.00E+14	1.3
High Tg epoxy-E glass: Risho CS-3665			4.3	3.00E+14	1.3
Teflon-E glass	0.2		2.3-2.6	1.00E+10	0.2
Epoxy-aramid (PPDETA)	4.4		3.7		2.6
PI-Kevlar 108	4	30	3.95	1.00E+12	1.7
Epoxy-fused silica					
PI-fused silica				1.00E+09	
BT epoxy-Kevlar 120			3.51		1.1
High Tg epoxy-fused silica #525					1.3
'Gore-Ply' (cyanate ester-expanded PTFE)			2.6	> 10E+07	0.3
PI-unwoven Kevlar					
'ROHSI 2800' (Rogers)	0.12		2.8		0.3
PI film: Kapton H	0.4	25	3.5	1.00E+12	0.25
Upilex S	1.3	57	3.5	1.00E+11	0.13
Polyester film		20-40	2.8-3.2		0.3-1.6
Epoxy resin (#5010)	0.39		3.8		
PTFE	0.05		2.2		
'E'-glass			6.3		
'S'-glass			5.3		
Aramid fabric	18.5	440	2.3		0.7
Unwoven Aramid / PI					
Fused silica fabric					
Copper (CDA 102)		32-55		1.67E-06	
Aluminum (elemental)		45		2.66E-06	
Aluminum (6061)		35		4.30E-06	
Molybdenum		95			
Kovar		75		4.70E-05	
Cu/Invar/Cu: 20/60/20	19	60			
12.5/75/12.5	19	60			
Cu/Mo/Cu: 20/60/20	20	100		3.40E-06	
13/74/13	39			3.80E-06	

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structure as the individual phases attempt to behave independently during environmental and electrical stressing. One of the major reliability problems associated with PWBs is barrel-cracking, or the cracking of the plated through-hole copper during temperature cycling. This is due to the fact that the z-axis thermal expansion is much higher than the xy-thermal expansion of typical boards. The thermal expansion of copper is ~18 ppm/°C, from 0°C - 125°C, which closely matches the range of xy-thermal expansion (~13 - 18) offered by typical fiberglass-based laminates. The z-axis thermal expansion can be 3 to 5 times the thermal expansion of copper, at temperatures below the board glass transition temperature (T_g) and 10 - 20 times higher above the board T_g.

Desirable dielectric properties shown are in Table 5-2. With most materials, the dielectric layers typically take two forms, the core layers (fully cured in advance), and the prepreg layers (partially cured, or B-staged, in advance). The compositional makeup of the two types of layers can vary in the board, but designers strive to achieve a balanced structure, where the copper and dielectric content are fairly uniform throughout the structure. This balanced structure reduces bowing, or camber, after lamination due to variations in the thermal expansion and cure shrinkage of individual layers on opposing sides of the board's "neutral plane," which extends through the center of the laminate. This is why MCM-Ls are usually symmetric through the board center in terms of signal and reference layers. If the board is thin and flexible, solder masks also are used in equal proportion on both surfaces, even if it is really only needed on one surface. The solder masks usually have higher thermal expansions than the board and induce board camber at room temperature, or while the board heats up in an assembly operation or in an electronic system.

Varying the ratio of reinforcement to polymer and the type of fabric reinforcement and polymer, permits moderate variations in the properties of the final board, but it may induce significant variations in fabrication process control. For example, increasing the resin content in the core and prepreg may reduce the dielectric constant of the board. On the other hand, a higher polymer content may cause greater lateral displacement during lamination. This can cause problems in dimension control or cause difficulty in hitting the internal pads during hole drilling. Increasing the glass fabric content, or changing the fabric weave, may improve layer thickness control after lamination, but also may induce lamination voiding and cause increased drill wear and breakage. Difficulties in process control and subsequent reliability and assembly problems, (the result of the low T_g for FR-4 resins and the resultant high CTE at typical assembly temperatures), have been the driving forces behind the development of new polymers and dielectric layers.

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Table 5-2 Desirable MCM-L Substrate Properties.

ELECTRICAL	
Low dielectric constant	1.0 - 3.0
Homogeneous dielectric	Isotropic properties
Low dissipation factor	≤ 0.1% for desired frequencies
PHYSICAL	
Low moisture absorption at saturation	< 0.01%
Low rate of moisture absorption	Slower than FR-4 (< 0.05% sat.)
High glass transition temperature	> 250°C
Low CTE (xy-plane)	Close to Si (3.3 ppm/°C, 0-200°C)
Low CTE (z-axis)	Match Cu (18 ppm/°C, 0-200°C)
High Cu adhesion	> FR-4
Low lateral deformation during lamination	< FR-4
High modulus of elasticity and high strength	Resist encapsulant induced camber

5.3.2 Polymers for Dielectric Layers

A variety of high T_g polymers are available for board manufacturers. FR-4 grade PWBs are made from a relatively low glass transition temperature (T_g = ~ 125°C) epoxy (commonly supplied by Shell Chemical) with an internal E-glass fabric reinforcement. Other widely available polymer materials include tetra- and multifunctional epoxies (T_g range of ~150°C - 200°C), cyanate esters (T_g = ~180°C - 200°C), bismaleimide triazine (BT) (T_g = 175°C - 190°C), and polyimides (T_g = ~240°C - 270°C). Triazine is a cyanate ester, and often is blended with bismaleimide (one of the precursor constituents of polyimide) in a range of customer specified ratios to achieve the desired properties. Mitsubishi is the primary source of the BT resins.

Microwave applications often demand the use of very low loss materials made from fluorinated thermoplastic glass fabric laminates. New materials are constantly being developed and evaluated. Recently Hercules Corp. announced a silicon-carbon thermoset polymer (SYCAR) which is being evaluated for PWBs in conjunction with PolyClad Corp. This material has a T_g of ~180°C, low dielectric constant, and extremely low moisture absorption characteristics [12]. Low moisture absorption aids processing, reduces risk of delamination during high temperature assembly operations and reduces risk of conductor corrosion and polymer microcracking. Polymers typically adsorb and desorb water as a function of the local relative humidity, and processing environment. This

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dependency upon the relative humidity of the environment causes variations in the dielectric constant and in the loss characteristics (both increase with increasing water absorption) as polymer water content adjusts dynamically to the ambient. A material which shows low moisture sensitivity provide a more stable transmission line environment with much less variation of line capacitance and characteristic impedance than other polymers. General Electric [13] recently has come out with a high T_g epoxy (olefin-modified) which is cost competitive with conventional low T_g FR-4 epoxies.

5.3.3 Reinforcements for Dielectric Layers

FR-4 grade dielectric materials use woven fiberglass fabrics for reinforcement. The most commonly used glass is E glass, the designation applied to the specific silicate glass composition with a dielectric constant of 6.3 and a thermal expansion of 5 ppm/°C. Other glasses are available, but are not commonly used due to higher cost. An example of an alternative glass fabric is S-glass, which has a dielectric constant of 5.3 and a CTE of 2.3 ppm/°C [14].

Reinforcing fabrics are available in a wide number of weaves, in which the following parameters are varied: fiber diameter, fibers per thread, number of threads per inch, tightness of the weave and type of weave. The ratio of polymer resin to fiber volume in the dielectric layers and the fabric characteristics determine the properties of the core and prepreg layers. The fabric reinforced dielectric is a nonhomogeneous material. During lamination, the prepreg resin is displaced as it flows to accommodate the raised copper pattern to which it is bonding. This results in resin-rich and glass-rich regions. The resin flow and the nonhomogeneity of the dielectric actually create microregions of variable dielectric constant in the dielectric. The knuckles (xy-crossovers) of the fabric create high spots which actually may press against the copper pattern regions after lamination. At very high frequency, the local variations in the dielectric medium surrounding the conductor transmission line contribute to pulse dispersion and scattering. This effect usually is not too significant until very high frequencies, where the signal wavelengths approach the dimensions of the fabric features.

5.3.4 Copper Conductors

Copper foils used for PCBs all have high copper purities (> 99%). The foils are made usually by rolling, but also can be made by electrodeposition (ED). The microstructural morphology of rolled copper is affected by the noncopper additives, the heat treatment of the original large cross section copper feedstock, the rolling conditions and the annealing process. The microstructure of the ED

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copper is controlled by the chemistry of the plating bath and the plating conditions (temperature, current density, etc.). The microstructure and copper chemistry affect preprocessing steps prior to lamination to prepreg and core layers, and subsequent micro etching processes prior to board lamination. The etching behavior of the copper is also greatly dependent upon the microstructure and foil chemistry.

Copper deposited in PTHs and on the surfaces of the PWB, develops properties highly dependent upon the plating bath chemistry and plating conditions. Probably the most critical concern is the thermomechanical properties of the PTH copper. Due to the high z-axis thermal expansion mismatch of most PWBs and PTH copper, it is desirable to use high elongation, high ductility and high tensile strength copper. Proper plating bath chemistry (usually proprietary to vendors) and good process controls are needed to attain the desired set of properties. The strain on the copper increases with board thickness, so this type of copper is critical for thick boards, high aspect ratio PTHs and when materials with very high z-axis expansions are being used. The reduction in the quantity of PTHs in a board through the use of very low aspect ratio blind and buried vias reduces the risk of copper failure.

5.4 FLEXIBLE ("FLEX") CIRCUITS

Flex circuit MCM-Ls are constructed with dielectric and conductor planes which permit the finished circuit to retain mechanical flexibility after circuit finishing. The typical dielectrics are unreinforced polymer films, most commonly polyimide or polyester. The conductors typically are copper, aluminum or polymer thick films. The conductor-dielectric layers are formed usually by bonding the metal foil to the dielectric with an adhesive, or by electroplating copper to an adhesion layer deposited on a dielectric surface. The degree of flexibility is a function of the physical properties of the dielectric, copper and adhesive (if used), the dielectric and conductor plane thicknesses, and the number of circuit layers.

Multilayer structures can be formed using adhesive layers between conductor planes. Vias, PTHs and laminates are fabricated using processes similar to those used for rigid PWBs. SHELDAHL Corp. uses a special film to laminate layers together. The film has an adhesive matrix with properly sized and spaced solder balls dispersed throughout. During lamination, the solder particles melt as the adhesive is softening. The solder contacts and wets any capture pads about PTHs that were formed previously and about plated blind and buried vias, effecting plane to plane conductivity. This eliminates the need for drilling and plating holes for inner layer sublaminates, providing a savings in processing costs [15]. It is likely that unreinforced, flexible dielectric layers, or multilayer

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structures, will begin to be laminated into the interior of rigid laminate structures to exploit the lower dielectric constant and the << 100 μm thicknesses commonly available with these materials. When flex circuits are laminated to the surface of rigid boards, leaving flex circuit sections extending beyond the edge of the rigid component, the resulting module is commonly called rigid flex. Rigid flex segments may be needed for attachment of massive components and connectors.

Very low cost, low circuit density flex circuits are made with polyester films. These types of films are used commonly with polymer thick film conductors (carbon-loaded, or carbon/silver-loaded epoxy) to make keyboard, phone circuitry and low cost consumer electronics. CASIO Corp., for example, uses polyester films as the basis of many of their circuits. Calculator circuits often are fabricated from polyester films, with aluminum foil laminated to a surface. This surface is etched to form the circuitry; the opposing side is patterned with conductive epoxy. Side to side connections are made by filling vias with the conductive epoxy. Additional conductive layer patterns are formed on top of the aluminum or base conductive polymer layer by patterning a dielectric layer between the conductor planes. Components are attached typically using anisotropic conductive adhesives (z-axis conductive only) because standard polyethylene terephthalate (polyester) films begin to decompose at ~180°C, which is less than the eutectic temperature of Sn/Pb solder. For calculator circuits, TABed LCD driver and microprocessor die are attached to form the keyboard circuitry. A laminated, multilayer version of this type of MCM-L forms a circuit which represents the lowest cost for a low interconnect density MCM.

5.4.1 Flex Circuit and Connector Integration

PWB and MCM assemblies often require the use of connector components to connect between the circuit and the remainder of the system. The use of a connector involves forming two electrical connection interfaces. The PWB or MCM must connect with the connector, and the connector must couple to the rest of the system. If the original circuit was a flex circuit, the functionality of the connector can be integrated, in many instances, with the circuit itself. This may reduce part cost, increase ease of assembly and improve reliability due to the elimination of a connection interface. Since a transmission line experiences some level of an impedance discontinuity at the interface with the connector, elimination of this interface provides an enhanced level of signal integrity in the flex. The flex circuit also allows the incorporation of an integral cable(s) into the MCM-L. This cable can twist, turn and bend, permitting system design options not available with other types of substrates.

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5.5 ADVANCED MCM-L MATERIAL AND PROCESS TECHNOLOGY

The standard materials discussed in previous sections may present some limitations when attempts are made to use these materials to build advanced high performance MCM-L systems. These issues are summarized below:

1. Standard photolithographic patterning and copper etching limits the minimum line widths and spacings.

2. The low glass transition temperature (T_g) of FR-4 limits high temperature assembly processes and results in high thermal expansion values both below and above the T_g.

3. High density MCMs may utilize large die with low stress compliance interconnections (straight TAB or flip chip). In these cases, the relatively high thermal expansion of FR-4 may not be acceptable.

4. The dielectric constant of FR-4 may not be suitable for high frequency, low power systems.

5. The minimum thickness of standard FR-4 dielectric (~ 100 μm) may not permit attainment of the desired characteristic impedance value if very fine line technology is used. The minimum thickness also may impede attaining thin, low mass modules for portable electronic systems.

6. The need to drill PTHs greatly reduces available signal routing channels in a module. The large diameter of even the smallest drilled vias still negatively impacts routing.

Advanced MCM-L technologies which address these, and other, problems are discussed in this section.

5.5.1 Integral Termination Resistor Technology

High frequency transmission line interconnects often require terminations to reduce reflections due to characteristic impedance mismatches. Resistors are most commonly used for line termination, although active termination with diodes has been used. If the interconnect is highly lossy (DC resistance is high), it may be possible to use the net itself for series damping of reflections. These lossy nets cause significant rise time degradation and signal attenuation, introducing RC time delay effects. None of these characteristics are beneficial

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to interconnect performance. In most instances, resistors are used in series or parallel termination schemes. It is possible to integrate resistors into laminate structures using two or three processes.

Nickel alloy films can be formed on core layers used for standard PWBs. The film is then photo patterned and etched to form the desired resistive element. This layer is laminated into the interior of the PWB. The normal processing of drilling and hole plating interconnects the resistor to the desired net and terminating voltage plane. This process is licensed from OHMEGA Corp. and is utilized by a large number of PWB vendors. Since ECL series termination uses a high value pull down resistor and a resistor in series with the driver and the load, this structure is more difficult to construct than a parallel termination structure where a single resistor is close to and in parallel with the receiver.

Polymer thick film resistors also are being used to form integral resistors in PWBs. In this case, internal layers are screen printed with resistor paste, and laminated into the stackup. This provides another method that is potentially lower cost [16].

In prototype structures, thin film resistors have been formed on the surface of high temperature PWBs, permitting high density termination resistor arrays on the MCM-L surface. The composition of the possible resistors may vary from titanium nitride, to nichrome, etc. The surface real estate is very valuable, and is frequently better used for device attachment, so the internal resistor schemes often have the most appeal.

5.5.2 Additive Conductor Processing

The conductor processing described above is referred to as subtractive processing since the circuits are defined by etching, or removing, copper material (as discussed in Chapters 2 and 7). Another method of circuit definition, additive processing (AP), is becoming more popular as the size of circuit features is decreased and the mechanical requirements of conductors are getting more severe, due to greater board thicknesses, and board bending requirements. With additive processing, the surface of the PWB is activated with a plating catalyst, commonly palladium, coated with a photoresist developed to expose the areas where plating is desired, and then immersed in the plating solution for the controlled deposition of copper. Copper thickness control is easier than standard electrolytic Cu plating, and the plating in high aspect ratio PTHs is more uniform. The properties of AP copper are dependent upon the plating bath chemistry and deposition process controls, but the copper usually possesses higher ductility, elongation and tensile strength than circuits fabricated from laminated copper foils, using standard subtractive processing. The full additive copper, deposited on PTHs, possesses greater resistance to barrel cracking than

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electrolytically deposited copper (due to the higher ductility provided by AP copper), but AP copper usually shows lower adhesion strength than subtractive copper. This can be a problem with surface bond pads, which are exposed to considerable thermomechanical abuse during the device bonding and attachment process and during repair cycles.

One of the major attributes of AP copper is the generally accepted ability for this process to produce fine lines more readily than subtractive processing. The subtractive process uses photolithographic and etching processes which remove the copper exposed through the photoresist, so there is a risk of uneven etching of the resulting conductor line. The enchant tends to etch under the protective resist as it etches through the copper foil (undercutting). With a narrow conductor line width, the undercut from both sides of the conductor can approach the width of the line. The use of thin copper foils (for example one-half ounce copper, 18 μm thick) reduces the undercutting problem. Unless the undercutting is well controlled, the etching of 50 μm lines, may force the use of a line spacing of 75 - 100 μm. AP conductors tends to be square or rectangular in cross section, since AP circuits are defined by plating up through photoimaged resists, which typically possess straight sidewalls. Since there is no undercutting, 50 μm lines may be processed with finer spacings than typically possible with subtractive processing, offering the potential for AP lines at < 50 μm. Since the patterned PR is controlling the line width, it also is possible to plate close to the full thickness of the PR to achieve 50 μm lines, which are thicker than those typically possible with subtractive processing. With standard AP, the PR usually is removed after plating the conductors.

The use of a similar process allows the construction of a multilayer additive circuit. In this case, the initial PR layer is not removed after plating the initial AP circuit layer. A secondary PR layer is applied, covering the initial AP copper pattern. This PR layer is imaged to permit via etching, and the via post then is plated. The secondary PR is activated with a plating catalyst. A ternary PR layer is applied, imaged and developed, exposing the underlying activated, secondary polymer layer, in the regions in which the deposition of the AP circuitry is desired. AP of the Cu circuitry follows. The use of this type of additive processing is being developed by a number of companies, including IBM, Ibiden and Litronics.

The unfilled liquid polymers typically have been photosensitive acrylate-modified epoxies, which are not as environmentally stable as unmodified epoxies (lower solvent resistance, moisture resistance and glass transition temperature). The dielectric and PR films usually are applied in liquid form, but unfilled polymer films also are being used. Unmodified epoxies (liquids or B-staged films) are being evaluated for this type of surface circuit fabrication. Photoimaged and developed via or circuit formation is not normally possible with these unmodified epoxy films.

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These additive surface layers provide very high routing density. One of the chief factors limiting the extension of classical MCM-L to very high performance, high density circuits is the inability to achieve the fanout from a dense array of interconnections without greatly increasing the effective die connection footprint. The ability to form conductor and dielectric features with this "near thin film" process technology offers the greatest extendability to future systems for MCM-L. This near thin film technology includes AP, use of unreinforced dielectrics (liquids or films) and actual thin film patterning of buried conductor planes, constructed upon an MCM-L base. This process offers the lowest cost option for MCM-D type of circuitry, due to the use of the MCM-L substrate base and the unique processes used to create the surface pattern layer(s). This type of substrate offers the promise of great extendability for MCM-L into very high performance systems, and represents the future of MCM-L.

5.5.3 Advanced Reinforcement, Rigidifying Materials

The use of standard E-glass fabric as the reinforcement material in FR-4 boards has a number of limitations. The dielectric constant and thermal expansion are higher than desired. The use of a woven fabric creates a core layer surface texture which may impede the formation of very fine conductor lines and spaces. The use of novel fabric structures and materials, particulate filler replacement of fabrics, and the use of porous polymer film reinforcements provide significant improvements. In another approach, laminates are built upon preformed rigid substrates. Organic laminates constructed on cofired multilayer ceramic or MCM-L bases also are possibilities. This progression of improved materials and processes is leading toward the merger of laminate (MCM-L) and thin film (MCM-D) technologies.

Advanced Dielectric Filler Materials and Structures

Compositech Corp. has developed nonwoven, glass reinforced dielectric materials with various polymer matrices. The elimination of fabric knuckles in boards using these dielectrics for all layers, or only surface layers, can provide very smooth surfaces, aiding in the formation of fine geometry surface conductor features and the assembly of very fine pitch surface mount devices [17].

Gore Associates Inc. manufactures a highly porous, expanded poly-tetrafluoroethylene (PTFE) film for use as the reinforcement for dielectric layers. This material is a high temperature thermoplastic possessing very low dielectric constants, ε_r, of 2.2 and 1.2, respectively, in bulk and expanded states. It can be coated or partially impregnated with a variety of polymers to form dielectric layers that can be laminated. A wide range of thermomechanical and electrical

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properties results. The film can be manufactured in thin layers, permitting construction of 25 - 50 μm dielectric layers. When processed with a low dielectric constant (2.9), and high glass transition temperature, cyanate ester polymer, a high performance material designated Gore-Ply, is formed. The Gore-Ply™ (ε_r = 2.7) layers are used as pre-pregs to laminate Gore-Clad layers. These are comprised of a polyimide film core, with copper foil laminated to the polyimide using a material similar to very thin Gore-Ply layers. The Gore-Clad layers serve a role similar to the fully cured core layers in conventional PWBs. Entire boards can be constructed with this material, or it may be used only in critical planes [18].

Rogers Corp. makes a material designated RO-2800, which is a PTFE material incorporating filler materials that are a blend of particulate crystalline and glassy ceramic materials. A dielectric with low, nearly isotropic thermal expansion, and a low dielectric constant (ε_r = 2.8) is the result. Since this material is a thermoplastic, the designation of prepreg and core layers has no meaning. Copper-clad layers are processed in typical fashion, and laminated at temperatures higher than those used for thermoset PWB materials. Since the dielectric reinforcement is not continuous in the xy-plane, processes which guarantee that excessive lateral flow does not occur must be used [19].

Fused silica (silicon dioxide, SiO_2) fabrics also have been used when its low thermal expansion (~ 0.5 ppm/°C, 0°C - 100°C) and lower dielectric constant (ε_r = 3.8) are desirable. The resulting dielectrics have CTEs of 6 - 12 ppm/°C, with low to normal resin contents. The materials with a CTE of 6 - 7 ppm/°C are not readily laminated due to the low resin content. The hardness of fused silica creates dielectric layers which are harder to drill, causing increased drill wear and breakage. Fused silica fabric has limited availability and is more difficult to manufacture due to the very high temperatures needed to form the fibers, and the very high viscosity of fused silica during the fiber drawing process [20], [14].

Organic aramid fiber fabrics also are used for MCM-C. The fabric is similar to those used in the fabrication of tires and bullet proof vests. These fibers are exceptionally strong, and tough, but also contribute to high drill wear and breakage. Adhesion of the polymer matrix material to the aramid fibers has been a problem. Adhesion has been improved in recent years, but may still pose a concern with some material systems and applications due to the high moisture absorption shown by aramid fibers. Poor adhesion in any laminate can lead to separation at the interface of the polymer and the fibers, and polymer microcracking, due to thermal or mechanical stress cycling. The low density, and negative thermal expansion of aramid allows the formation of low weight, low CTE PWBs. PWBs containing Aramid also are considerably more expensive than standard FR-4 boards but in a pinch, they may stop a bullet!

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Non-woven, random orientation, aramid fiber fabric for PWB reinforcement also is available. This material also provides smooth surfaces, and essentially provides isotropic properties in the xy-plane. The non-periodic nature of the fiber overlap and orientation allows smooth surfaces after lamination. Of course, as with the woven aramid fabric, a low xy-thermal expansion results.

Graphite, or carbon fibers, also are used to construct reinforcing fabrics for use in the construction of very stiff and thin boards, possessing a low thermal expansion and improved thermal conductivity. Uses of this type of fabric have been limited to aerospace or military applications.

Rigid MCM-L Bases and Cores

Ibiden Corp. developed CERACOM™ substrate technology, which uses a porous ceramic substrate as the base of a single sided substrate, or as the core of a two sided substrate. The preferred ceramic is based upon cordierite, a magnesium-alumino-silicate crystalline phase, possessing a low thermal expansion, a low dielectric constant, a high thermal conductivity (relative to standard laminate structures) and a high modulus of elasticity (relative to standard laminates). Laminate structures for the CERACOM technology are prepared by lamination of prepreg layers on the epoxy impregnated porous cordierite. Conductor layers can be processed with standard subtractive and additive procedures. Structures that interface with flip chip solder bump arrays on 250 μm pitch are readily fabricated with fine pitch additive plating of conductors. PTHs are drilled with the same equipment used with standard boards. The hardness of the ceramic material reduces drill life. The thermal expansion of the resulting CERACOM module increases with the number of laminate layers, and expansions of 5 - 7 ppm/°C are typical for structures with three conductor layers on each side of the substrate. This structure is likely to have a conductor layer formed on each surface of the cordierite, and two additional conductor planes formed over the base conductor plane on each side of the core. The middle plane on each side can be a power or ground plane, allowing the construction of embedded microstrip transmission lines on all signal interconnect layers. This type of substrate has been used for flip chip connections on a 250 μm chip array I/O pitch. The low thermal expansion of this MCM-L substrate offers great promise for flip chip modules, particularly when large die are used [21]-[22].

The use of a base substrate for the construction of a laminate, as exemplified by CERACOM, may represent an emerging generation of MCM-L substrates. In the case of CERACOM, the cordierite ceramic core possesses no interconnect functionality, except as provided by the PTHs. There is no reason why a low CTE multilayer ceramic base could not be used in the construction of an MCM-L substrate. In this case, the base would possess a number of interconnect planes which interconnect to the organic dielectric and copper layers laminated to the

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surface of the bases. The interconnection would be affected by use of PTHs (in CERACOM™), adhesive contacting pads on the ceramic surface or by the use of thin film metallurgy to connect from the surface pad to the laminate via sidewall to the surface contact pad. A low CTE metal base also could be used for the construction of an MCM-L laminate stackup.

In another approach to reducing the thermal expansion of the MCM-L substrate, low CTE metal foil layers are laminated into the PWB stackup. Materials typically used are copper clad Invar (Cu/Invar/Cu), and copper clad molybdenum (Cu/Mo/Cu). The CTE of the metal foils is a function of the cross sectional ratio of Cu to Invar, and of Cu to Mo. Boards with a CTE of approximately 6 - 7 ppm/°C are attainable using these metals. During processing, oversize drills are used to drill some of the holes in the metal plane. These holes are filled with an insulative epoxy plug to prevent PTH sidewall metal from shorting to the heavy metal planes. Subsequently, the laminated substrate is drilled through the via plugs and in locations not previously drilled where electrical connections to the plane are to be made. Typical hole processing and plating follows. This technology was developed for surface mount board technology for military programs, where low CTE boards were needed to permit the use of leadless ceramic chip carriers. The low CTE requirement extends to the use of large flip chip and flip TAB die, where little or no stress compliance is built into the connection.

5.6 IC CONNECTION AND REPAIR: LAMINATE IMPLICATIONS

IC connection techniques have great influence in the selection process of the laminate technology. The common connection methods are wire bonding (WB), tape automated bonding (TAB) and flip chip (solder bumped die connections). Each of the bonding processes requires a set of joining process specifications and board specifications. The chip joining processes are described in detail in Chapter 9. The joining process specifications designate the temperature, time, pressure, atmosphere, and chemical exposure to which the die and the MCM-L substrate are exposed during and after the joining process. The board specifications must meet the requirements of the joining process, including the minimum line width and spacing for the surface contact pads, the glass transition temperature of the board (or more specifically, the board properties at the joining temperature), the maximum temperature exposure the board can tolerate, chemical durability and metallurgical compatibility with the joining materials. Many MCM-L applications require that the module system be repairable, which involves separation of the die's electrical connections, die removal, die bond pad preparation, die attach site preparation, die reattachment and the rebond of the

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I/O connections. The joining process and rework procedures subject the module to considerable thermal, mechanical and chemical abuse. The substrate and the surface contact pads must withstand this treatment without structural degradation or without reduction of surface metal adhesion.

5.6.1 Wire Bonding to MCM-L Substrates

Both aluminum and gold wires are used to connect die to MCM-L substrates. Gold wires are used in most consumer electronic chip-on-board MCM-L applications, where nonhermetic, glob-top encapsulation is widely practiced. In both cases, the deposition of a barrier layer of 5 µm of low stress Ni over the copper conductors is recommended. The final plating is typically a soft 99.99+% purity electrolytic gold film, measuring 0.5 - 0.75 µm in thickness. Some wire bonding to electroless Au plating with a thickness of approximately 0.25 µm is underway in Japan.

The pressure to reduce the cost of electronics is causing an increase in the use of lower cost FR-4 boards for Al wire bonded MCM-L applications. FR-4 materials are well suited to Al wedge bonding since the required bonding temperatures are << 100°C. The level of leachable ionics in glob-top materials has been greatly reduced in the past few years, largely eliminating the major cause of reliability concerns with the use of aluminum wires with glop-topping. Gold wire bonding requires a temperature of approximately 150°C, which is higher than the T_g of FR-4 (~125°C); therefore, reliability concerns often preclude the use of FR-4 for Au wire bonded die. If the wire bond count is high, the substrate needs to be held at the wire bond temperature for several minutes (assuming a bond rate of 2 to 8 wires per minute). At temperatures greater than the board T_g, the polymer matrix softens and the board undergoes an increase in thermal expansion. In this softened state, the board material can transfer the bond pressure from the bond point into the surrounding material via viscoelastic deformation of the underlying material. This can degrade the adhesion of the bond pad to the MCM-L dielectric material. The ultrasonic energy applied to the bond point also is attenuated quite readily above the T_g. This is due to the significant reduction in elastic modulus which occurs above the T_g. The likely result is inadequate bond strength and degradation of the bond pad to board adhesion. Therefore, a substrate material with a T_g greater than the necessary Au bonding temperature is desirable. Wire bonding processes are covered in detail in Section 9.3.

Module rework is another major consideration. The substrate, assembly process and materials must be selected to permit the removal of defective die. The use of a reworkable die attach adhesive is required. If a module test

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indicates a defective die, the wires are pulled or cut by hand under a microscope, and the die is removed at temperatures high enough to soften the adhesive. The reattachment and rebonding of die require that the substrate structure be strong enough to withstand the necessary processes. The bond pad adhesion must not be degraded by the repair processes. The bond pads also must be designed large enough to permit one or more reworks, since it may be impossible to achieve a good bond on the same site from which a wire was removed. Some very low T_g epoxies and thermoplastic materials do not need much site rework since they soften so well with applied heat.

5.6.2 TAB Bonding on MCM-L Substrates

Tape bonded die can be attached to a substrate using either thermodes (solder reflow or conductive adhesives) or single point bonding. Au to Au single point bonding is most common, but single point solder reflow can be performed at a much slower bond rate. A challenge for MCM-L is the etching of the fine bond pads often required, especially for in-line TAB (no fanout from the die to the bond pad). MCM-L boards with TAB bond pad pitches of 100 µm are available. TAB bonding is discussed in detail in Section 9.4.

Other MCM-L challenges involve the stresses the TAB outer lead bonding (OLB) process exerts on the bond pads. In this process, the substrate is heated to 100° - 200°C, the hot thermode (> 250°C) presses on each lead. Also, potentially corrosive fluxes are used, the residues of which usually are cleaned away. Improper board materials and OLB processes can induce mechanical and thermal stresses which can char the board, induce internal delamination or weaken bond pad adhesion. The rework of a TAB site also is a relatively complex issue. If the die back (or the die face in the case of flip TAB connections) is bonded adhesively to the substrate, this adhesive must be softened simultaneously with solder at the OLB sites. At this point, the die and the TAB leadframe are pulled from the PWB. The bond sites often are cleaned of residual solder, especially if the bond pad surfaces are rough or if Au content in the solder exceeds 3 - 4%. It also may be required to add solder to the pads before a replacement die is bonded. The die attach site is prepared as previously described.

5.6.3 Flip Chip Bonding on MCM-L Substrates

Flip chip bonding classically has taken the form defined by IBM, wherein a refractory lead-tin solder (historically 95/5, but other metallurgies are used) is used to bump the die. The bumped die are connected to ceramic substrates at temperatures exceeding 300°C. With MCM-L, this connection process is not possible because of the high temperatures. An alternative process is required,

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which permits joining at a temperature suited to organic boards. The general flip chip process is discussed in detail in Sections 9.5 and 9.6.

The process being pursued by Motorola and IBM involves surface preparation of the MCM-L which allows a lower temperature Pb/Sn solder join between the substrate and the die bumps, allowing the use of FR-4 modules. To reduce the incidence of temperature cycling-induced failures in a flip chip connection, the gap between the die face and the substrate is filled with a specially formulated polymeric material. This material becomes the major load bearing member, leading to a significant enhancement in temperature cycling life. Rework and die replacement can be done only prior to performing the underfill. This process is referred to as direct chip attach [23]. There are numerous other means to bump die and to achieve an connection to MCM-L. Sections 9.5 and 9.6 provide more information.

5.7 VERSIONS OF ASSEMBLED MCM-L SYSTEMS

MCM-L assemblies take many forms. In previous sections, the wide variety of substrates was discussed. In this section, some of the possible MCM-L configurations are presented. Several of these forms are generically unique to MCM-L technology, while others are formed with any MCM technology. The forms contrast mainly in the details of I/O configuration (edge versus area), the die sealing and lidding approach, type(s) of die connection technologies used and single or dual sided assembly.

5.7.1 Substrate I/O Configurations

Perimeter I/O

Perimeter lead configurations are discussed in Chapter 9. MCM-L uses several methods of perimeter lead configurations. In its simplest form, the lead frame can be soldered to surface pads, similar to brazed MCM-C assemblies. If the MCM-L substrate perimeter is defined by a cut through a row of PTHs, which connect to the bond pads, added lead adhesion strength can be achieved by solder fillet wetting of both the underside of the lead and the sidewall of the sectioned PTH. This is common practice for leaded, fine pitch, cofired ceramic packages.

Figure 5-3 is a prototype MCM-L from Motorola exemplifying this type of lead frame attachment. It consists of a 32 mm sq. BT glass substrate with 100 I/Os on 0.8 mm pitch, a back side bonded lead frame heat spreader, one digital signal processor (DSP) die, three fast static random access memories (FSRAMs), a number of resistors and capacitors, black glob-top encapsulant and a white

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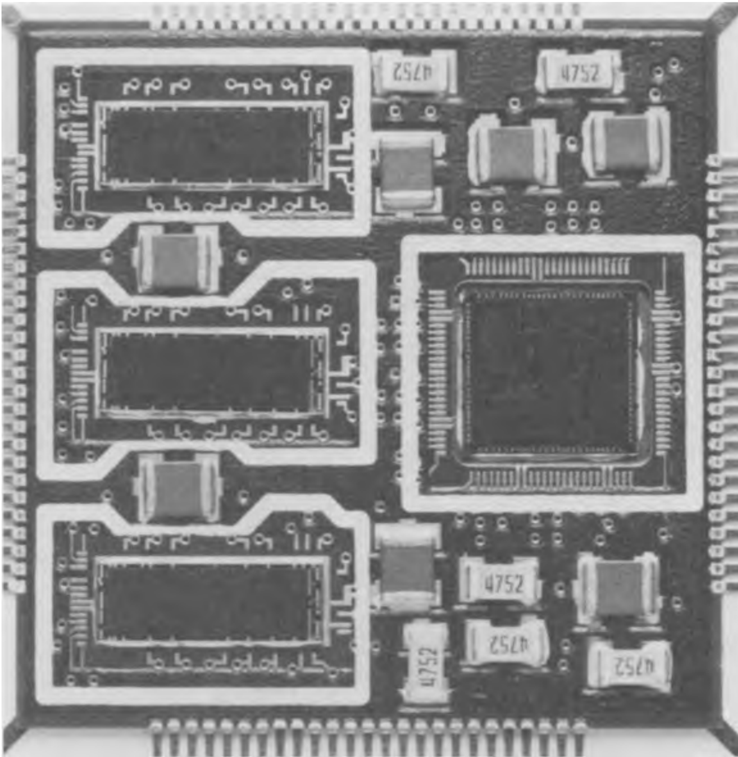

Figure 5-3 Prototype DSP/FSRAM module. Features: four conductor planes, BT glass dielectric, $Z_0 = 60\ \Omega$, 40 MHz operation, 100 I.O, 0.8 mm pitch, glob-topped. (Courtesy of Motorola.)

epoxy flow dam. Glob-top encapsulation provides good mechanical and environmental protection for the die, but the specific requirements are not well defined. The thermal expansion, modulus of elasticity, moisture permeability, extractable ion content and wettability and adhesion of the encapsulant to all wetted materials must be carefully evaluated for each material system.

The square DSP die is attached through an opening in the substrate, directly onto the copper heat spreader. The FSRAMs are attached to the substrate surface, on top of PTHs functioning as thermal vias to the heat spreader. Au

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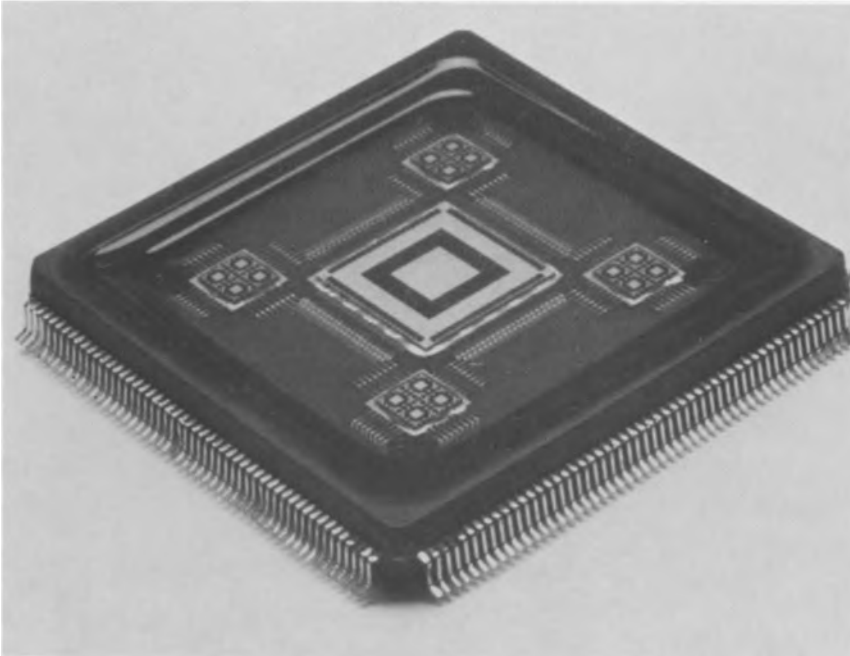

Figure 5-4 Module with molded perimeter. Features: Standard PQFP footprint, silicone elastomer encapsulation, high temperature lead-to-PWB connections, 0.65 mm pitch. (Courtesy of Matsushita.)

plated leads are excised and formed into a gull-wing shape, permitting die down assembly to a board and heat sinking away from the board.

Lead adhesion may not be adequate with this type of lead frame attachment. Matsushita Corp. molds a frame around the perimeter of a similar substrate, effectively encapsulating the board perimeter and the bond pad region (see Figure 5-4). Due to the temperatures involved in transfer molding, eutectic Pb/Sn solder joining is not used, and a joining operation with higher temperature stability is practiced. Hestia Technology, Inc. uses an adhesive to bond a preformed frame to the substrate with perimeter soldered leadframes, embedding the leads between the substrate and the frame. In other instances, a high rheology adhesive material is dispensed along the edge of the substrate, covering the ends of the leads and the bond pads, effectively encapsulating the lead tips. A version of this method was used on the Motorola MCM-L shown in Figure 5-3. In all cases, these molded, preformed and dispensed frames also act as dams to

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constrain the flow of material used to coat or pot the substrate components, if the frames are formed on the die side of the substrate. These frames also can act as a base against which lids to the MCM-L are attached. The attached die may be sealed by several methods, including potting with silicone gel (as done with the Matsushita module in Figure 5-4), using epoxy or silicone elastomer attachment of a lid, glob-topping with an epoxy compound, lid sealing without an encapsulant, transfer molding of the die side surface (overmolding) or full transfer molding of the entire substrate.

Ibiden Corp. uses a configuration in which the leadframe is laminated directly into the MCM-L substrate. Ibiden calls this substrate technology PACKTHOL™. Die attach cavities are formed in the top and/or bottom portions of the substrate, exposing the copper leadframe plane as the cavity floor. These cavity floor segments can be electrically connected and share common connections with other cavity floor segments. In other instances, the cavity floor is contiguous with several 150 - 200 μm leads, acting as heat pipes, which connect the die to the substrate solder joints. In Figure 5-8, the die attach floor is the opposing surface of the back side copper heat spreader. The presence of the cavities significantly reduces the circuit routing capacity of the substrate. This configuration is not likely to provide a high interconnect density. The die are sealed typically with glob-topping or transfer molding of the substrate. Transfer molding of the substrate provides level of reliability similar to a standard molded quad flat pack (PQFP).

The I/O provided by perimeter leadframes does not provide adequate I/O for small, high I/O density modules. In these cases, very fine pitch flex circuits are used to provide connection between the MCM-L substrate and the board. IBM uses similar flex circuits with their experimental RS-6000 workstation and PS-2 computer modules, which are MCM-D based [24]. This type of flex connection also is used in the Digital Equipment Corp. VAX-9000 MCM-D module.

MCC developed an MCM utilizing both TAB and wire bonding on a single substrate with approximately 1700 internal interconnection nets. The TAB assembly pads are on pitches as fine as 100 μm. The TAB pads are solder plated and the wire bond sites are gold plated. The substrate is designed to be connected to the next level through the use of a perimeter pad connector. The substrate is built with both MCM-D and MCM-L technologies. Both substrate types achieve the same xy-dimensions. The MCM-D substrates are built with five metal layers. The MCM-L substrates eight metal layers and built with 3 mil line and space design rules. The MCM-L substrates are made by Assist Inc. and Diceon Inc., and were priced at levels substantially less than their MCM-D counterparts [25]. This MCM-L is shown in Figure 5-5.

Another very high performance MCM-L, made by Litronics Corp., is shown in Figure 5-6. This module uses TAB for all the die connections. The substrate

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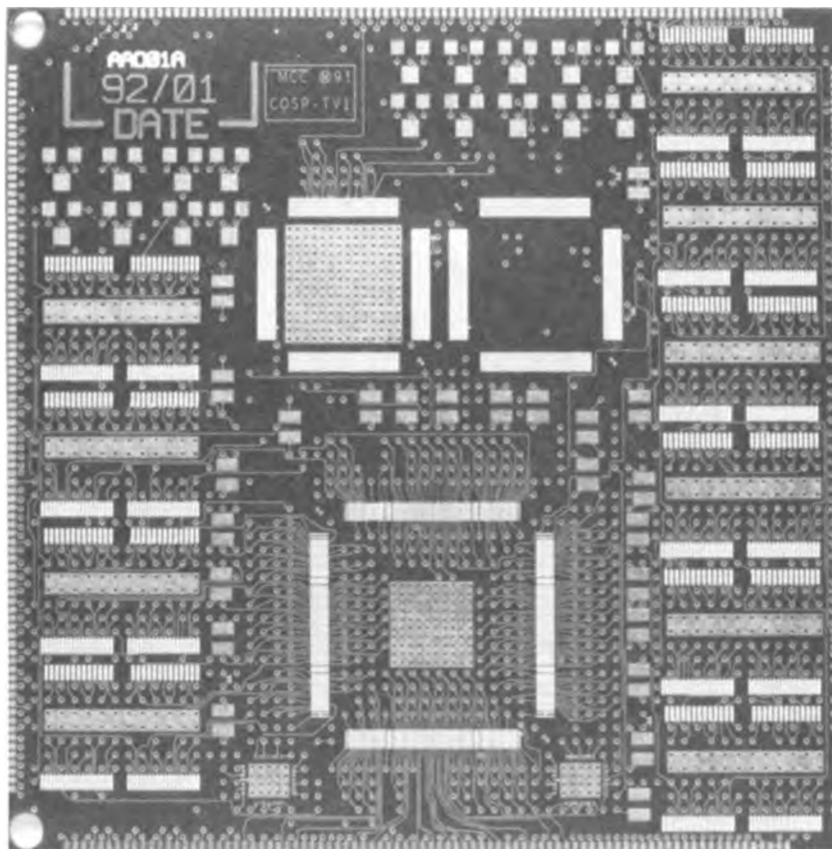

Figure 5-5 Microelectronics and Computer Technology Corporation (MCC) designed MCM for evaluation of a two processor RISC chip set. Features: 2.5" × 2.5", eight copper planes, 10 mil vias on 40 mil grid, 3 mil lines and spaces internal, 2 mil lines and spaces on bond surface, $Z_0 = 50\ \Omega$, > 65 MHz operation, selective plated Au and Pb/Sn surface, TAB reflow and Au wire bond assembly. (Courtesy of MCC.)

is designed to interconnect with a stack of other similar modules to create a super computer functionality in less than a one liter volume. The stack utilizes Cinch Corp. fuzz button connectors (as discussed in Chapter 10) to connect the substrates.

The lead frame or flex circuits, described above, add significant cost to the MCM-L substrate. The use of a socket also adds considerable cost to the system. For the lowest cost applications, it is desirable to eliminate the lead

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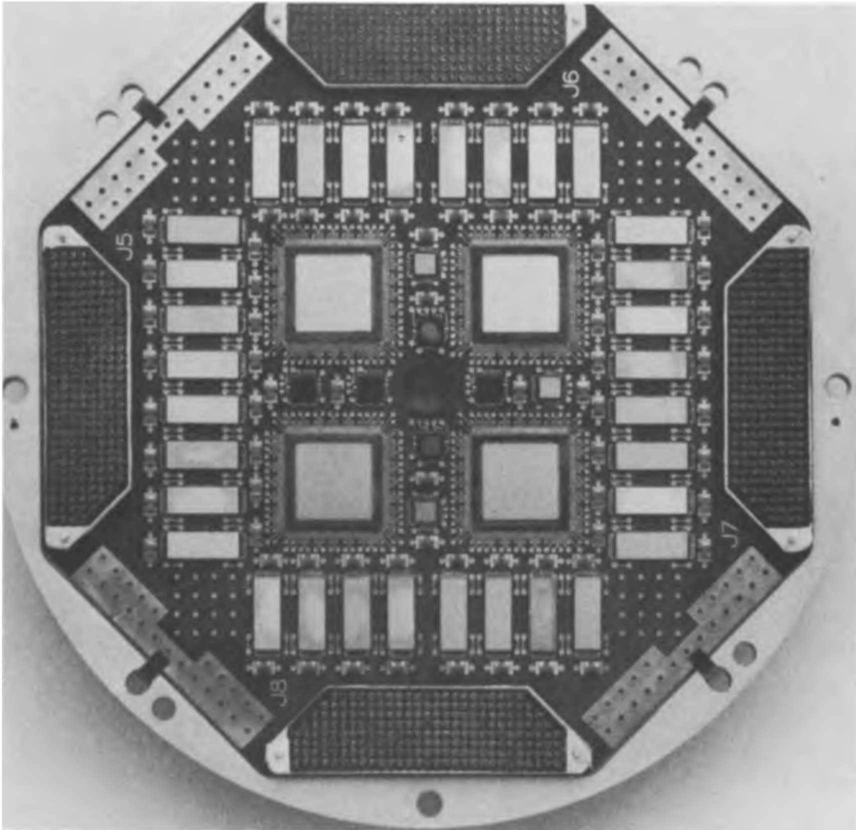

Figure 5-6 Single board element of a massively parallel computer. Features: 10 copper planes, polyimide/glass, approximately 3.5" diameter board, three sets of dual stripline signal pairs, 3 mil lines and spaces, buried 8 mil vias, 12 mil plated through-holes, approximately 4000 layer holes, over 1600 nets, all single point Au/Au TAB bonding. (Courtesy of Litronic Industries Incorporated.)

frame or flex. A form of MCM-L which uses perimeter pads, much like those of leadless ceramic chip carriers, is gaining widespread popularity in Japan. This configuration is appropriate for relatively small MCM-Ls, with few die (~≤ 6) and a low interconnect density, where a two sided substrate (two metal layers), or multilayer board, can be employed for the interconnection. The I/O pads usually are arranged in a single row at the perimeter of the substrate area array I/O pads. Forming a land grid array is also quite feasible. They are connected directly to bottom or top side interconnect nets, with PTHs or with perimeter

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castellations. The castellations are PTHs bisected by the action of cutting the substrate free from a multi-up panel of parts. The electrical integrity from the top side net to the bottom side pad is maintained after the cutout process. This type of surface mount technology (SMT) MCM-L is soldered, or attached with conductive adhesion, directly to the motherboard. Since the MCM-L substrate and the motherboard usually are made of the same material (FR-4, BT resin/glass etc.), the thermal expansion mismatch between the substrate and the motherboard is minimal. There is a thermal resistance imposed by the air gap between the MCM-L substrate and the motherboard, but for low power modules the temperature difference is small. If a thermally conductive underfill adhesive is applied between the substrate and the motherboard, the thermal stress between the two assembled elements is reduced further and the under fill acts the primary stress bearing member, reducing the stress on the solder joints. This type of substrate is likely to see great use as a vehicle for a few-chips-module (FCM), where the interconnect density is likely to be low enough for the use of a two sided, or a 3 - 4 layer substrate. As mentioned previously, the FCM arbitrarily is defined as a substrate interconnecting a small number of die (~≤ 4 - 6), where the number of die to die connections is less than the number of module I/O [26].

Area Array I/O

MCM-L offers the option of area array I/O (discussed in Chapter 9), which take the form of pins, pads or solder bumps. These I/O contacts usually are dispersed in an array about the bottom side of the substrate. If it is desired to mount the die on the same side of the substrate as the I/Os, then the bond pads must be allocated into rows and columns to leave space for component attach. Figure 5-7 shows a substrate, made by Eastern Electronic Components used in Epson portable computers for graphics control. The substrate uses a connector soldered on two edges of the substrate for connection to the next level. The connector headers are comprised of two rows of pins in a molded plastic bar, forming a type of a perimeter pin grid array (PGA) I/O [27].

Figure 5-8 shows an MCM-L substrate, made by Ibiden Corp. incorporating mixed connection technologies. Three sites for the attachment of wire bonded die are in the central portion of the substrates. The two centermost sites have the PWB material routed out to allow direct die attach to heatsinks attached with adhesive to the back of the module. The third wire bond site permits die attach directly to the PWB surface, where four thermal vias (PTHs plated with thick copper) are formed to reduce thermal resistance through the board. The presence of the routed openings and the thermal vias reduces board routing efficiency. In cases where routing requirements are very dense, this reduced efficiency forces the addition of more layers to the stackup. The presence of routed openings and dense fields of thermal vias also can cause the average

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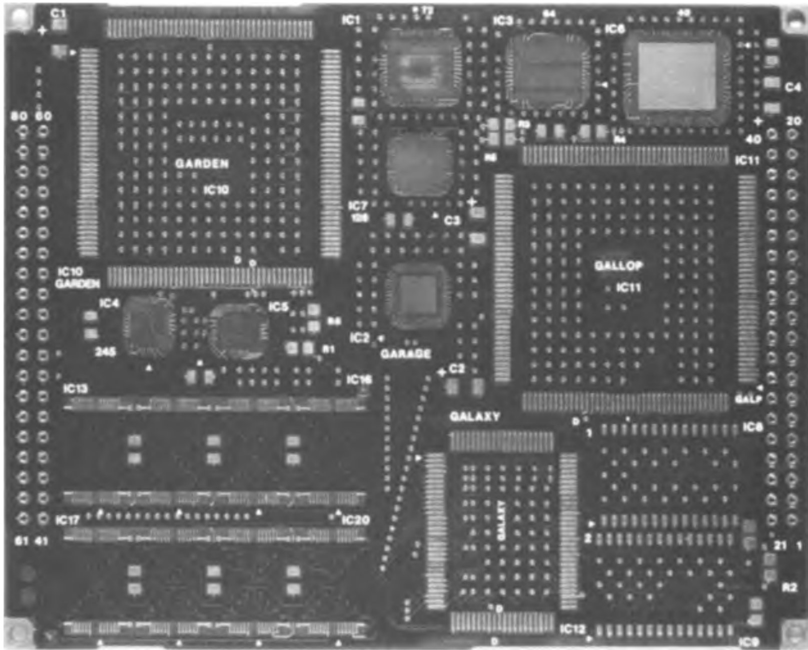

Figure 5-7 Graphics controller MCM from a Seiko/Epson portable computer. Features: selective plated Au and Pb/Sn for TAB and wire bond assembly, glob-top encapsulation, perimeter pinned headers used for I/O. (Courtesy of Eastern Electronic Components Ltd.)

length of the MCM-L nets to increase. This increases signal parasitics and propagation delay, possibly reducing high speed system performance.

The remaining components are packaged surface mount devices. Footprints for three PLCCs can be seen across the top, and in the lower third of the substrate footprints for two SOJ packages also are shown. The opposite side of the substrate supports six other SMT devices. Finally, the module I/O is provided by an array of PTHs along the bottom edge, permitting the insertion of a through-hole connector.

The I/O array in Figure 5-8 populates only one edge of the package. Figure 5-9 shows a Hestia Technologies, Inc. PGA MCM-L made with a polyimide/glass substrate. This particular substrate has no I/O pins in the center of the bottom side, but some other PGAs have fully populated arrays. The I/O arrays also can take the form of pads or solder spheres. I/O arrays can

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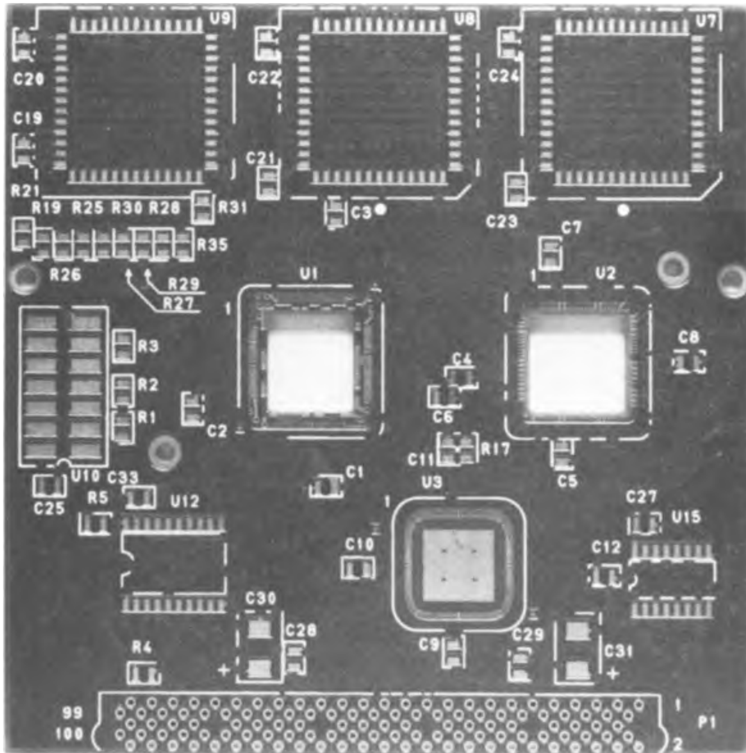

Figure 5-8 RISC microprocessor system module. Features: routed windows for back side heatsink attachment, wire bonding and SMT, perimeter pinner connector for I/O. (Courtesy of Ibiden Inc.)

be connected to the next level using solder, adhesives or connectors. Connection to motherboards is discussed in detail in Chapter 10.

Motorola Inc. has used solder ball I/O on near die size packages for several years. They are developing a new type of solder ball I/O package called an OMPAC (overmolded pad array carrier). This type of solder ball package connection is called Controlled Collapse Chip Carrier Connection (C5). OMPACs have been discussed as single and multichip packages. The OMPAC is made from a BT glass substrate, with bottom side solder balls attached

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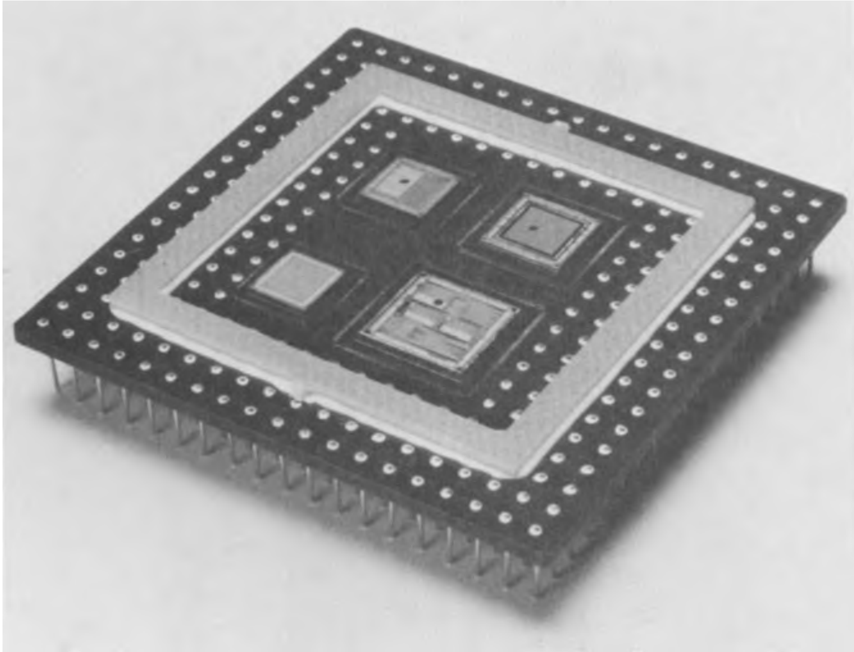

Figure 5-9 Pin grid array MCM. Features: Polyimide/glass structure, bottom side chip capacitor attachment orientation, use of a surface ring for encapsulant containment, metal lid. (Courtesy of Hestia Technologies, Inc.)

typically on a 0.040" - 0.060" pitch. After device attach, the substrate is overmolded (transfer molding only on the die side of the package), but alternative sealing processes, such as glob-topping or lidding can be used [28].

Overmolding has been used for other types of MCM-L. Figure 5-10 shows an overmolded module, from Citizen Corp. which interconnects four static random access memories (SRAMs). The mold compound encapsulates the die-side surface, while maintaining interconnect access to the back surface. In this case, the module I/O takes the form of a row of surface mount contact pads along a single edge. The memory module is based upon a very thin, two sided board, providing a very low profile and mass.

Dual Sided MCM-L Assembly

One of the advantages of MCM-L is the ability to use both substrate surfaces for

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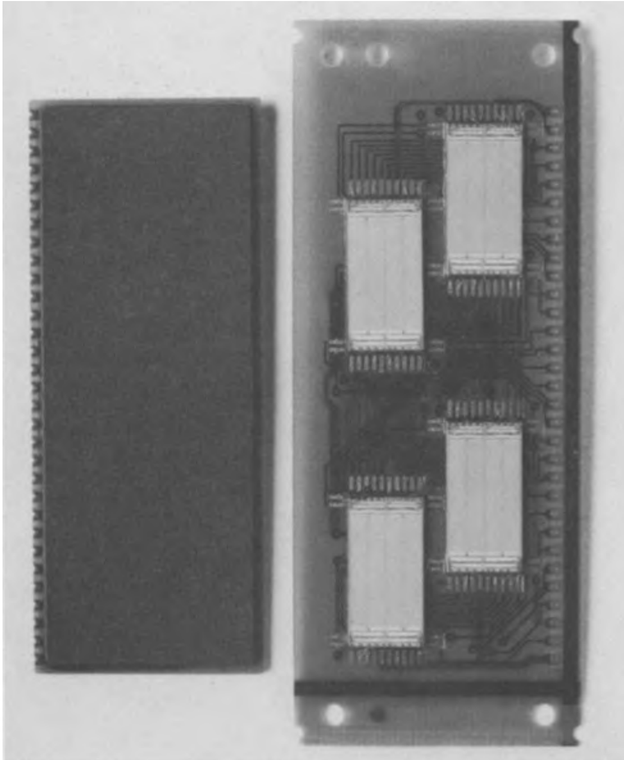

Figure 5-10 Overmolded SRAM module: Use of two-sided board, SIMM-type I/O format of a row of pads on one edge for use with surface attachment, low profile molding. (Courtesy of Citizen, Inc.)

device connections. There have been instances of PWB and ceramic substrate assembly where both surfaces are utilized, but in almost all cases, the devices are packaged. The MCM design must be configured very carefully to allow use of both sides of the substrate, since the substrate under the site of a die connection may need to be supported mechanically during assembly or provide for heat dissipation while in use. Similar access will be needed to effect repairs to the module in most cases. This dual surface assembly is not usually an option with MCM-D. Silicon substrates with through vias allowing circuit buildup on both surfaces have not been reported to date. In theory, a cofired multilayer ceramic base, containing internal circuitry, could permit the development of thin film interconnections on one surface, while permitting the connection of parts to gold

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or solder plated pads on the opposite ceramic module surface. If a high density laminate is used as the base for final construction of thin film interconnection circuitry on the top surface, it might be possible to connect bare die on the bottom of the laminate base. The use of both module surfaces implies a perimeter module I/O configuration. Area array I/O, from a field of die which require cooling, may be very difficult to achieve in a product.

Thermal management of any dual sided assembly module may be more complicated. Unless excellent lateral heat spreading is built into the substrate by virtue of the materials used, it may be impossible to cool the bottom side components for a planar mounting on a motherboard. Provisions for heatsinking into the motherboard, or for the insertion of heat pipes between the die and the motherboard, can be implemented, but the series thermal resistance, the complexity, the board area demand, and the cost may preclude this possibility.

If it is not possible to dissipate module heat from the MCM substrate, then heat must be removed directly from the die surface. This is facilitated most readily when the connection method permits die back contact (flip chip or flip TAB), but it also may be accomplished by contact to the junction surface of the wire bonded die. In all three modes of connection, the lid and heatsink(s) must make adhesive and mechanical contact with the back side, or face, of the die. Dual surface MCM-L may be applied in designs where modules are stacked in the z-direction, permitting air to be ducted through the stack, cooling both surfaces simultaneously. Another design where dual surface modules have promise is the SIMM (Single In-line Memory Module) configuration. (See Chapter 10 for a description of the SIMM connection design.) The distinguishing characteristic of SIMM is that all of the module I/O are on one edge, on one or both sides of the module. This type of MCM mounts perpendicular to a motherboard, typically with a socket. A similar ducted and directed air thermal management solution is appropriate here. A schematic of a dual surface MCM-L with flip chip assembly is shown in Figure 5-11.

5.8 MCM-L SYSTEM EXTENDABILITY AND COST ISSUES

The cost of an MCM substrate, for any material technology, is controlled by the yield of good functional product. Due to the complexity of manufacture, a 99% yield from a 40 to 50 step process results in low product yield, increasing costs (as discussed in Chapter 3). The manufacturing base for PWBs is very broad and competition is high, forcing competitive pricing. The base of manufacturers willing to build PWBs with the characteristics necessary for MCM-L is fairly limited at this time, but is growing. Therefore, the pricing for MCM-L substrates continues to be quite reasonable when compared with other MCM technologies.

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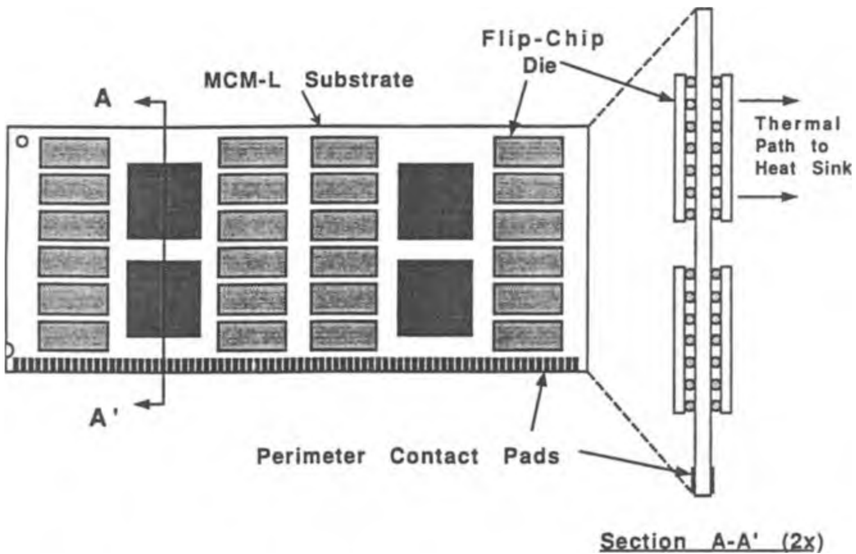

Figure 5-11 Schematic of dual surface MCM-L assembly. Features: SIMM I/O, dual surface assembly, flip chip assembly.

The choice of dielectric material has the greatest effect on the material cost of the substrates. If the MCM-L substrate is made from standard FR-4 material, it is much less expensive than if it were made of polyimide/aramid fabric. However, as the cost of the substrate usually is much less than the cost of mounted chips often it does not make sense to cut corners on substrate material in an effort to minimize expense. The higher price materials may offer higher reliability due to their higher glass transition temperatures (lower CTE in the use temperature range, less copper feature adhesion degradation during high temperature assembly operations etc.). Conversely, it is folly to use a much higher performance board than is needed for an application.

The cost drivers for MCM-L substrates [29] are:

- High layer count
- Small drill diameter
- Tight characteristic impedance tolerance specifications
- Narrow etched feature widths and spacings
- High number of drilled holes

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- Nonstandard material selection (composition, thicknesses)
- Plating complexity: more than one metal finish on the surfaces
- Tight thickness specifications
- High plated through hole aspect ratio
- Use of blind and buried vias
- The incorporation of leadframes

High layer count requirements result in a considerable reduction in yield. One approach to solve this problem is the testing of inner layers and inner layer sublaminates prior to committing them to final lamination. Of course, the cost of testing must be balanced against the yield benefit. DEC utilized a version of this approach with the MCM-D used in the VAX-9000 (see Chapter 17).

In some analyses comparing PWB and MCM-D technologies it often is assumed that the former remains static while the latter will grow. Thus, there is some crossover point where MCM-D becomes cost competitive. While it appears that thin film interconnections offer the greatest density (≤ 25 μm feature sizes are now available), it is unclear where the cost crossover point with MCM-L actually occurs. It also is possible that thin film conductor processing may become common on dielectric layers prior to lamination (inner layer construction), or on the surface of a completed base laminate for fanout purposes. It is unclear which arbitrary MCM technology designation would be applied to this type of structure. MCM-L fabricators will continue to improve their technologies and experience economies of scale as the MCM industry accelerates. Therefore, the costs of both technologies should continue to fall in the near future. Since many high volume MCM applications do not require the interconnection density of MCM-D or MCM-C or the hermetic characteristics of MCM-C, it is likely that the demand for classical and emerging MCM-L substrates and assemblies will be quite high over the next several years. This may offer the MCM-L fabricators the opportunity to ride the economy of scale curve before the MCM-D vendors. Initially, this may widen the price disparity between the two technologies.

It also appears that the blending of MCM-L and MCM-D technologies will create a set of substrate technologies which satisfies the very high end of MCM-L applications and the low-to-high end of projected MCM-D applications. This may create a cost arena not currently anticipated by market forecasts, where this hybrid MCM-L/D will even satisfy very high end applications.

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6

THICK FILM AND CERAMIC TECHNOLOGIES FOR HYBRID MULTICHIP MODULES

William A. Vitriol

6.1 INTRODUCTION

Ceramic based multichip modules (MCMs) have been used in the electronics industry for over 20 years; however, the term MCM-C has become popular only in the last few years. For the purpose of this chapter, ceramic MCMs are considered as sophisticated extensions of simple hybrid circuits in which bare chips are mounted on substrates and interconnected using screen printed conductor materials. Three ceramic based technologies are used to make the various microelectronic circuits that are considered MCM-C structures. They are thick film multilayer (TFM), high temperature cofired ceramic (HTCC), and low temperature cofired ceramic (LTCC) MCM-C technologies. In fact, standard TFM hybrid circuits may be the oldest type of MCM-C.

6.1.1 Definitions of MCM-C Technologies

Thick Film Technology

Thick film is a technology in which specially developed pastes (also referred to as inks) are deposited and patterned by screen printing onto a ceramic substrate. The paste can be formulated to produce any number of different passive electrical components such as conductors, resistors, inductors and capacitors.

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The pastes are applied by a screen printing process. After printing, the pastes are dried at temperatures of 85°C - 150°C to remove low boiling point solvents and then fired at temperatures ranging from 400°C - 1000°C. The substrate in the thick film-based technology is a passive inorganic material used to provide a mechanical platform for the thick film circuit. Typically substrates are made from 96% alumina. For MCM applications multilayer circuits are generally used instead of single layer circuits because of greater density requirements. Figure 6-1 shows an exploded view of a fabrication sequence for a single layer of a TFM circuit. The first conductor layer is printed, dried and fired on the substrate. Next, the dielectric (or insulating) layers are printed, dried and fired. Depending on the materials and complexity of the circuit as many as four dielectric layers may be processed before the next conductor layer. After the dielectric is fired the vias (vertical conductors that provide electrical connection between dielectric layers) are filled, dried and fired. This sequence of operations is repeated until the complete multilayer circuit is produced.

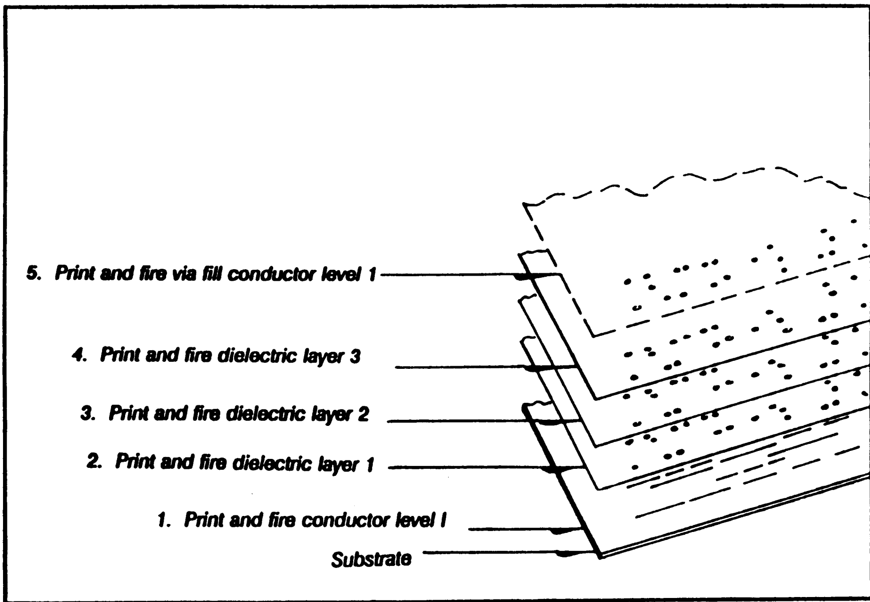

Figure 6-1 Exploded view of a fabrication sequence for single level of a thick film multilayer.

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High Temperature Cofired Ceramic (HTCC) Technology

Cofired multilayer ceramic technologies have been developed to improve packaging densities by increasing circuit density, reducing the number of interconnects and by shortening conductor lengths. The building blocks for cofired ceramic structures are green (unfired) sheets of dielectric tape formed from a slurry of alumina powder, small amounts of glass and various organic components using a fabrication process called doctor blading. Doctor blading is a method of forming the slurry into a thin sheet by the use of a knife blade placed over a moving carrier to control slurry thickness. The dried, "green tapes" formed from the slurry, are usually 0.010" thick and have the consistency of fresh unchewed chewing gum!

Vias, or holes, then are formed in each individual sheet of tape. These vias are filled with a specially formulated conductive material to make electrical connection between metal layers. Each sheet then is patterned with a conductor material using screen printing techniques. After all the required sheets of alumina dielectric have been processed, they are stacked, aligned and laminated together using temperature and pressure. Figure 6-2 shows a drawing of the major steps involved in making a cofired part (both LTCC and HTCC). The finished product is formed by firing the laminated module at a high temperature, approximately 1600°C. At high temperatures only refractory metals such as tungsten (W) and molymanganese (Mo-Mn) can be used as conductors and they must be fired in a reducing (hydrogen) atmosphere to keep the conductors from oxidizing. The entire assembly shrinks approximately 17% in the x- and y-directions and 20% in the z-direction. Figure 6-3 shows an exploded view of the individual sheets of tape and is representative of either cofired technology.

Low Temperature Cofired Ceramic (LTCC) Technology

The conductor materials used to make high temperature cofired structures are limited by their low conductivity. Developments have sought to combine the advantages afforded by the cofired process (dielectric tape formation) with the advantages of standard thick film materials (use of metals with higher conductivity). For example, lowering the firing temperature of the dielectric tape to 850°C would make it possible to use thick film metals such as gold, silver and copper. These metals have a much higher conductivity than tungsten or molymanganese, allowing hybrid circuits to be made with faster processing speeds. The processing sequences using HTCC and LTCC technology are shown in Figures 6-4 and 6-5. The initial development in LTCC technology used a commercially available tape system from Dupont called Green Tape™.

Tape Transfer (TTRAN) is a variation of the LTCC process. It combines the serial processing of thick film technology with the use of dielectric tape. A single layer of cast tape replaces multiple screen printings of the thick film

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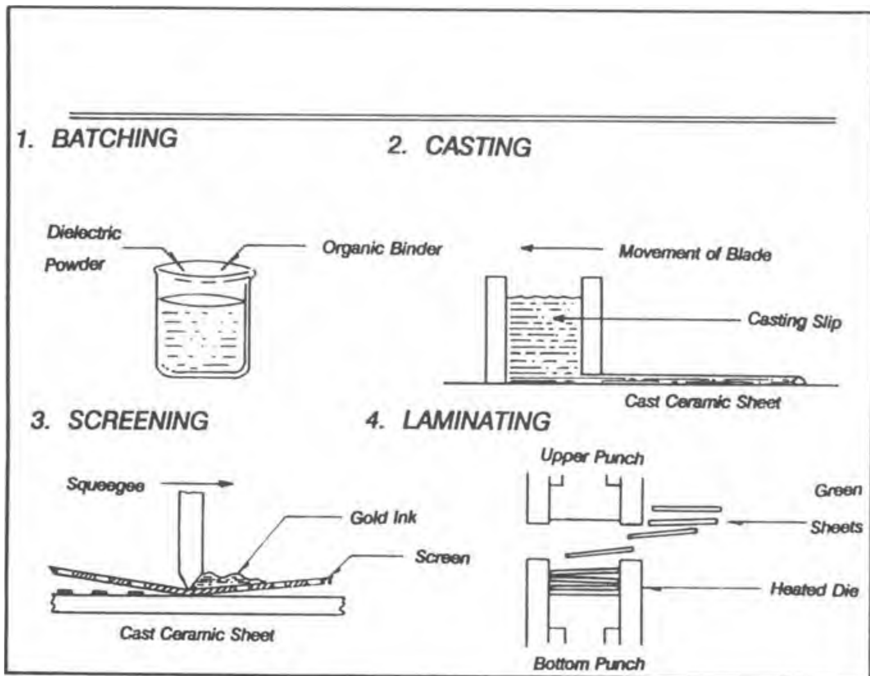

Figure 6-2 Cofired ceramic process steps.

dielectric layers in the TTRAN process [1]. Sheets of dielectric tape, with preformed vias, are registered and laminated to fired 96% alumina substrate at a fixed temperature and pressure. Since the tape adheres to the substrate it does not shrink in the x- or y- direction, but does shrink in the z-direction. Figure 6-6 compares the TTRAN process sequences to thick film processing for a single level of a multilayer circuit. Notice that fewer process steps are required when tape processing is used relative to thick film processing. It takes three or four individually printed and fired layers of thick film dielectric (15 μm - 25 μm thick per layer) to replace a single sheet of 3 mil (75 μm) thick tape laminated to a substrate and fired. The TTRAN process is lower cost and has higher yields relative to conventional TFM circuits [2]. Since it is fired on an alumina substrate, it exhibits superior mechanical and dimensional control compared to LTCC.

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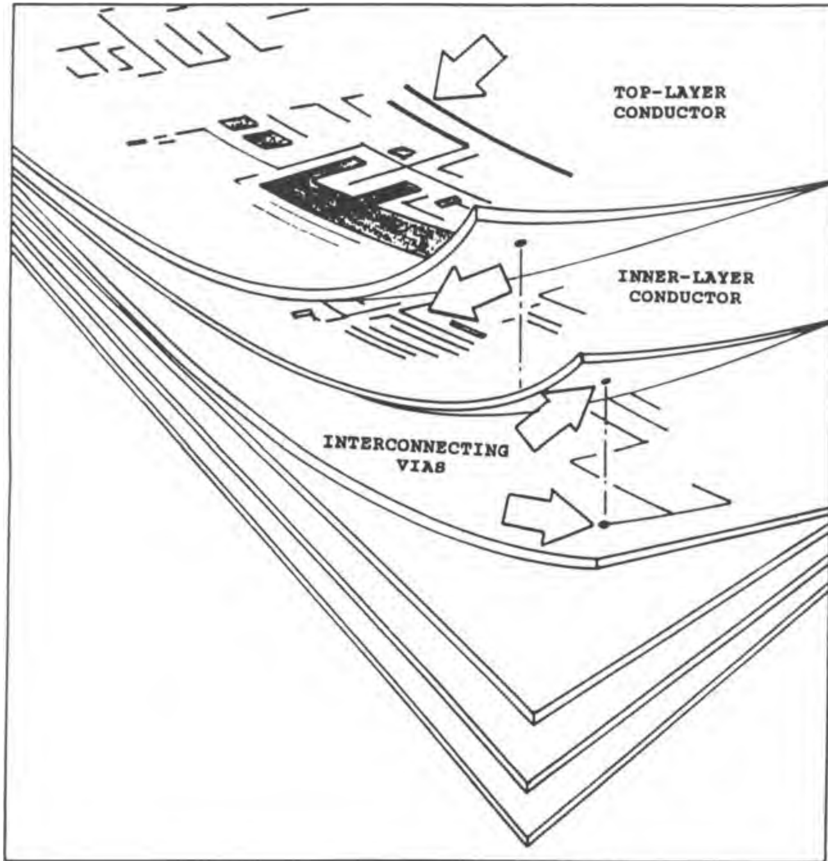

Figure 6-3 Exploded view of cofired ceramic structure.

6.1.2 General Comparison of MCM-C Technologies

The major difference between TFM MCMs and HTCC or LTCC MCMs, other than the fact that a substrate support platform is required for TFM circuits, is that thick film parts are processed serially, layer by layer. Each conductor level of a multilayer circuit may require as many as six printing steps and firing operations per level. This consists of three (sometimes four) individually printed and fired layers of dielectric, two via fills and the conductor. A similar structure

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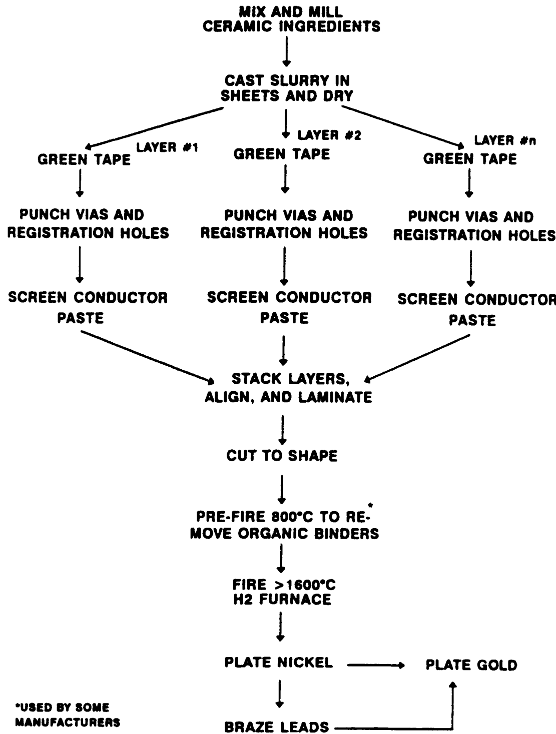

Figure 6-4 Process sequence for HTCCs.

using the cofired technology requires only a single step to fire all the laminated layers and then possibly three or four post firing process steps. The three technologies are described in Table 6-1.

In the cofired ceramic technologies, the substrate and the package form a single monolithic structure. The HTCC or LTCC package is usually sealed hermetically by attaching a metal lid to a metal seal ring which was previously soldered or brazed to the substrate. In contrast, surface mounted devices on TFM substrates are not hermetically sealed, so the substrate must be mounted into a package or the devices must be passivated in some other manner. Standard thick film sealing techniques can be used to attach the lid. Another possibility is to make an all ceramic package by forming a ceramic sidewall, integral to the package, during fabrication of the structure. Again, a metal lid can be attached to the ceramic sidewall to provide hermeticity. For high density applications, cavities can be manufactured in both the high and low temperature

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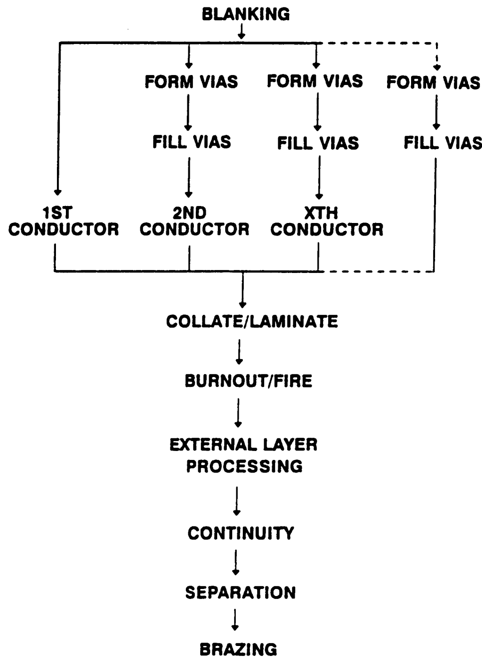

Figure 6-5 Process sequence for LTCCs.

ceramic structures to accommodate active and passive devices. When cavities are used, multiple bond shelves or ledges are used to fanout fine pitch bond fingers (pads) so that wire or tape automated bonds (TAB) can be made easily and reliably. Figure 6-7 shows a cofired package demonstrating multiple bond shelves. Tables 6-2a and 6-2b compare the three MCM-C technologies in terms of the technology options and the mechanical and electrical characteristics.

These tables show that LTCC MCM-Cs have a number of advantages over HTCC modules. One advantage is the use of high conductivity metals such as gold, silver or copper for the LTCC technology in place of the tungsten metal required for HTCC. Gold and silver do not oxidize to any great degree so they do not have to be plated to protect the metal. This is not the case when copper is used. Another big advantage of LTCC is that the basic ceramic substrate can be modified to provide any number of combinations of dielectric materials with different electrical and physical properties. For example, the dielectric constant can be varied between 4 and 400 and the coefficient of thermal expansion (CTE) can be designed to match silicon, gallium arsenide, or alumina. Finally, the same

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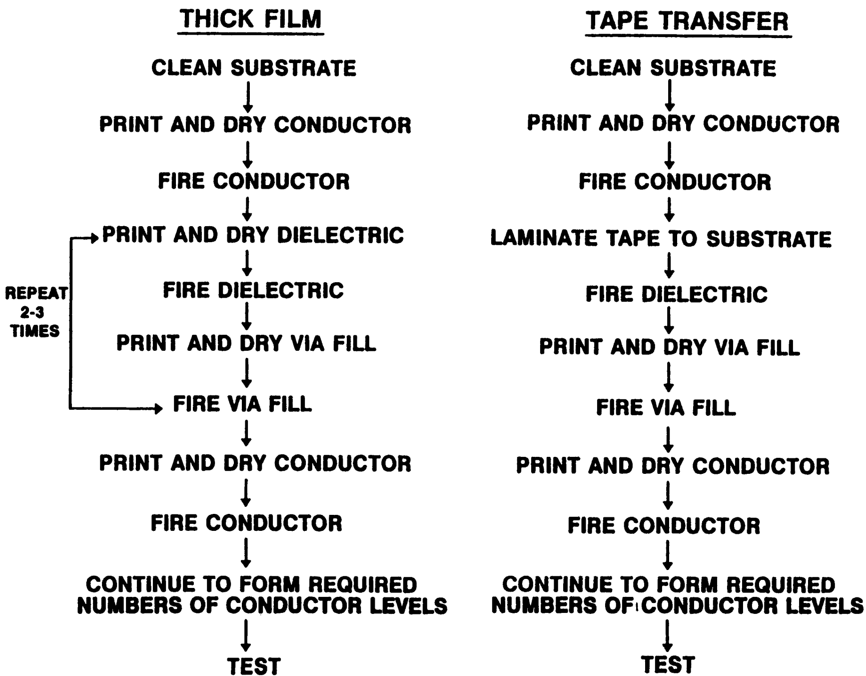

Figure 6-6 Fabrication process flow for thick film multilayer circuit: Comparison between thick film and tape transfer.

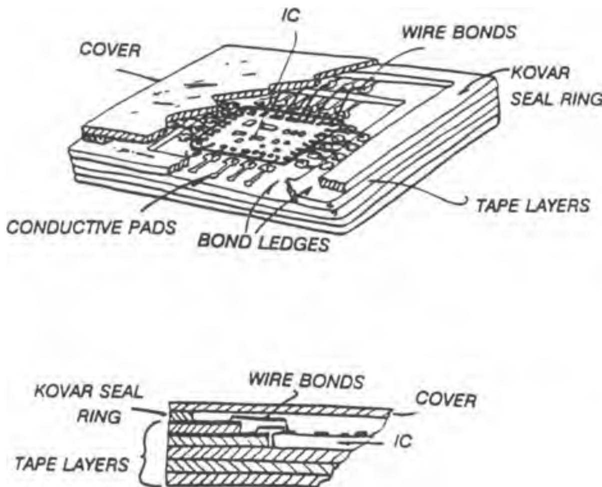

Figure 6-7 MCM-C package demonstrating the use of multiple bonding ledges.

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Table 6-1 Comparison of Characteristic Differences of MCM-C Technologies.

MULTILAYER THICK FILM	LTCC	HTCC
• Requires a mechanical support base • Serial processing • 6 prints per layer (3 dielectric, 2 via fill, 1 conductor) • 60 sequential firing steps for up to 10 layers • Must protect devices	• Monolithic structure • Parallel processing • 2 prints per layer (1 via fill, 1 conductor) • 1 cofire step plus three postfire steps • Hermetic package	
	• Fires at 850°C • Uses standard thick film conductors—gold and silver • Fires in air • Standard thick film processing time • Tailorable dielectrics	• Fires at 1600°C • Requires refractory metals—tungsten and molymanganese • Fires in hydrogen • Long processing time to remove organics • Uses alumina dielectric

thick film resistor and capacitor materials developed for standard thick film circuits can be adapted to LTCC circuits. Both buried and surface resistors and capacitors have been designed into LTCC parts [3].

Tables 6-2a and 6-2b also show some advantages in the use of high temperature cofired MCMs. HTCC is a mature technology; its materials and processes are better understood. Also, alumina has a much higher mechanical strength than LTCC dielectric materials, making packages stronger and more durable. Finally, the thermal conductivity of alumina is almost 20 times higher than that of the basic LTCC dielectric materials.

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Table 6-2a Feature Benefit Matrix for Multilayer Thick Film, HTCC and LTCC: Technology Characteristics. (Ranking order; 1 = best.)

Feature	Thick Film	HTCC	LTCC	Benefits
1. Mature materials and processes	1	1	3	Higher yields
2. Shorter proof of design cycles	3	3	1	Faster response to design changes
3. Lower nonrecurring expense (NRE)	1	3	1	Lower prototype costs
4. High print resolution	3	2	1	High frequency application
5. Unlimited number of layers	3	1	1	Highest possible circuit density
6. Postfiring process	1	3	1	Conventional thick film material
7. Wide processing options	2	3	1	Greatest design flexibility
8. Brazing	N/A	1	2**	Network and package processes
9. Tight process controls	2	3	1	Improved overall yield
10. Accommodates chip wire and surface mount assembly	1	1	1	Design flexibility
11. Cavities	3	1	1	Multiple bonding shelves

** Low temperature braze.

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Table 6-2b Feature Benefit Matrix for Multilayer Thick Film, HTCC and LTCC: Mechanical and Electrical Characteristics. (Ranking order; 1 = best.)

Feature	Thick Film	HTCC	LTCC	Benefit
1. Camber	2	2	1	Improved wire bond assembly yield
2. Surface roughness	3	2	1	Better high frequency performance
3. Top layer dimensional stability	1	3	2	Improved wire bond, assembly yield stability
4. CTE matched to alumina or silicon	2**	3	1	Capability of assembly
5. Thermal conductivity	2	1	3***	Good thermal characteristics
6. Hermeticity	2	1	1	Development of packages
7. High conductivity metallization	1	3	1	Smaller line and space designs
8. Low K values	1	3	1	Improved high frequency performance
9. Excellent dielectric control	3	1	1	More consistent electrical performance
10. High mechanical strength	2	1	3	More rugged package

** Varies with substrate material.
*** Thermal via designs enhance thermal conductivity.

6.2 MATERIAL CONSIDERATIONS

6.2.1 Thick Film Technology

Substrates

A substrate is the base onto which all thick film circuits are printed. It provides mechanical support, electrical insulation and assists in dissipating heat. Substrates can be obtained in various shapes, sizes and thicknesses. The shape

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Table 6-3 Common Substrate Materials by Application.

SUBSTRATE TYPE	APPLICATION
Alumina	
99+%	Thick/thin film circuits Microwave integrated circuits
96% (glass)	Thick film single/multilayer circuits
85% - 94% (glass)	Refractory thick film/cofired circuits
40% - 60% (glass)	Thick film/LTCC
Beryllia	Thick/thin film power circuits
Aluminum Nitride	Thick/thin film power circuits Refractory thick film circuits

can be pressed and fired to meet a variety of configurations or laser scribed to size specification. Sizes may range from 1" × 0.33" up to 6" × 13" and from 0.010" - 0.060" thick. For special applications thicknesses as great as 0.125" can be made. Because of the variation in available sizes, circuits can be processed in a multiple-up format, scribed and singulated (separated) in subsequent operations to improve handling efficiencies. Substrates may be laser drilled to permit use of the other side of the substrate, with connections made using through-hole technology. Substrates and their applications typically are defined by the amount of glass contained in the ceramic body. For example, a 99+% alumina substrate is used for thin film circuits and for high frequency applications, while HTCC bodies range from 85 - 94% alumina, and LTCC formulations from 40 - 60% alumina. The majority of thick film circuits are printed on 96% alumina because it provides the best compromise of cost, strength, resistor stability and conductor adhesion. Table 6-3 summarizes commonly used substrate materials by their principal application. Table 6-4 lists the advantages and disadvantages of these same substrate types.

Most substrates used in the electronics industry are alumina; however several other ceramic materials have found limited application based on their specific material properties. Beryllia (BeO), one such material, has one of the highest thermal conductivities of any ceramic material and is used most widely for high power handling applications. A major consideration in using BeO is its toxicity. Special handling is required for its use in certain processing steps. Also, thick film materials specifically formulated to match the properties of the ceramic must be used, since adhesion promoters used with alumina do not work with BeO.

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Table 6-4 Advantages and Disadvantages of Substrates for Thick Film Circuits.

SUBSTRATE TYPE	ADVANTAGES	DISADVANTAGES
99+% Alumina	Low microwave loss High strength Good stability for resistors Good thermal conductivity No alkali migration—low loss Good surface finish	High cost Low conductor adhesion
96% Alumina	Lower cost High strength Good stability for resistors Good conductor adhesion	Higher microwave loss
Beryllia	Highest thermal conductivity	High cost Requires special thick film materials Toxic
Aluminum Nitride	High thermal conductivity Low CTE	High cost Requires special thick film materials

More recently another ceramic material, aluminum nitride (AlN), has come into wide use. AlN has some very unique properties that make its use highly desirable [4]. AlN, like BeO, has a very high thermal conductivity. Since the thermal conductivity of AlN increases with temperature, unlike BeO which decreases with temperature, AlN is a better material for high power applications. Additionally, AlN has none of the toxicity problems associated with BeO. Another desirable property of AlN is its close coefficient of thermal expansion (CTE) match to silicon. This means that it is more compatible with the large silicon devices that are being designed into MCMs. A great deal of research and development time has been spent to attach AlN to both MCM-D (deposited) substrates and LTCC MCM-C structures thus taking advantage of the thermal benefits of AlN [5]. Table 6-5 shows some of the electrical and mechanical properties of substrate materials, including AlN, used in hybrid applications.

Conductors

Thick film conductors are made from mixtures of metal powders, small amounts of vitreous or oxide powders and an organic phase that determines the printing

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Table 6-5 Properties of Commonly Used Ceramic Substrate Materials.

PROPERTIES	MATERIALS			
	AlN	BeO	Al_2O_3	Al_2O_3
Purity	98 - 99.8%	99.5%	96%	99.5%
Color	Dark gray to translucent	White	White	White
Density (g/cc)	3.255	3.01	3.70	3.87
Specific Heat (cal/g°K)	0.177			
Thermal Conductivity (W/m-k) at 25°C	80 - 260	250 - 260	20 - 35	20 - 35
CTE (10^{-6}/°C) (25°C - 400°C)	4.4	9.0	7.1	7.6
Dielectric Constant at 1 MHz	8.8 - 8.9	6.5	9.5	9.9
Dielectric Loss Tangent at 1 MHz	0.0007 - 0.0020	0.0004	0.0004	0.0001
Resistivity (Ω-cm)	$> 10^{13}$	10^{15}	10^{14}	10^{14}
Dielectric Strength (kV/mm)	10 - 14	9.5	26	24
Flexural Strength (N/mm^2)	280 - 320	170 - 240	250	400

Note: CTE (25°C-400°C) for Si = 3.35×10^{-6}/°C, for GaAs = 5.73×10^{-6}/°C.

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characteristics of the ink or the paste. In most cases the conductor inks are designed to be fired between 850°C and 950°C. The glass or oxide constituents of the ink are developed so that they react with the substrate and form a glass or oxide bond. This reaction provides the adhesion mechanism critical to the performance and reliability of the electrical circuit. The main function of a thick film conductor is to provide the electrical connections between different points in the circuit. Conductors also are used as resistor terminations to provide low contact resistance, as capacitor electrodes, as attachment pads for active and passive devices and as low value resistors.

Most commonly used thick film conductors fall into two categories: noble metals that can be fired in air, and non-noble metals that must be fired in an inert or reducing atmosphere. The noble metals include platinum, palladium, silver and gold, as well as binary and ternary mixtures of these metals. The non-noble metals include copper, aluminum and nickel. Of the non-noble metals only copper plays a major role in thick film technology.

Critical parameters characterizing a conductor are its conductivity, solder wettability, solder leach resistance (the ability of a conductor to not dissolve in the solder), adhesion and wire bondability. Good adhesion to the substrate is the one property required of all thick film conductors. A great deal of time and effort has gone into improving adhesion.

There are three basic mechanisms of adhesion between the substrate and the metal: glass bonding (fritted), oxide bonding (fritless) and mixed bonding. Fritted conductor systems add small amounts of low melting point glass powder to the metal. The glass powder, typically a lead borosilicate, melts during the firing process and wets both the particles of metal and the substrate. If too much glass is added, excess glass can float to the surface and cause problems with soldering and wire bonding. If not enough glass is used, adhesion is reduced.

Fritless adhesion mechanisms were developed originally for use with air fired gold formulations but were quickly adapted for use in nitrogen atmospheres and with copper conductors. In fritless conductors the glass is replaced by small amounts of copper oxide. During firing the copper oxide reacts with the alumina substrate to form a spinel (copper aluminate) structure that creates a chemical bond between the substrate and the metal. Too much oxide in the formulation will result in an oxide layer on the surface of the copper, reducing solderability and wire bondability. Too little copper oxide reduces adhesion. In many cases manufacturers plate the top copper layer with gold to eliminate problems associated with oxide formation.

A mixed bonded system produces the best of both worlds. By using both oxide and glass, the amount of each can be reduced, minimizing the deleterious effect of too much of either additive. Typically, better adhesion and improved wire bond strength are obtained with mixed bonded conductors.

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Table 6-6 Comparison of Key Conductor Metals for Thick Film Circuits.

PROPERTIES	SILVER	COPPER	GOLD
Conductivity	Excellent	Excellent	Excellent
Resistor Compatibility	Good	Good	Excellent
Print Definition	Good	Moderate	Excellent
Solder Leach Resistance	Poor	Excellent	Poor
Wire Bondability	Good*	Good*	Excellent
Processing	Very good	Moderate	Excellent
Cost	Very low	Low	High

* Aluminum wire

Three metals (gold, silver and copper) have found widespread use in thick film conductor inks used to make hybrid circuits. In addition, metals such as platinum and palladium have been added to the gold and silver, in either binary or ternary combinations, to enhance specific properties such as solderability and solder leach resistance. The properties of these materials are compared in Table 6-6.

Gold is useful because it is an inert metal and does not oxidize during subsequent processing steps. It is also highly conductive, and easily wire bondable. Active devices can be attached readily and reliably to gold pads on the substrate. The biggest drawback to the use of gold is its cost. Gold is approximately 10 to 20 times more expensive than silver or copper. Additionally, gold leaches (dissolves) readily with commonly used solder and is not typically used where soldering is required. If soldering is necessary, gold/tin solder can be used. Gold conductors find their greatest application where high reliability is an issue, particularly for military, medical and space related requirements. The addition of varying amounts of platinum and palladium to gold will improve the adhesion and the solder leach resistance at the expense of conductivity and wire bondability.

Silver is used in place of gold specifically where cost is an issue. Silver has a higher conductivity than gold and has lower losses at microwave frequencies. The biggest drawback to the use of pure silver in hybrid circuits is that it will

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migrate in the presence of voltage, humidity and ionic contaminants if not passivated properly. This electromigration of silver has precluded its use in many military and high reliability applications. Silver over time will tarnish making for more difficult soldering and bonding. While pure silver conductors leach readily, they have a significantly higher leach resistance to commonly used solders such as 62 Sn/36 Pb/2 Ag than do gold conductors. Components can be solder attached reliably to silver conductors for many applications. The addition of platinum or palladium improves solder leach resistance and inhibits migration, but lowers conductivity and increases cost. Silver bearing thick film conductors are used mostly for commercial circuits and as capacitor and resistor terminations. If silver is buried within a hermetic material, so that moisture or ionic contaminants are not present, no migration can take place [6-7].

A copper thick film technology was developed because of the high cost of gold and the reliability related issues of silver. Even though copper will oxidize, it is migration resistant and, therefore, acceptable for military and high reliability applications. Some advantages of copper are its high electrical conductivity, its low loss at microwave frequencies and its low cost. Values for all of these properties fall between those of gold and silver. The overall fabrication cost of copper circuits includes the additional cost of nitrogen gas. As mentioned previously, copper will oxidize, so the surface needs to be protected, usually by plating with gold. The plating process also adds labor costs to the product.

Dielectrics

A dielectric material is a material that does not conduct electricity. In the strictest sense of the word, a dielectric refers to a material used in a capacitor. An insulator is a material that provides electrical isolation between conductive circuit elements. In the microelectronics industry the two terms have become synonymous. Thick film dielectric inks are mixtures of dielectric powders and an organic vehicle. The dielectric portion of the ink may be a low melting point glass, a mixture of glass and ceramic powders or a crystallizable material. As with thick film conductors, the organic portion of the ink defines the rheological characteristics and determines how well the ink prints. There are five major applications or uses for dielectric inks in a hybrid circuit: crossovers, insulating layers in multilayer circuits, capacitors, encapsulation, and hermetic seals. The critical properties that define whether a dielectric material can be used in a given application are the temperature and frequency and voltage response of its dielectric constant, dissipation factor, insulation resistance and dielectric breakdown voltage.

Crossover Dielectrics. The crossover dielectric is a low dielectric constant insulating material used in single layer thick film hybrid circuits to separate two conductor traces or lines. A crossover configuration allows the production of the

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simplest type of three dimensional circuit. Crossover dielectrics are designed to separate conductors occupying the same location on the substrate, effectively increasing the available circuit area. The first crossover dielectrics were made from low melting point glasses such as lead aluminum borosilicates and were designed to be compatible with conductors fired around 850°C. Additionally these materials had to match the CTE of the substrate so that stresses were minimized during the processing of the hybrid circuit. It is important to be aware of some of the problems that can occur when using glass crossovers in a hybrid circuit. For example, depending on the number of times the glass is fired, reactions between the glass and the conductor can result in short circuits. Excessive flow of the glass can cause swimming (movement) of the conductor, possibly distorting the printed pattern.

Because of these problems, glass-ceramic formulations were developed to replace glass dielectrics. Glass-ceramic materials are made as a glass, printed and then crystallized during the firing process. The crystalline phase that forms is dispersed uniformly throughout the glassy matrix so that the resultant material has very uniform properties. The crystalline material has a higher softening point than the parent glass and is stable under multiple refirings as long as it is not fired higher than the original processing temperature. Another major advantage is that glass-ceramic crossovers have less tendency to form pinholes, minimizing short circuits. The glass-ceramic materials do not react with conductor materials to the same extent as their glassy counterparts. Other terms synonymous with glass-ceramics are crystallizable and devitrifying glasses.

Multilayer Dielectrics Once a hybrid circuit with crossovers has been designed and built there is no more area available on the substrate to increase the circuit density. Circuit density may be increased by increasing the size of the substrate, by printing on two sides of the substrate or by building a multilayer circuit. Since the latter has the fewest limitations, circuit designers have long been designing their hybrid circuits with multiple layers. By definition a TFM circuit is one containing multiple internal conductor traces separated by insulating dielectric layers.

Electrical connections between layers are made through vias in the dielectric filled with conductor. The same technical issues (of using glass-ceramic materials with the crossover dielectrics) presented even more serious challenges in making multilayer circuits. Material requirements for multilayer dielectrics are demanding due to the multiple firing steps required in processing. Glass-ceramics make the best multilayer dielectrics. As mentioned in the previous section, these stable materials limit problems such as blistering, conductor reactions and shorting. One common problem with devitrifying multilayer dielectrics is the incompletion of the crystallization process during the first firing

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step. Crystallization will continue through additional firings and the CTE of the layers may change making it difficult to control the CTE of the composite.

A glass-ceramic material developed for a multilayer circuit application must have certain properties that are not required when used as a crossover material. For example, because the overall thickness of the multilayer dielectric can be quite large and screen printed to cover the whole substrate, the dielectric material must have a CTE closely matched to the alumina substrate. Mismatch produces excessive substrate camber, making it difficult to print additional dielectric layers, to attach devices to the surface and to mount the substrate to a heatsink or to a package base. The via holes must remain open to allow electrical connections between the layers. Finally, the fired dielectric material should have a very good surface finish so that fine line patterning of the conductors is possible.

Capacitor Dielectrics As mentioned above, dielectrics also can be used as capacitors, but not so much in MCM applications. Typical materials are combinations of barium titanate ($BaTiO_3$) and glass to lower the firing temperature. Thick film capacitors for resistor capacitor (RC) networks or as blocking or bypass capacitors have dielectric constant values ranging from 20 - 2000. Typically they are porous and have poor mechanical integrity, but serve the purpose for which they were developed. Low firing (850°C - 1000°C) crystallizable capacitor formulations, called relaxor dielectrics, have been developed, which have very high dielectric constants (> 20,000).

Resistors Thick film resistors have been used in the microelectronics industry for over 40 years in applications ranging from simple resistor networks to printed resistors as part of very complex multilayer circuits. Most of the modern thick film resistor inks are combinations of heavy metal (lead or bismuth) ruthenate compositions or ruthenium dioxide dispersed in a glassy matrix. As with other thick film inks, these active ingredients are mixed with an organic vehicle that defines the printing characteristics of the ink. Resistor inks are usually formulated in a series of decade values ranging from 1 Ω/□ to 1 MΩ/□. The individual decade value inks, called end members, are blended in varying proportions to obtain resistivity values between those specified by the end members. The actual resistivity range is determined by the type of resistive element in the ink and by the ratio of this material to the glassy phase. When fired, (typically to 850°C) the glass softens and wets the resistive material and substrate. Typical electrical parameters of resistor inks are given in Table 6-7.

Resistor values, for design purposes, are determined by the equation shown in Figure 6-8. The key terms in the equation are sheet resistivity (Ω/□) and number of squares (defined as the resistor length divided by the resistor width). The resistance can be determined from this equation if the geometry of the resistor and the value of the ink are known. Thickness of the printed resistor is

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Table 6-7 Typical Fired Resistor Properties[1].

Sheet Resistivity[2] (Ω/□)	TCR[2] (ppm/°C)	Short Term Overload Voltage[3] (V/mm)	Standard Working Voltage[4] (V/mm)	Maximum Rated Power Dissipation[5] (mW/mm^2)	Blendable Series
10 ±20%	0 ±100	45	1.8	320	A
100 ±20%	0 ±100	22	9	810	A
1k ±20%	0 ±100	62	25	625	A
3k ±20%	0 ±100	77	30	300	A
3k ±20%	0 ±100	90	36	430	B
10k ±20%	0 ±100	145	58	340	B
100k ±20%	0 ±100	245	98	96	B
1M ±20%	0 ±100	310	124	15	B

1 Typical resistor properties based on laboratory tests using recommended processing conditions; termination - DuPont Pd/Ag Conductor 8134 prefired over DuPont Dielectric 5704 at 850°C; substrate - 96% alumina; printing - 200 mesh stainless steel screen (8 µm - 12 µm; firing 30 minute cycle to peak temperature of 850°C for 10 minutes.

2 Shipping specifications. Resistor geometry - 1.5 mm x 1.5 mm. Temperature coefficient of resistance - 55°C to +25°C to 125°C.

3 Short term overload voltage - tested under military specifications of MIL-R-83401D, Paragraph 3.15.

4 Standard working voltage - 0.4 × short term overload voltage.

5 Maximum rated power dissipation. $\frac{(\text{Standard Working Voltage})^2}{\text{Resistance}}$

another important factor affecting sheet resistivity. Values can be increased or decreased by varying the thickness of the printed resistor.

6.2.2 High Temperature Cofired Ceramic Technology

Dielectric Materials

The common dielectric material used to fabricate HTCC substrates or circuits is alumina with varying amounts of glass. Depending on the application, the percentage of alumina may vary from 88 - 96% but typically falls between 92 - 96%. Because of the maturity of this technology, the properties of both the raw materials and the fired ceramic have been well characterized. Table 6-8 shows

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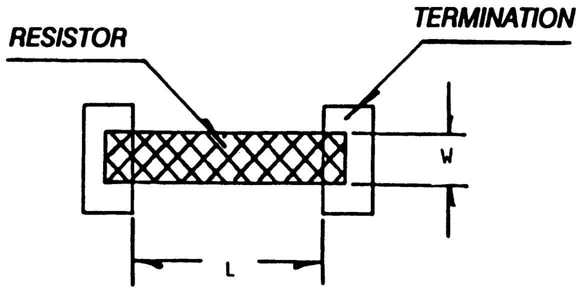

$R = \rho L/A$

Where R = Resistance
ρ = Bulk resistivity (resistance per unit volume)
L = Length of resistor
A = Cross-sectional area of resistor

$R = \rho_s L/W$

Where ρ_s = Sheet resistivity (ρ/t)
t = Resistor thickness
L/W = Number of squares

Figure 6-8 Equation to calculate resistance.

the key physical and electrical properties of fired alumina ceramic material. The critical parameters to note are flexural strength (which relates to the ability of the ceramic to withstand bending forces) and thermal conductivity. These properties differentiate HTCC dielectric materials from LTCC dielectric materials.

Conductors

All of the processing parameters for HTCC circuits are established by the fact that the alumina dielectric is a refractory material and must be sintered at approximately 1600°C. This limits the selection of conductors to high temperature metals such as tungsten and molymanganese. The thick film inks used for conductor traces and as via fills have been modified to match the sintering temperature and shrinkage rate of the alumina body. Since tungsten and molymanganese both oxidize readily in air, any exposed metal must be plated to protect the conductor surface. Typically two different metals are plated sequentially to achieve the best results. Nickel is plated first for solderability and brazability. Gold is then applied to keep the nickel from oxidizing so that reliable gold wire bonds and soldered leads can be formed. Both electrolytic and electroless nickel plating is used, but gold is usually plated electrolessly. Plating is a process that is not required by the other two MCM-C technologies. Also, the relatively high resistivity of tungsten and molymanganese metals is a limitation on their use for high speed, high frequency applications.

6.2.3 Low Temperature Cofired Ceramic Technology

Dielectric Tape Materials

The driving force in developing a low temperature cofired process was the use

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Table 6-8 Physical and Electrical Properties of Ceramic Material for HTCC Multichip Modules.

Composition	92% - 96% alumina
Color Available	White or black
Flexural Strength	55,000 psi (380 N/mm^2)
CTE 25°C - 200°C	6.3 x 10^{-6}/°C
Thermal Conductivity at 100°C	15 W/m-K
Volume Resistivity at 25°C	10^{14} ohm-cm
Dielectric Constant at 25°C	8.9
Hermeticity	1 x 10^{-8} cc/sec

of the high conductivity metals and thick film processing. The alumina dielectric used in the HTCC process was replaced with dielectric materials that fire below 1000°C, specifically around 850°C. Such materials were available from TFM circuit technologies. Standard thick film dielectric formulations in tape form became the basic building block for developing the LTCC technology. The low temperature dielectric allowed standard thick film materials and processes to be used when manufacturing LTCC MCMs.

Two basic types of dielectric materials are used in LTCC fabrication today. These are alumina filled glasses and crystallizable ceramics [8]. In the alumina-filled glass, glass softens and wets the alumina powder during firing, providing a dense hermetic structure. Most of the critical parameters of the fired composition, such as firing temperature, CTE, mechanical strength and thermal conductivity, are dictated by the nature and properties of the glass. Most typically the fired properties are designed to match the CTE of standard alumina ceramics. They are also designed to have dielectric constants from 6 to 9. Another benefit of using alumina filled glasses is that the glass softens during firing, allowing the dielectric to conform to the setter on which it is fired. The finished part can be extremely flat. Alumina filled glass dielectric tape, Green Tape®, is available from Dupont. Other thick film suppliers, such as ESL and EMCA, also manufacture and sell tapes.

Another dielectric formulation is a glass-ceramic or crystallizable material, a magnesium aluminum silicate, called cordierite [8]. As discussed in Section 6.1.2, glass-ceramic materials exhibit many of the same advantages over alumina

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filled glass type formulations. For example, LTCC modules made from glass-ceramic materials are much less sensitive to the adverse effects of multiple firings. This is advantageous when parts are subject to additional postfiring steps. Also, the ceramic does not soften when fired as much as alumina filled glass parts soften. Glass-ceramic dielectric tapes are available from Ferro and Dupont. Different variations of commonly used LTCC dielectric materials and their electrical and physical properties are shown in Table 6-9.

The most significant feature of the cordierite glass-ceramic system is its stability when fired in nitrogen for use with copper conductors. Another process [9] is the firing of the LTCC/copper laminate in a steam-hydrogen gas mixture instead of in a nitrogen-oxygen gas mixture. The steam-hydrogen firing atmosphere ensures that a proper range of oxygen potentials exists, at the temperatures of interest, to remove completely carbon residue and to allow complete densification of the glass-ceramic without oxidizing the copper.

Conductors

The use of thick film dielectric formulations for the tape allows the use of the high conductivity conductors such as gold, silver and copper to make the LTCC MCMs. Most of the work has been with gold conductors.

Cofired top conductors, inner layer and via fill golds are available which eliminate registration problems associated with nonuniform fired shrinkage. Shrinkage variations are eliminated by printing the top conductor either on an unlaminated sheet of tape or on the laminate prior to firing. The number of processing steps, the process time, and the cost of the finished part are all reduced by cofiring all of the top layer metallizations.

Gold conductors available from commercial suppliers exhibit physical properties that are comparable to their thick film counterparts. Gold materials have been tested and have been shown to exceed Mil Spec requirements for 1.0, 1.5 and 2.0 mil gold wire bond adhesion. These same conductors also have been tested and passed requirements for TAB applications. See the discussion in Section 9.4.

LTCC modules must also interface to other modules. A low temperature brazing capability (the joining of two metals together using a filler material with a lower melting temperature than either of the base metals) has recently been developed using either gold/tin solder or gold/indium solder [10]. Brazing allows reliable attachment of leads and seal rings giving the LTCC technology a packaging capability. Figure 6-9 shows an example of an LTCC module with brazed leads (25 mil pitch) and a brazed Kovar seal ring demonstrating the capability of manufacturing packages that can be sealed hermetically. The part is 2.8" × 2.8", made from 10 layers of 6.5 mil tape. There are over 10,000 6 mil electrical vias, 20 mil thermal vias, 5 mil lines and spaces and ground and power planes.

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Table 6-9 Physical and Electrical Properties of Common LTCC Dielectric Materials.

Matrix	Fillers	Firing Temp. (°C)	Firing Atm	Dielectric Constant	Tan δ	TCE (ppm)	Shrinkage (%)	Shrinkage Tolerance (%)
BaO-Alumino-Borosilicate	Al_2O_3 Forsterite	850-900	air	5.0-6.5	0.0008-0.002	3.8 - 6.8		
Alumino-Borosilicate	Proprietary	850	air	7.8	0.002	7.9	12	±0.2
Borosilicate	Al_2O_3	900	reducing	5.6		4.0	16	
Pb-Alumino-Borosilicate	Al_2O_3 $CaZrO_3$	850	air	9 - 12	0.001 - 0.003		16	
Cordierite	None	925 - 1050	air/neutral	5.3 - 5.7		2.4 - 5.5		
Spodumene	None	850 - 990	air/neutral	5.0 - 6.5		2.0 - 8.3		
MgO-CaO-Alumino-Borosilicate	Al_2O_3	1000	reducing	7.1	0.0025			
BaO, SiO_2, Al_2O_3, CaO, B_2O_3	None	950 - 1000	reducing	6.1	0.0007	8	13.5	
CaO-Alumino-Borosilicate	Al_2O_3	880	air	7.7	0.0003	5.5	16	
Pb-Borosilicate	1) Al_2O_3 2) Cordierite 3) SiO_2	900 900 900	air air air	7.8 5.0 3.9	0.003 0.005 0.003	4.2 7.9 1.9	13 13.7 13.9	< 0.3 < 0.3 < 0.3

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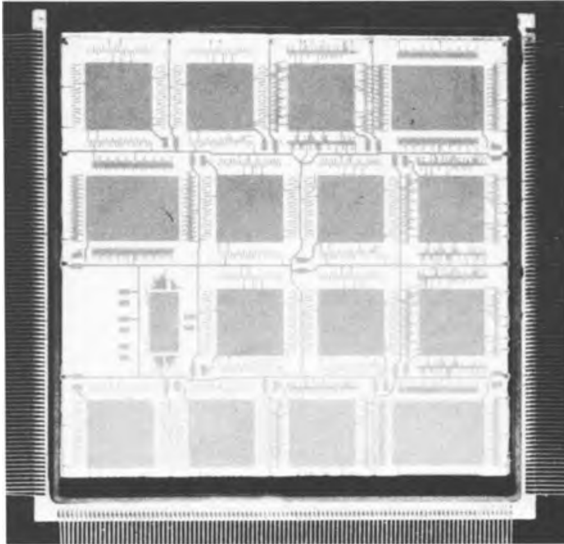

Figure 6-9 LTCC module demonstrating brazed leads and Kovar seal ring.

The full cost advantage of the LTCC technology requires that the expensive gold conductor be replaced with a reliable, lower cost metal. Both copper and silver conductor systems offer possibilities. The silver conductor system is easier to implement, since it can be fired in an air ambient. Formulations of silver and silver/palladium mixtures for inner layers, via fills and top layer conductor formulations compatible with commercially available dielectric tape formulations exist. These systems are used currently to build LTCC modules.

Silver and silver/palladium conductors also can be used on top of the LTCC structure to satisfy wire bonding and soldering needs for commercial applications where humidity is not a major issue. The metal system is not acceptable for military and commercial circuits requiring high reliability. Silver based conductors do not meet the environmental, wire bonding or soldering requirements demanded for those kinds of circuits. Gold conductor must be used where gold wire bonding is needed. For solderability requirements, the best results have been obtained using gold/platinum conductors. A low cost option to gold/platinum is a low firing (< 600°C) copper conductor. This type of conductor will meet all of the soldering and adhesion requirements of high reliability circuits without degrading the properties of air fired conductors and dielectrics when fired in nitrogen [11].

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Resistors

Resistors currently play a limited role in LTCC designs. The same standard thick film resistor inks developed to use on top of thick film dielectric can be used with the LTCC dielectric layers because the ceramic has already been fired. One problem is that the irregular fired surface makes it difficult to print the correct thickness of resistor. This problem is magnified when very small resistors (< 0.030" × 0.030") are needed. This nonflat or contoured surface occurs after firing because of differences in compressibility between the printed conductor and the dielectric tape.

A big advantage of the LTCC technology is that buried resistors can be printed and cofired with the rest of the part. This feature allows the MCM manufacturer to reserve more of the surface area of LTCC modules for active devices rather than for passive components. The major drawback to burying resistors is that resistor materials have not been developed fully for this purpose. Reaction with the dielectric tape can occur making it difficult to achieve correct design values. Buried resistors cannot be trimmed easily, so that resistor values must be designed with wide tolerances.

6.3 PROCESSING

6.3.1 Thick Films

Screen Printing

Thick film circuits are manufactured with a series of screen printing passes. A flow diagram for processing a TFM circuit is shown in Figure 6-6. The process starts with the development of a thick film layout from the circuit schematic. Layouts are generated typically on a computer aided design (CAD) system. Each print must have its own artwork. From a CAD system, a photoplotter is used to generate the mylar film or glass mask necessary for each screen, even in multiple-up configurations. The artwork positive (the pattern to be printed is dark) is placed against a photosensitive emulsion coating on the proper mesh size screen and exposed, defining the desired pattern. Once the screen is made, it is placed in a screen printing machine and covered with ink. The pattern is aligned to the substrate or to a previous pattern. A squeegee forces the thick film material through the open areas of the screen onto the substrate. The part is then dried and fired. This printing cycle is repeated for each print pass required.

The printing process requires control of a number of key parameters: print head speed, durometer (hardness) of the squeegee, sharpness of the squeegee, angle of attack and snapoff distance. Other parameters needing control are the screen mesh type, the wire diameter, the number of openings per inch, the

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emulsion buildup, the emulsion type and the ink viscosity. Screen printing machines may be fed automatically or by hand. Automatic systems may include the use of vision systems to reduce set up time and to optimize printer throughput.

Drying and Firing

After each pattern is printed the ink must be dried to remove organic solvents that give the ink its desired rheological properties. A typical drying temperature is 85°C - 150°C for five to ten minutes. Drying can be done in either a box oven or a continuous belt dryer. The drying process plays a critical role in obtaining the fine line definition required for the circuit. After each printed layer of the multilayer is dried, the part must be fired. Firing is a well defined process and can be accomplished using conventional furnace equipment. A typical thick film furnace profile is shown in Figure 6-10. Most materials are fired to 850°C with a 10 minute dwell time at peak temperature in clean, dry air. Other critical parts of the firing profile are the heating and cooling rates. As the part is heated, the organic binder portion of the ink is burned off, usually by 500°C. From

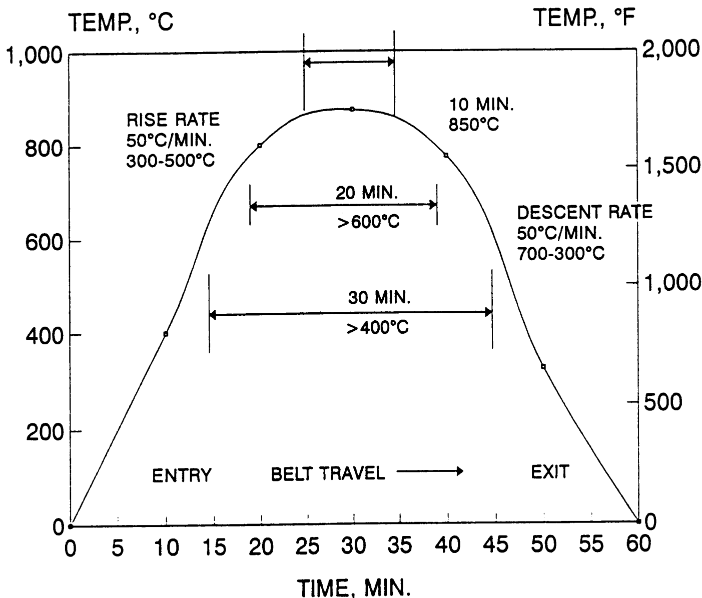

Figure 6-10 Typical thick film furnace profile.

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500°C - 850°C any glass or oxide in the paste will soften and react with other elements of the ink or the material on which it is printed (the alumina substrate or a dielectric layer). It is during this part of the profile that sintering and densification occur. The rate of heating is important because it controls how rapidly and how completely the organics are removed. The cooling rate is critical because thermal stresses are set up during cooling. If parts are very large, if the substrate has been laser machined or if there are laser drilled holes, cracking may occur during cooling.

6.3.2 High Temperature Cofired Ceramics

Process Flow

The process sequence for a typical HTCC process is given in Figure 6-4. It begins with the dielectric tape. Initially, each lot of cast tape is inspected for defects such as pits, thin spots and contamination and is characterized prior to use. Tape is cast in thicknesses from 0.004" - 0.025" depending on the electrical and mechanical requirements of the parts being fabricated.

Once the tape is accepted it is blanked (cut into individual sheets) to a standard size using either a blanking die or a computer controlled cutting machine. Each sheet of the tape is punched to form vias, cavities and/or castellations (grooves formed in the edges of the ceramic to aid in solder attach and subsequent inspection). These features can be made using either hard tool punching dies or with computer aided punching machines. After all of the tape machining steps have been completed, the vias are filled with conductor ink and the conductor is printed, both usually with tungsten metal. Typical conductor thicknesses vary from 0.0003" - 0.0005". As with thick film processing each conductor print must be dried prior to performing any additional processing. Next the individual sheets are stacked onto each other and laminated for fixed times, temperatures, and pressures. Laminating pressures can vary from 2000 psi to 4000 psi; laminating temperature varies from room temperature to 100°C depending upon the tape formulation used by each manufacturer. In most cases the completed laminate is scribed and/or cut into individual parts or to the final shape of an individual part.

The individual laminated parts are fired to approximately 1600°C in a reducing atmosphere to sinter the structure and to prevent oxidation of the refractory metals. Firing can be done either in an automatically controlled high temperature box furnace or in large continuous pusher type furnaces. The overall burnout and firing cycle is quite long, 24 to 48 hours. Typical HTCC parts when fired shrink approximately 16% ±0.5 in the x- and y-directions and 20% ±2 in the z-direction.

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6.3.3 Low Temperature Cofired Ceramics

Process Flow

Extensive hands-on labor is required for making LTCC circuits, because of the newness of the technology and the lack of high volume applications. Most manufacturers of LTCC products buy the tape formulated and cast by materials suppliers, which shifts the burden of defining good material to the user. Tape is cast on mylar and stored in this fashion. The first step in the manufacturing process is to inspect the tape for defects, such as pits, holes and contamination. Areas that are not usable are marked and removed from the roll. Then the tape is stripped from the mylar and blanked using steel ruled dies or some type of cutter to a specific standard size such as 5" × 5". Because of problems associated with tape relaxation (shrinkage) after removal of the mylar, the tape goes through a low temperature preconditioning bake to stabilize it. Preconditioning allows the tape to be stored without further shrinkage.

The process sequence for LTCC parts is shown in Figure 6-5. It is very similar to the process flow for HTCC parts. Each sheet is rotated 90° to eliminate any possibility of nonuniform firing shrinkage resulting from tape casting direction. Registration holes and vias are formed in the individual sheets of tape. The vias are filled using specially formulated via fill conductor inks designed to shrink at the same rate as the dielectric material when fired. Conductors are printed using standard screen printing equipment and processes. After printing all conductors, any cavities in the tape are cut or nibbled using an automatic punch. Finished sheets are stacked on a laminating plate over tooling pins. The laminating fixture is placed in a conventional uniaxial laminator or in an isostatic laminator. The typical laminating cycle is 3000 psi at 70°C for ten minutes, but pressures can vary from 2000 - 4000 psi and temperatures from 60°C - 80°C. Isostatic lamination is more advantageous than uniaxial lamination because the same uniform pressure is applied to the whole part, and because parts of varying sizes can be laminated simultaneously.

The part can be fired after lamination using either of two slightly different procedures. The first procedure requires a separate furnace to burnout the organics. After burn out the part is fired in a conventional thick film belt furnace using a profile similar to the one shown in Figure 6-10. The second firing process uses a modified thick film furnace so that burnout and firing can be done as a single step. For this firing process there are two separate temperature holds. The first, typically at 500°C, is the binder burnout step. The hold, typically at 850°C, allows the ceramic material to densify. The single step furnace profile is faster than the two step furnace process, but may not be as desirable for large complex modules. Fired parts typically shrink 12% ±0.2 in the x- and y-directions and 17% ±2 in the z-direction. The tighter shrinkage

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Table 6-10 Thick Film Multilayer Design Guidelines.

PARAMETERS	STANDARD	CUSTOM
Substrate Size	< 7" x 7"	> 7" x 7"
Substrate Thickness	> 0.025"	< 0.025"; 0.050"
Maximum Number of Layers	< 8	> 8
Dielectric Thickness	> 0.045 µm	> 0.045 µm
Minimum Line Width	0.008"	0.005"
Minimum line Spacing	0.008"	0.005"
Minimum Via Diameter	0.008"	0.005"

tolerance is a major advantage over HTCC technology. The fired dielectric material, whether an alumina filled glass or a glass-ceramic, is very dense and has proven to be hermetic. Hermeticity is the key material property necessary for developing a low cost silver LTCC process. Moisture will not penetrate the package and buried silver will not migrate since the dielectric is hermetic.

6.4 DESIGN RULES

Well defined design rules exist for both TFM and HTCC technologies since these are both mature technologies. Typical design guidelines for these two technologies are given in Tables 6-10 and 6-11. LTCC is a relatively new technology and is evolving so that design rules are still changing. A typical set of LTCC design rules for circuits being built today is listed in Table 6-12.

When comparing the design rules for LTCC circuits with thick film and HTCC, the number of dielectric layers and the pitch of the printed conductors are the areas of difference. Typically the number of layers is greater and the pitch is lower with LTCC designs. LTCC circuits generally require some additional means to handle thermal dissipation. Since the thermal conductivity of the LTCC dielectric material is much lower than the alumina used for thick film and HTCC, thermal vias or slots are designed into these circuits for power management. The addition of thermal vias increases the thermal conductivity of the LTCC module so that it becomes a thermal equivalent to 96% alumina. An example of a part with thermal arrays is shown in Figure 6-11. This module is

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Table 6-11 HTCC Design Guidelines.

PARAMETERS	STANDARD	CUSTOM
Size (max.area)	6"x 6"	6" x 6"
Number of Layers	≤ 15	≥ 15
Layer Thickness	0.010" - 0.025"	0.005" - 0.010"
Tolerances Length and Width Thickness Camber	 ±0.8%, NLT ±0.004 ±10%, NLT ±0.003 0.003"/", NLT ±0.002	 ±0.5%, NLT ±0.002 ±5%, NLT ±0.001 0.002"/", NLT ±0.001
Conductor Width	0.007" minimum	0.004" minimum
Conductor Spacing	0.007 minimum	0.004" minimum
Via Diameter	0.007 nom.	0.005" nom.
Via Cover Pad	0.014"8	0.006"
Via Center to Center	0.024"	0.010"
Via Center to Center (with one conductor)	0.034"	0.020"
Sheet Resistivity	0.012 Ω/□	0.008 Ω/□
Via Hole Resistance	0.010 Ω/□	0.005 Ω/□

a MIL STD 883 Group D test coupon, built by CTS Microelectronics Division. It is made from nine layers of 6.5 mil tape and has arrays of 20 mil thermal vias stacked from top to bottom beneath the two large die pads for thermal management. When fully assembled there is 60% silicon coverage of the top surface. This test coupon also demonstrates the ability to print 3 mil lines and spaces.

6.5 APPLICATIONS

Current and future applications for MCM-C can be divided into three major categories: military/aerospace, medical, and commercial.

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Table 6-12 LTCC Design and Producibility Guidelines.

Parameters	Preferred Manufacturing	Prototype Manufacturing	Future Development
Maximum Substrate Size (fired)	1.5" x 1.5"	3.5" x 3.5"	12" x 12"
Minimum Line Width (cofired)	10 mil	5 mil	2 mil
Minimum Line Space 8(cofired)	10 mil	5 mil	2 mil
Minimum Line Width (postfired)	10 mil	5 mil	2 mil
Minimum Line Space (postfired)	10 mil	5 mil	2 mil
Minimum Via Diameter	8	6	4
Maximum Layers of Stacked Vias	3	4	6
Maximum Thermal Via Diameter: 4.5 mil thick tape ≥4.5 mil thick tape	 15 mil 20 mil	 20 mil 25 mil	 25 mil/slots 25 mil/slots
Maximum Number of Metal Layers	10	15	25+

The initial development of LTCC MCMs, using commercially available material, was a result of government funded programs. This development is discussed further in Chapter 15 of this book as a case study. The first applications were for memory circuits. LTCC modules were fabricated with over 1 megabyte of memory packaged in a ceramic block less than an inch square.

There is still interest in using MCM-C technology in military electronics, particularly in the areas of microwave and millimeter wave packages. The technology driver here is improved performance and lower cost. LTCC could become the dominant military packaging technology as dielectric materials are modified to perform better at higher frequencies and as the less expensive metals become acceptable.

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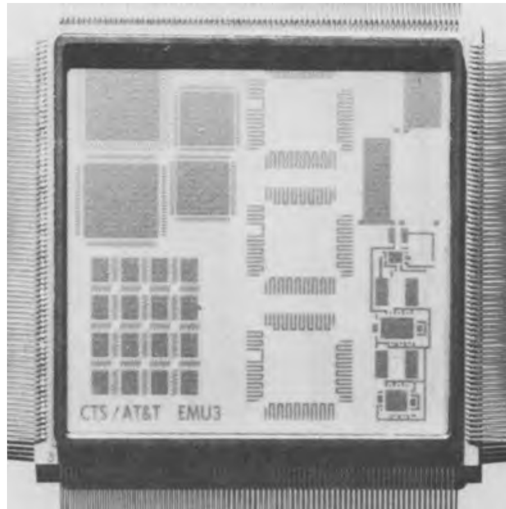

Figure 6-11 LTCC module with thermal arrays. (Courtesy CTS Corporation.)

The medical industry is another industry that has adopted the use of MCM-Cs, in particular, LTCC circuits. These applications require high reliability, reduced weight and smaller packages at lower cost. Large numbers of medical pacemakers, hearing aids and defibrillators are being manufactured using LTCC technology. Figure 6-12 shows a heart pacemaker manufactured for a supplier of medical hybrids. It uses seven layers of 6.5 mil tape and has 900 8 mil electrical vias, 5 mil lines and spaces and is double sided. The hearing aid in Figure 6-13 is manufactured with five layers of 7.5 mil tape and has 10 MΩ, 20% resistors postfired on the surface. This part also is double sided and has a hole punched in it after lamination.

The overall growth in MCM-C usage will be determined by high volume commercial applications, such as occur in the computer, transportation and telecommunications industries. The need for high performance CPUs, microprocessors and memory circuits, combined with the growing popularity of workstations, personal and laptop computers makes the computer industry a critical area of focus. The drive to reduce the size and weight of packages combined with the need for increased electrical performance makes MCM-C packaging technologies ideal for these applications. The electronics requirements of the transportation industry continue to grow becoming a major component in

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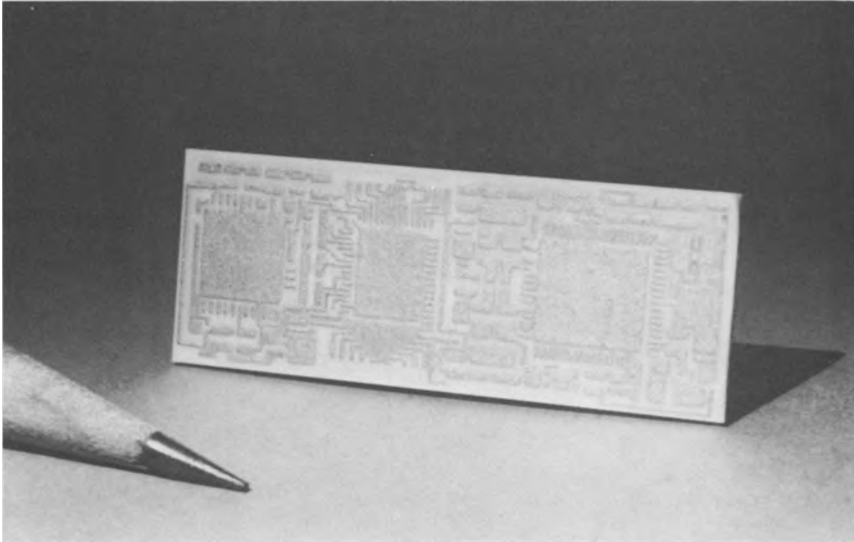

Figure 6-12 LTCC heart pacemaker. (Courtesy Pacesetter Systems Inc.)

the cost of new cars. Some applications include on board computers and collision avoidance radar, as well as electronic sensors to determine brake wear and fuel levels. The part shown in Figure 6-14 is an aircraft antilock brake hybrid circuit made with eight layers of 6.5 mil tape, 8 mil vias and a stepped through cavity. It contains three decade value 1% postfired resistors. All these applications require low cost, small, rugged electronic packages. MCM-C hybrid circuits meet these requirements. MCM-Cs will play a major role in telecommunications, particularly home satellite receivers and their related electrical circuitry, where the requirements are also for low cost, light weight hybrid circuits such as MCM-Cs.

6.6 FUTURE TRENDS

At a recent conference on MCM technology [12] a great deal of discussion took place on the merits and future of each individual MCM technology (MCM-L, MCM-D and MCM-C). Manufacturers of MCM-L made it quite clear that they have the low cost alternative. They claimed that MCM-L would be the technology leader within the next ten years, if advances are made in fine line processing techniques and in methods to handle the thermal dissipation.

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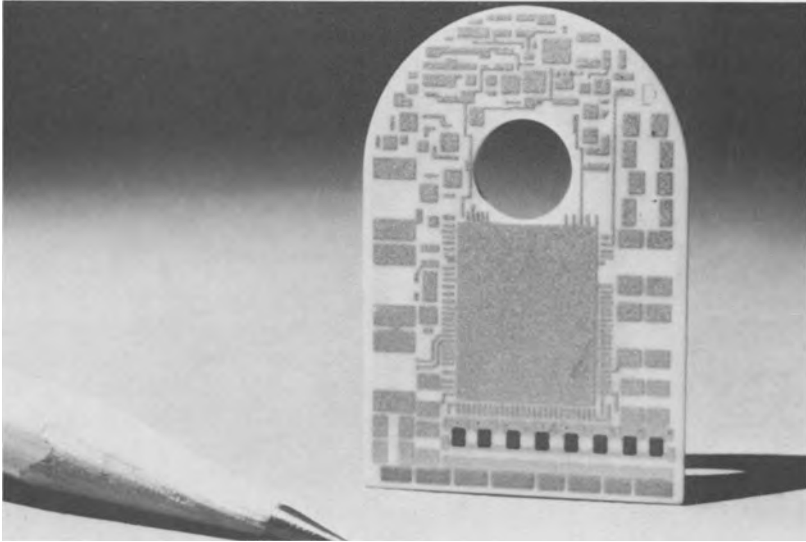

Figure 6-13 LTCC hearing aid. (Courtesy MiniMed Technologies.)

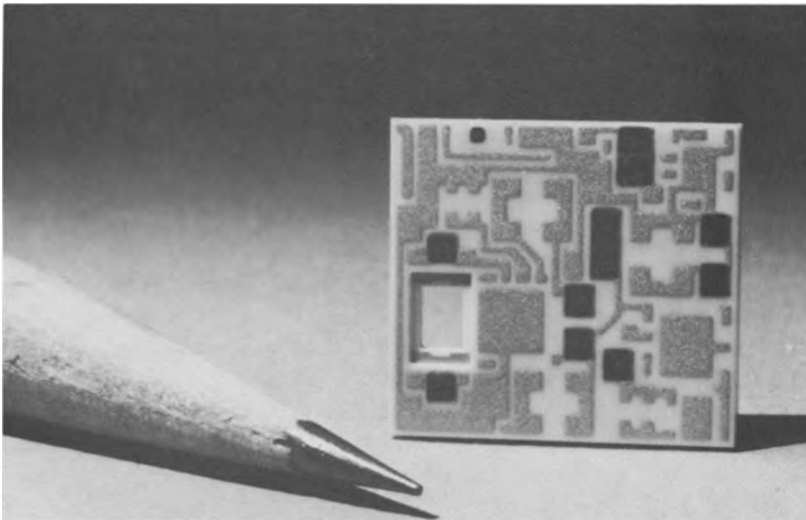

Figure 6-14 LTCC antilock brake substrate. (Courtesy Allied Signal Bendix Engine Controls.)

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Engineers and scientists involved with MCM-D argued their case with equal fervor. They pointed to future requirements for high speed, high density circuits and indicated that no other technology could do what MCM-D could do.

Surprisingly no one vouched for the future of MCM-Cs. The consensus, however, was that it is the technology of the present! Specifically, we now consider high frequency applications, new ceramic materials, buried passive components, fine pitch interconnections and thermal management techniques as areas for future development.

Input from military systems' houses and newly funded government programs indicate that MCMs will need to be capable of performing at very high frequencies (in the 40 - 60 GHz range) in future years. LTCC materials are expected to meet this capability. Some new low firing ceramic dielectric formulations already operate at these frequencies with low transmission loss. Silver will be used as an interconnect metal for MCMs. The combined benefits of reduced transmission loss and the lower cost of silver conductor will encourage the replacement of gold. Using lower dielectric constant tape materials will produce a positive benefit for high frequency and high speed requirements. Dielectric materials with dielectric constants as low as 4, and developmental materials having dielectric constants as low as 2.5, will be available for both thick film and LTCC MCMs. Similarly, new high temperature materials for HTCC MCMs, such as mullite, with a CTE similar to silicon and a dielectric constant lower than alumina (6.8), will open application areas for HTCC [13].

Fine line technology is another future trend that will influence the use of MCM-Cs. A great deal of time and money is being spent to reduce the pitch of conductor traces on thick film and cofired ceramic modules. While 5 mil lines and spaces are common now, future goals include 2 mil lines and spaces. One approach is the use of standard screen printing techniques with new fine print conductor pastes and advanced wire materials and emulsions for making the screens. Wires are now available as fine as 0.7 mils in 325 and 400 mesh screens. Screen mesh open areas greater than 50% allow denser lines to be printed. These advanced wires also are much stronger and do not stretch as easily and quickly as standard wire materials. Finally, new emulsion materials allow much sharper line definition than is possible with the older emulsions.

New techniques for attaining top layer fine lines are being investigated and, in some cases, are being implemented into advanced designs. Technologies such as photolithography, sputtering, laser delineation of solid ground planes and ink writing are all techniques for reducing the conductor pitch. The ultimate goal may be to couple thin film MCM-D technology with multilayer thick film and cofired MCM-C technology (MCM-C/D). See the discussion in Chapter 7.

Power management is becoming more important and more difficult to accomplish. It is not high power circuits alone where heat management is

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critical. As more and more low power devices are packed onto ceramic modules, the overall heat dissipation requirement of these packages becomes an issue. Several future trends in this area are becoming apparent. AlN is an important substrate material for TFM circuits and HTCCs. Development of compatible thick film materials (gold, silver and tungsten) is continuing. The increased availability and increasingly lower cost of AlN has renewed interest in its use. The tape transfer process can be used on AlN substrates. Tapes compatible with AlN material also have been developed. Combining the use of AlN substrate/package base with the ability to make cavities in the tape, so that high power devices can be mounted directly on the substrate, makes this future combination of new technologies quite interesting. AlN can also be coupled to LTCC structures using pressure assisted sintering techniques. The same benefits as with TTRAN on AlN are realized. A more standard approach to power management for LTCC modules has been the use of arrays of thermal vias beneath the high power devices. Such configurations are limited in capability. A better approach is to attach heatsinks (such as AlN, W/Cu and any number of the new thermally conductive composite materials) to the fired module. The heatsink can be soldered or brazed to the bottom of the package and the devices mounted directly on them.

Another possible trend is the use of buried components within the LTCC body. Buried resistors are examples here, but there may be an even greater demand for buried capacitors and inductors.

6.7 ENGINEERING CHOICES

The first decision a circuit designer makes is which of the three major MCM technologies should be chosen (MCM-L, MCM-D or MCM-C). This decision is based generally on three specific areas: familiarity with the technology, technology innovations or drivers and cost.

In many cases the selection is based on familiarity with and availability of a specific technology. For example, people comfortable with or already using organic printed wiring boards (PWBs) would tend towards MCM-L technology since this is what they understand best. Similarly circuit designers working with and knowledgeable about thin film or semiconductor technology would most likely pick MCM-D technology as their first choice. Finally, it is apparent also that practitioners of thick film technology look upon MCM-C technology as being the closest, in materials and processing, to what they do best.

Looking at technology drivers and cost as critical decision makers the choice becomes much more complex. Suppliers of MCM-L claim that their product is less costly to manufacture and is therefore more attractive to use [14].

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Unfortunately there are a number of applications where MCM-Ls cannot be used until technological issues such as high density, power management and hermeticity are fully resolved.

The choice between using MCM-D or MCM-C technology is not clear cut since both technologies require different uses of ceramic materials, either as a platform or as the package itself. The determination of the selection is made usually because of circuit density and cost requirements.

Most manufacturers of MCM-D circuits point to three specific advantages of their technology. The first advantage is the ability to achieve finer conductor geometries with thin film processing. The second advantage is the lower dielectric constant of the polyimide dielectric. The final advantage is the higher thermal conductivity of the silicon, alumina or AlN substrate on which the multilayer thin film circuit is processed. The major shortcoming of this process is that it is essentially a serial, batch process; therefore, process times and manufacturing costs are quite high. Unfortunately MCM-D technology does not readily lend itself to high volume production. This may limit the area of potential applications.

Manufacturers of MCM-C circuits will highlight their ability to process larger parts with many more layers than can be made with MCM-D technology. While line density and spacing may not be as fine as that attainable with thin film technology, there are other technology tradeoffs: lower cost, higher volume manufacturing, faster prototype turn around time, tailorable ceramic dielectric properties, the capability to add integral passive components and to seal the package hermetically.

The technology innovations and process changes being made in both the materials and manufacturing processes for MCM-Cs (specifically thick film and LTCC) and MCM-Ds will make it more difficult in the future to determine which of these technologies to choose. Manufacturers of MCM-Ds could build circuits that have tighter pitches (approaching 2 mil lines and spaces rather than micron size). The defect density of the substrate would become less of an issue. Yields go up and costs come down. Manufacturers of thick film and LTCC circuits are reducing the print geometry of their conductor traces. New technology in the area of screen emulsions and wires and the development of fine print conductors allow lines and spaces approaching 2 mils, albeit not yet for high volume manufacturing. Finally, new dielectric materials have been developed with dielectric constants as low as 3.5, making inorganic systems equivalent to their organic counterparts. What this all means is, as the performance gap between MCM-D and thick film and LTCC MCM-C technologies continues to diminish, the deciding factor in choosing one over the other will come down to cost, yield and volume throughput.

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What is not so well defined is where LTCC technology should be used instead of the other two MCM-C technologies. Simple, low layer count circuits will be less expensive to build with thick film than with either of the other ceramic technologies. However, the industry appears to be moving away from this concept toward denser MCMs with increasing silicon area demands. As this happens, LTCC circuits with their potentially lower cost and quicker manufacturing turnaround time should dominate, especially as this technology moves up the learning curve.

LTCC circuits, since they use higher conductivity metals, also have a major advantage over HTCC MCMs. There is an increasing interest in MCMs that operate at millimeter wave frequencies (20 - 40 GHz) and higher. HTCC circuits using tungsten metal cannot be used for this application. LTCC technology also has the advantage of being much more flexible than HTCC technology. The potential for dielectric materials with varying dielectric constants and CTE makes it even more attractive.

In general the decision on which one of the three MCM-C technologies to use is still an open issue. Both TFM and HTCC circuits, because of their maturity, appear to be the technology of today. However, the future may belong to LTCC technology. As materials improve, processes become better controlled and the technology matures, the natural advantages of LTCC could predominate and make it the MCM-C of choice. Most likely all of the technologies will continue to be used depending on the particular application required.

Acknowledgments

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7

THIN FILM MULTILAYER INTERCONNECTION TECHNOLOGIES FOR MULTICHIP MODULES

Ronald J. Jensen

7.1 INTRODUCTION

Historically there has been a wide gap between the feature geometries on integrated circuits (ICs) (typically ~1 μm) and those of IC packages and printed wiring boards (PWBs) (typically 50 - 100 μm). To achieve the ultimate density and speed in electronic systems, this gap must be closed, and it is inevitable that the thin film processes used to fabricate ICs will be required for IC packaging. In recent years, there has been active development of thin film multilayer (TFML) structures to provide high density interconnections between ICs in multichip modules (MCMs). The materials, processes, and designs for TFML interconnections are the focus of this chapter.

The term "thin film" does not refer to a specific range of film thicknesses, but implies the use of IC processes to achieve high density patterns in conductor and dielectric layers, roughly 2 - 25 μm thick. This chapter focuses on multilayer structures to distinguish the technology from single layer thin film metallizations (such as thin film resistors or bonding pads) that have been used on cofired ceramic or hybrid substrates for many years. The TFML interconnections generally use high conductivity conductor materials (such as copper, aluminum or gold). The conductor layers are separated by deposited dielectric layers, usually polymers with low dielectric constants. Within this

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broad definition there are many options for selecting substrate, conductor and dielectric materials. Many different processes are available for depositing and patterning the multilayer structures. Also, TFML interconnections may be implemented in a variety of package designs.

The development of TFML interconnections has been a major trend in electronics packaging over the last 5 to 10 years, coinciding with the emergence of MCM technologies. The term "MCM-D" was introduced to describe a wide variety of MCMs using thin film interconnections with deposited dielectrics. MCM-D generally is recognized as the most important and extendable MCM technology for future systems. However, the growth of the MCM-D market has been slower than expected, largely due to high costs, limited availability of substrates and advances in competing technologies such as ceramic-based MCMs (MCM-C) or MCMs based on laminated PWB technology (MCM-L). It is important to examine critically the strengths and weaknesses of thin film interconnections relative to other packaging technologies.

This chapter gives a general description of TFML interconnections, their characteristics and their benefits relative to alternative interconnection technologies. It examines, in detail, the options for substrate, conductor and dielectric materials, followed by options for processing multilayer structures. Design strategies for implementing thin film interconnections in MCMs are examined and illustrated with examples from industry. Finally, the tradeoffs involved in selecting an interconnect technology are summarized and the potential for the growth and extension of thin film interconnections is explored.

7.2 CHARACTERISTICS, BENEFITS OF TFML INTERCONNECTIONS

The primary emphasis in multichip integration is to achieve high silicon density in the MCM. This results in a smaller package, lower system cost and higher speed due to the shorter interconnection length between chips. However, it creates a need for a multichip substrate with high interconnection density. MCM-D approaches meet this need by using IC processes (such as photolithography, vacuum deposition, wet and dry etching) to pattern multiple layers of interconnections in deposited thin films. High conductivity metals, primarily copper (Cu), gold (Au) or aluminum (Al), are used for the conductor layers. The most widely used dielectric materials are polymers, particularly polyimides, which have high thermal, chemical and mechanical stability and low dielectric constants. The high conductivity conductor and low dielectric constant dielectric produce interconnections with low resistance and capacitance that can transmit high speed signals with little degradation. The characteristics of TFML

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interconnections and their benefits relative to other interconnection technologies are described below.

7.2.1 Packaging Structures Using TFML Interconnections

There are a variety of ways to incorporate TFML interconnections into multichip packaging structures. Figure 7-1 shows three basic approaches. The thin films may be patterned on a blank substrate mounted in a second level package such as a perimeter leaded flat pack (middle approach in Figure 7-1). Electrical connections (such as wire bonds) are made between the substrate and the package, and the package then may be hermetically sealed. Alternatively, the TFML interconnections may be patterned on a multilayer ceramic substrate that contains pins or leads, power and ground distribution layers and sealing structures. In this approach the substrate serves as the package body. In the third option, the thin films are patterned on a large substrate used like a PWB for interconnecting bare or packaged ICs. This is essentially an extension of chip on board technology to much higher interconnection densities.

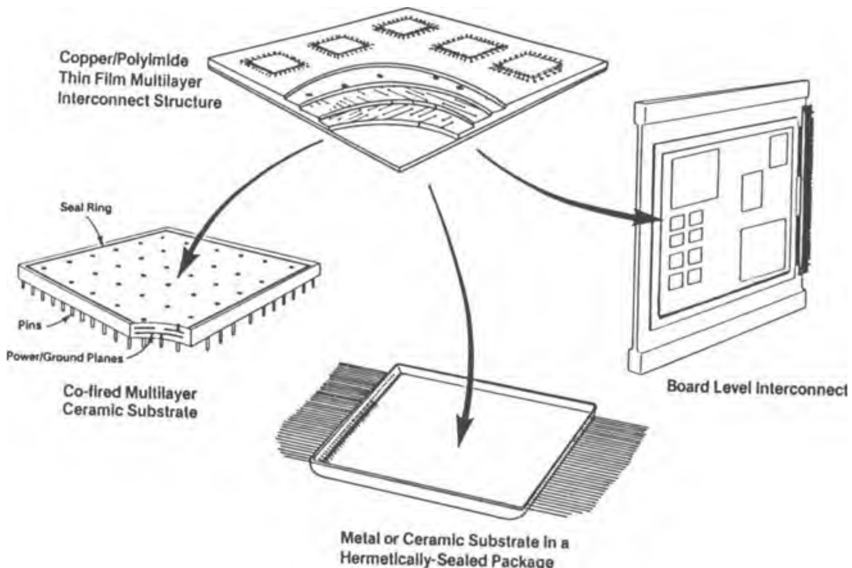

Figure 7-1 Implementation of TFML interconnections in IC packaging structures.

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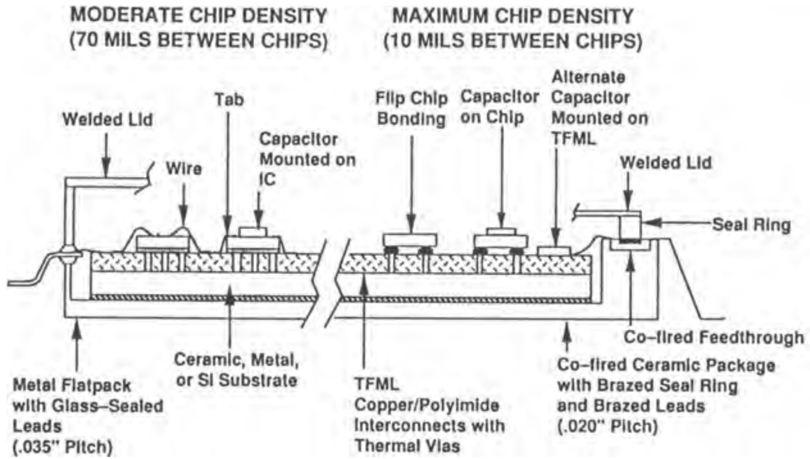

Figure 7-2 Cross section of an MCM containing a TFML interconnecting substrate, showing several options for IC bonding and package materials.

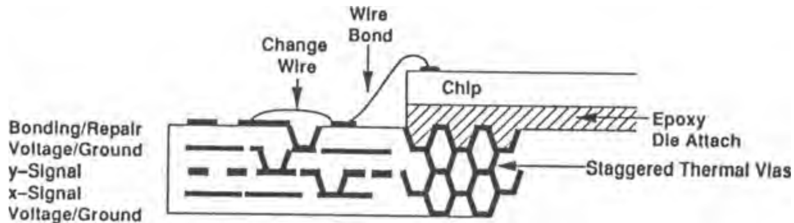

Figure 7-3 Detailed cross section of thin film layers on a TFML interconnect substrate.

Figure 7-2 is a cross section representing several different options for bonding chips and mounting TFML substrates into a second level package. The chips may be attached and bonded to the TFML substrate using a variety of technologies (refer to Chapter 9): Au or Al wire bonding, tape automated bonding (TAB) with face up or face down chips or flip chip solder bonding. Flip chip bonding provides the closest spacing between chips.

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Figure 7-3 shows a detailed cross section of the thin film layers. A dense array of vias (similar to electrical vias) may be provided beneath the die attach pad to promote the conduction of heat to the substrate (discussed in Section 7.5). For flip chip bonded ICs, most of the heat is removed from the backside of the ICs, although a significant amount of heat can be removed through the solder bumps and electrical vias to which they are attached.

7.2.2 Signal Line Characteristics

Layer Configuration

The signal interconnections are usually routed on two or more layers of orthogonally oriented conductor lines (x and y layers) as shown in Figure 7-3. Additional metal layers may be used to distribute power and ground voltages; these are essentially planes (solid or meshed) with low resistance and inductance. For high speed applications (generally > 100 MHz clock frequency or < 1 ns signal rise time), the interconnections are fabricated as transmission lines with controlled characteristic impedance, typically 40 - 60 Ω. Figure 7-4 shows the most common transmission line structures for TFML interconnections:

- **Microstrip** - with the signal line on top of the dielectric over a reference plane
- **Stripline** - with the signal line sandwiched between reference planes
- **Offset stripline** - with two signal layers offset symmetrically about the center line between reference planes

The offset stripline is used in most high speed applications because it eliminates one reference plane, provides uniform impedance and protects against crosstalk (noise coupling between adjacent signal lines). A common structure for lower speed applications is the buried microstrip, which has two layers of signal lines above one or more adjacent power planes. This structure is somewhat easier to fabricate, and the capacitance between adjacent power planes provides some noise decoupling.

Electrical Characteristics

Characteristic Impedance. The electrical characteristics of the signal interconnections are related to their geometry and material properties. If we assume the interconnections are lossless (have negligible resistance), the

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characteristic impedance (Z_o) of the stripline [1] shown in Figure 7-4 is given by Equation 7-1:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{(1 - \frac{t}{b})}{\frac{w}{b} + \frac{1}{\pi}\left\{2 \ln\left[\frac{1}{1 - t/b} + 1\right] - \frac{t}{b} \ln\left[\frac{1}{(1 - t/b)^2} - 1\right]\right\}} \quad (7\text{-}1)$$

where ε_r is the relative dielectric constant of the dielectric material, and b, t and w are the dielectric thickness, conductor thickness and conductor linewidth, respectively. Equation 7-1 is valid for $w/(b-t) < 0.35$ and $t/b < 0.25$. In reality, TFML interconnections are usually somewhat lossy and Z_o is frequency dependent. (Refer to Chapter 11 for a more detailed discussion of electrical characteristics.) However, Equation 7-1 is still useful for seeing the effects of geometrical parameters on Z_o. A high Z_o requires a low dielectric constant, a large dielectric thickness, and a small conductor cross section (small t/b and w/b). In general, these geometries require high aspect ratio structures (high thickness/width). A high Z_o (> 40 Ω) is usually required to maintain low power dissipation and delay in driver circuits, low switching noise and high noise tolerance [2]; conventional values of Z_o are 50 - 60 Ω.

Resistance The DC resistance of an interconnection line is given by Equation 7-2:

$$R = \frac{\rho L}{w t} = R_s \frac{L}{w} \quad (7\text{-}2)$$

where ρ is the conductor resistivity, R_s is the sheet resistance and L is the length of the interconnection. For low resistive losses, the conductor should have low resistivity and the signal lines should be short with a large cross section (wt). Since the linewidth must be narrow for high wiring density, low resistance interconnects require a large conductor thickness and thus a large aspect ratio (t/w).

At high frequencies, the current is forced out of the center of the conductor toward the surfaces adjacent to the nearest ground plane, a phenomenon known as skin effect. The depth at which the current has decreased to 1/e of its density at the surface is called the skin depth, defined as $\delta = \sqrt{(\rho/\pi f \mu)}$, where f is the frequency and μ is the conductor permeability (1.26×10^{-6} H/m for

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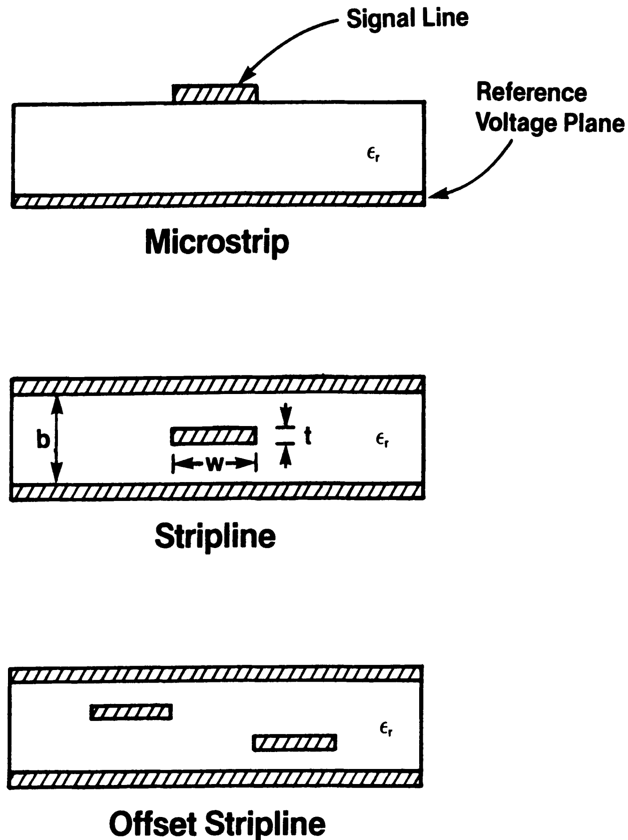

Figure 7-4 Transmission line structures for TMFL interconnections.

nonmagnetic conductors). For Cu, the skin depth is 2 μm at 1 GHz. When the skin depth is less than the conductor thickness, the AC resistance of the line is greater than the DC resistance, resulting in dispersion and degradation of short rise time signals. The skin effect may be a concern also if an interface metal (discussed in Section 7.3.2) with high resistivity is used around the primary conductor. If the thickness of the interface metal is a significant fraction of the skin depth (more than a few hundred nm), most of the current will be conducted in the interface metal and the line will be more lossy than if the primary conductor were used alone.

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Capacitance and Propagation Delay. The capacitance per unit length of a lossless interconnect is given by Equation 7-3:

$$C = \frac{\sqrt{\varepsilon_r}}{c\,Z_o} \qquad (7\text{-}3)$$

where c is the speed of light in vacuum. Thus the geometries that produce a high characteristic impedance produce low interconnection capacitance. Low capacitance is desirable to minimize the RC delay time and the power required to charge an interconnection.

A final important characteristic is the propagation delay time of a lossless interconnection. The propagation delay per unit length (τ_{pd}) is the inverse of the phase velocity (v_p) of electromagnetic waves in the dielectric, as shown in Equation 7-4:

$$\tau_{pd} = \frac{1}{v_p} = \frac{\sqrt{\varepsilon_r}}{c} = 33\sqrt{\varepsilon_r}\ \text{ps/cm}. \qquad (7\text{-}4)$$

Propagation delay is minimized by keeping lines short and by using low dielectric constant materials (discussed in Section 7.3.1). The propagation delay is the minimum delay for a lossless line. RC charging time and resistive losses in the interconnection cause additional delay.

7.2.3 Interconnect Design Rules

TFML interconnections encompass a wide range of designs, making it difficult to define a typical set of design rules. Table 7-1 compares the materials, geometries and electrical characteristics of four TFML designs:

1. An interconnect technology developed at Honeywell for GaAs MCMs that has been characterized at frequencies up to 10 GHz [3],
2. An MCM-D substrate offered by Alcoa [4], based on the Advanced VLSI Package (AVP) developed at AT&T,
3. The technology used by DEC in the High Density Signal Carrier for the VAX-9000, described in Chapter 17, and
4. An MCM-D technology developed by IBM called VHSIC (VCOS chips on silicon technology) [5].

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Table 7-1 TFML Design Rules.

	Honeywell	Alcoa	DEC	IBM-VCOS
Substrate				
Material	99.5% Alumina	Silicon	Aluminum	Silicon
Size	2.5" - 5" square	6" round	6" round	100 mm round
Layer Construction	offset stripline	buried microstrip	offset stripline	offset stripline
# metal layers	5	5	5*	4
Conductor				
Material	Copper	Copper	Copper	Aluminum
Signal line geometries:				
Thickness (μm)	5	4	10	3
Linewidth (μm)	25	19-23	18	15
Line Pitch (μm)	100-125	50-75	75	25
Power plane thickness (μm)	5	2	18	3
Dielectric				
Material	Polyimide	Polyimide	Polyimide	Polyimide
Dielectric constant	3.5	3.4	3.5	3.5
Thickness (μm) §	15-25	6-12	25	2.5
Via diameter (μm)	25	20		8x8
Electrical Characteristics (Signal Lines)				
Sheet resistance (mΩ/sq)	3.5	4.5	1.7†	8.8†
Resistance (Ω/cm)	1.35	2.0, 2.4	1	5.9†
Capacitance (pf/cm)	1.2	1.0, 1.2	1.2	3.4†
Characteristic Impedance (Ω)	50	50,58	60	not controlled
Propagation delay (ps/cm) ‡	62	61	62	62
Via resistance (mΩ/via)	2.5	<5		
Insertion Loss (dB/cm)				
@2 GHz	-0.3			
@9 GHz	-0.9			

* signal core only
† calculated values from design geometries
§ signal line to nearest reference plane
‡ propagation delay for lossless line

Table 7-1 illustrates the wide range of materials and designs possible with TFML technology. Substrates include alumina, silicon and Al in both round and square shapes. Conductor materials include Cu and Al. There is a wide range

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in layer thickness, signal linewidth and pitch and electrical characteristics.

One of the most significant differences between TFML designs is the conductor line cross section and resulting electrical performance. For low speed systems (< 100 MHz), narrow linewidths of 10 - 15 μm and conductor thicknesses of 2 - 3 μm may be used. The VCOS technology is typical of this type of design. The small cross section of the signal lines (15 μm wide × 3 μm thick) and the Al conductor produce a relatively high DC resistance of 6 Ω/cm, which will significantly degrade high speed signals. The advantage of the narrow linewidth is that it permits high routing density (signal line pitch of 25 μm). The narrow lines also permit the dielectric layers to be relatively thin without producing high capacitance. The thin dielectric layers permit higher via density (although the VCOS technology has unusually thin polyimide layers).

For high speed systems (> 100 MHz), larger conductor cross sections are needed (5 - 10 μm thick × 18 - 25 μm wide) to reduce loss at high frequencies. A thicker dielectric is required to maintain low capacitance/high impedance. The result is a lower routing density of 50 - 125 μm, still adequate for most designs. The Honeywell and DEC designs are representative of this type of interconnection. Typical interconnect resistance for these geometries is 1 - 2 Ω/cm. The Honeywell design for striplines produced an insertion loss of 0.3 dB/cm at 2 GHz and 0.9 dB/cm at 9 GHz [3]. Since signal amplitude losses should be kept to less than ~1 dB, the interconnects for multi-GHz systems must be kept very short (< 1 cm), or long interconnects must have larger cross sections [6].

The Alcoa design rules achieve a compromise between relatively high speed and high interconnection density. These geometries will satisfy most MCM-D applications and are typical of most TFML designs. The Alcoa design uses a buried microstrip with two voltage planes below two signal layers. This produces a slightly different characteristic impedance on each signal layer, although the conductor linewidths can be adjusted to equalize the impedance on the two layers. A capacitance of > 0.7 nF/cm^2 is provided by using a dual silicon nitride/oxide dielectric between the power plane and conductive silicon substrate.

7.2.4 Comparison With Alternative Interconnection Technologies

Advantages of TFML Interconnections

Table 7-2 compares the characteristics of TFML interconnections with those of the primary alternative technologies: thick film screen printed multilayer structures (discussed in Chapter 6), high temperature cofired ceramic (HTCC - see Chapter 6) and laminated interconnections based on PWB technology (MCM-L - see Chapter 5). The advantages of TFML technology are apparent. First,

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Table 7-2 Comparison of MCM Interconnection Technologies.

	THIN FILM	THICK FILM	COFIRED CERAMIC[2]	LAMINATE
Conductor Material[1]	Cu (Al,Au)	Cu (Au)	W (Mo)	Cu
Thickness (μm)	5	15	15	25
Line width (μm)	10 - 25	100 - 150	100 - 125	75-125
Line pitch (μm)	50 - 125	250 - 350	250 - 625	150-250
Bond pad pitch (μm)	100	250 - 350	200 - 300	200
Max. # of layers	4 - 10	5 - 10+	50+	40+
Dielectric Material	Polyimide	Glass-ceramic	Alumina	Epoxy/glass
Dielectric Constant	3.5	6 - 9	9.5	4.8
Thickness/layer (μm)	25	35 - 65	100 - 750	120
Min. via diameter (μm)	25	200	100 - 200	300
Electrical Characteristics				
Propagation Delay (ps/cm)	62	90	102	72
Sheet Resistance (mΩ/□)	3.4	3	10	0.7
Line Resistance[3] (Ω/cm)	1.3 - 3.4	0.2 - 0.3	0.8 - 1	0.06-0.09
Stripline Capacitance[4] (pF/cm)	1.25	4.3	2.1	1.46

1 Primary conductor material; alternative materials in parentheses.
2 High temperature cofired ceramic
3 For range of line widths shown
4 For 50 Ω characteristic impedance line (minimum capacitance for thick film).

thin film structures provide higher interconnection density and a higher bond pad density. This is due to the thin film patterning processes, which can achieve much higher resolution and higher aspect ratios than the screen printing and hole punching processes used for thick film and cofired ceramic interconnections, or the through hole drilling and plating processes used in MCM-L. The laminated approaches (cofired ceramic and MCM-L) achieve high interconnection density by stacking a large number of layers. Eventually this process becomes more costly than the thin film approach. It also may be prohibited by height or weight limitations. The thin film technology is the only one that can match the finest bond pad pitch used on ICs (~100 μm). Other technologies require a fanout or double row of bond pads on the substrate, reducing the chip packing density.

The TFML interconnections achieve the best high speed performance due to the material properties and high aspect ratio patterning. Low temperature

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deposition processes, such as sputtering and plating, permit the use of high conductivity metals (such as Cu and Al) as opposed to the low conductivity refractory metals (W and Mo) used in HTCC. For typical conductor thicknesses of 3 - 8 μm, the high conductivity metals produce a low sheet resistance of 2 - 6 mΩ/square, versus 10 mΩ/square in cofired ceramic. This results in lower voltage drops and less switching noise on power distribution planes. The high conductivity metals also produce low resistivity for narrow signal lines (Equation 7-2). (Low resistivity is obtained in MCM-C and MCM-L by using wider lines at the expense of routing density.) Lines with low resistivity cause less degradation in signal amplitude and rise time. The polymer dielectrics used in TFML interconnections have a significantly lower dielectric constant than typical HTCC or thick film glass-ceramics. The low dielectric constant enhances high speed performance by reducing propagation delay (Equation 7-4), interconnect capacitance (Equation 7-3) and crosstalk between closely spaced signal lines.

The thin film approach is more versatile than the other interconnection technologies because the multilayer structures can be fabricated on a wide variety of substrates and incorporated into a variety of package designs. High thermal conductivity substrates such as metals, aluminum nitride (AlN), or even diamond may be used for applications requiring high thermal dissipation. Substrates that match the coefficient of thermal expansion (CTE) of silicon (including silicon itself) may be used to improve the reliability of flip chip bonded ICs. Silicon substrates with active driver circuits or passive resistor or capacitor structures also may be used.

Finally, TFML technology is extendable to even higher interconnection density and speed. A number of thin film interconnection systems are being evaluated for multi-GHz digital applications [5]. The material system is also compatible with some planar optical waveguide approaches and may even be extended to thin film superconductor interconnections (discussed briefly at the end of Chapter 2 and this Chapter).

Issues

In spite of numerous advantages that are widely recognized, thin film interconnections are being implemented more slowly than initially expected. This can be attributed to a variety of factors: high costs, an unstable vendor base, a lack of standardized designs and materials, an inadequate infrastructure for MCM design and test, and continual improvements in competing MCM technologies. Due to the use of polymer dielectrics, with insufficient life cycle and field performance data, the thin film systems are generally seen as risky and less robust toward assembly processes than more established technologies such as cofired ceramic. These factors must also be considered in selecting an MCM technology. The tradeoffs are discussed in more detail at the end of this chapter.

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7.3 MATERIALS FOR THIN FILM INTERCONNECTION SYSTEMS

7.3.1 Substrate Materials

Substrate Requirements

TFML interconnections can be fabricated on a wide variety of substrates, including metals, ceramics and silicon wafers. The selection of a substrate material is dictated by a combination of thermal, mechanical and processing considerations and is also dependent on the second level package design. However, there are some universal requirements or desirable characteristics for all substrates.

The substrate should have high thermal conductivity to dissipate heat generated by ICs. The substrate should also have a high flexural strength to avoid fracture. A lightweight (low density) substrate is obviously desirable for MCM applications such as airborne or space-based systems or medical implants.

The CTE of the substrate is dictated by several considerations. If the substrate is mounted in a second level package, its CTE should match that of the package material. It may also be important for the substrate CTE to match that of silicon (2.3 - 3.5 ppm/°C) to avoid excessive stress in the die attach material or flip chip bonds for large die. Finally, the substrate CTE should match that of the dielectric, especially for polymer dielectric materials. As the polymer film cools from the cure temperature or glass transition temperature, the CTE mismatch causes stress (usually tensile) in the polymer film, resulting in bowing of the substrate. The bowing can complicate photolithographic patterning and the bonding of the substrate into a second level package. It can be shown (refer to equations in Chapter 16) that the camber warpage of the substrate, B, is given by Equation 7-5:

$$B = \left[\frac{d^2}{4}\right]\left[\frac{3\,t_f}{t_s^2}\right]\left[\frac{E_f}{E_s}\right]\left[\frac{1 - \upsilon_s}{1 - \upsilon_f}\right](\alpha_f - \alpha_s)(T_c - T_r) \tag{7-5}$$

where d is the substrate diameter or diagonal, t_f and t_s are the thickness of the dielectric film and substrate, respectively, E_f and E_s are the Young's modulus of the film and substrate, υ_f and υ_s are Poisson ratios, α_f and α_s are CTEs of the film and substrate, T_c is the cure temperature (or glass transition temperature if lower than the cure temperature) and T_r is the room or point of use temperature.

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The camber increases linearly with dielectric film thickness and depends on the square of substrate diameter/thickness. A substrate with a high modulus (E_s) and a CTE matched to the dielectric will experience less bowing.

From a fabrication standpoint, the substrate must be inert to all of the process chemicals (including both wet etchants and plasma gases) and temperatures (typically up to 450°C) used in TFML processing. For photolithographic processes the substrate must be flat (typically less than 50 - 100 μm total camber) and the surface must be smooth (typically less than 0.1 - 0.2 μm average roughness) and free of defects. Lapping or grinding is often required to achieve sufficient flatness in ceramic or metal substrates. Lapping removes material by rubbing the substrate against a slurry of relatively large abrasive particles; this produces a rough surface that may require polishing with smaller particles to achieve an acceptable surface roughness. The substrate must be machineable, since it is often cut to the final size or diced into multiple circuits. Finally, an inexpensive substrate available from multiple vendors is considered ideal. Table 7-3 lists some candidate substrate materials with their thermal and mechanical properties.

Ceramic Substrates

Ceramics, particularly alumina, are among the most frequently used substrate materials. This is partly an outgrowth of their use in thick film and single layer thin film hybrid circuits (refer to Chapter 6). The hybrid industry has provided an infrastructure for fabricating and machining (lapping, polishing, laser scribing etc.) high quality ceramic substrates. Most ceramics also have the advantage of being electrical insulators. This permits metal layers to be patterned directly on the substrate without an insulating film. The insulating substrate also can have internal metal layers or feedthroughs to the backside of the substrate. The main drawback to ceramics is the warped, rough surface of as-fired substrates. Ceramics can be lapped to an acceptable flatness, but lapping increases the surface roughness and exposes voids in the grain structure that can cause defects in thin film patterns. Ceramics with larger grains, generally, will have larger voids. After lapping, the surface can be polished to a near mirror smoothness (~10 nm average roughness). However, voids will still be present after polishing; their size and density must be minimized. A layer of polyimide is sometimes used on the ceramic substrate to fill the voids and produce a smooth surface for metal patterning.

Ceramic substrates can be fabricated by tape casting, hot pressing or injection molding. Multilayer structures are fabricated by the lamination and cofiring processes described in Chapter 6. Internal metal layers in the multilayer ceramic can be used to distribute power or to provide interconnection to external leads. In addition, metal features such as seal rings, perimeter leads or pins can

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Table 7-3 Properties of Substrates for TFML Interconnections.

MATERIAL	DENSITY (g/cm^3)	CTE (ppm/K)	YOUNG'S MODULUS (GPa)	THERMAL CONDUCTIVITY (W/m-K)
Polyimide	1.4	40	2.5	0.15
Si	2.3	2.6	113	148
Al_2O_3 (99.6%)	3.9	6.3-6.7	360	20-35
Al_2O_3 (92% cofired)	3.6	6.7	275	17-20
BeO (99.5%)	3.0	6.9	350	251
AlN	3.3	4	340	160-190
SiC	3.1	3.7	400	270
Mo	10.2	4.9	324	138
Cu	8.9	16.8	110	398
Al	2.7	2.5	62	237
Au	18.9	14.3		318
Steel (AISI 1010)	7.9	11.3	192	64
Kovar (Fe/Ni/Co)	8.4	6.1	138	16
Cu/Invar/Cu (20/60/20)	8.4	6.4	134	170
Cu/Mo/Cu (20/60/20)	9.7	7	248	208
Cu/Mo/Cu (13/74/13)	9.9	5.7	269	242
CuW (20/80)	17	8	283	186
Natural Diamond	3.5	1.1		2000
CVD Diamond	3.5	1.5-2.0	890-970	400-1600

Notes:
- All properties at 25°C or 300 °K.
- Thermal conductivity is for lateral conduction (for clad materials).

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be brazed to metal pads on the ceramic.

The most widely used ceramic is alumina (Al_2O_3). Al_2O_3 has a high modulus, a high strength-to-weight ratio, is chemically and thermally stable and is a good insulator. The main drawback to Al_2O_3 is its relatively low thermal conductivity. The highest quality Al_2O_3 substrates are fabricated by tape casting, which can produce a 99.5 - 99.9% Al_2O_3 material with a small grain size (1 - 3 μm). Tape casting typically produces an average surface roughness of 75 - 200 nm and a camber of about 10 - 30 μm/cm after firing. Tape cast Al_2O_3 can be lapped to a flatness of < 10 μm/cm and polished to a surface roughness of 10 nm. These techniques produce acceptable void sizes and an excellent surface for subsequent thin film processing.

Cofired Al_2O_3 is typically 92% Al_2O_3, resulting in a lower thermal conductivity and modulus than tape cast Al_2O_3. The cofired material has a larger grain size and therefore greater surface roughness and larger voids than tape cast Al_2O_3. After firing, the camber is typically 30 μm/cm, so lapping is usually required. The voids produced by lapping and polishing can be 10 μm or greater in diameter and may limit the feature sizes that can be patterned directly on the substrate. A smoothing layer of polyimide is required for critical feature dimensions less than about 20 μm.

Alternative ceramics with significantly higher thermal conductivity than Al_2O_3 have been developed. The most prominent alternatives are beryllia (BeO), aluminum nitride (AlN) [7] and silicon carbide (SiC). AlN and SiC have a low CTE that is closely matched to silicon. The main drawback to AlN is the difficulty in achieving good metal adhesion; it cannot form the metal oxide bonds that are usually involved in metal adhesion. AlN also has a larger grain size than tape cast alumina and therefore larger voids in the surface. SiC has a very high modulus of elasticity and excellent thermal conductivity. Furthermore, SiC can be polished to an excellent surface finish. However, it has a high dielectric constant which may preclude the patterning of signal lines directly on the substrate. A significant drawback to both AlN and SiC is their limited availability and the lack of industry experience with the materials. The main drawback to BeO is the health risk posed by airborne particles, which complicates machining processes.

BeO and AlN can be fabricated into multilayer structures, although the multilayer system for AlN is still in a developmental stage. Alternative multilayer ceramics such as glass-ceramic mixtures [8] and mullite [9] (refer also to Chapter 6) have been used as substrates for thin film interconnections. Their main advantages are a close CTE match to silicon and good dielectric properties (low ε_r) for internal interconnect layers. Their main drawback is low thermal conductivity.

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Metal Substrates

A variety of metals may be used as substrates for thin film interconnections. In general, the advantages of metal substrates are high thermal conductivity and relatively low cost. Because the metal substrate is electrically conductive, an insulator is required beneath the first patterned metal layer. (Note that a conductive substrate may provide a good ground plane.) Also, since metal substrates are reactive toward many of the metal etchants used in TFML processing, protective coatings may be required on the backside of the substrate. The flatness and surface roughness of metal substrates varies greatly and depends on the method of fabrication. However, most metals can be heat flattened, ground, lapped and/or polished to produce an excellent surface for thin film patterning.

Al and Cu substrates have excellent thermal conductivity. They are also inexpensive and are easily machineable. Al has the additional advantage of light weight. A disadvantage of Al and Cu is that they are quite reactive toward common metal etchants. These metals also have a much lower modulus than the ceramics and a high CTE that is poorly matched to silicon. DEC has used Al as a temporary substrate that is etched away after fabricating copper/polyimide TFML interconnection structures or power planes in their VAX-9000 Multichip Unit (refer to Chapter 17).

Molybdenum (Mo) and tungsten (W) are attractive metal substrates because of their high modulus of elasticity and low CTE. However, these metals are quite heavy and difficult to machine. Molybdenum is frequently used as a heat spreader and as a CTE buffer in high power devices.

Desirable properties may be produced in metal substrates by alloying or cladding a combination of materials. Cu clad and nickel clad Mo, produced by hot roll pressing, combine the high modulus and low CTE of Mo with the high thermal conductivity of Cu or the solderability of nickel [10]. Cu/W alloys (typically 10 - 20% Cu), produced by powder metallurgy, also achieve a high modulus, low CTE and high thermal conductivity. However, they are heavier and more difficult to machine than clad Mo. The CTE of these materials may be tailored by varying the Cu composition (for Cu/W) or the relative thickness of the Mo and cladding layers.

Silicon and Diamond Substrates

Silicon is an attractive substrate because it has a relatively high thermal conductivity and a perfect CTE match to silicon die. More importantly, silicon wafers are widely available in standardized sizes that are adaptable to IC process equipment. They also have a defect free polished surface that is excellent for thin film processing. For these reasons, silicon has been used widely in MCM-D

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systems, as discussed in Chapter 16. An additional advantage of silicon is the possibility for directly fabricating active driver circuits or passive devices on the substrate. The passive devices, such as implanted resistors or thin film capacitors, are relatively straightforward to fabricate. For silicon substrates with active devices, it is argued that thermal performance is enhanced by fabricating high power driver circuits in the substrate and that different circuit technologies can be used in the substrate and ICs. However, complex processes (including dopant implantations and isolation structures) are required to fabricate the active devices. It is debatable whether this is an economical use of processed silicon area.

The main drawback to silicon is its low modulus and low CTE, resulting in significant warpage when conventional high CTE polyimides are used as a dielectric material. 50 μm of high CTE polyimide (35 ppm/°C) deposited on a Si wafer 100 mm diameter × 0.5 mm thick (standard thickness) will cause over 500 μm of bowing; the wafer must be 1.4 mm thick to maintain an acceptable camber of < 75 μm. This phenomenon has been a major driver in the development of low CTE polyimides that match the CTE of silicon.

Recently, synthetic diamond has been investigated as a substrate material for thin film interconnect systems because of its extremely high thermal conductivity, as high as 1600 W/m-K (four times that of Cu) [11]. Diamond also has the advantages of a very high modulus and a good CTE match to silicon. There is a high level of activity in fabricating polycrystalline synthetic diamond, primarily through plasma-enhanced chemical vapor deposition processes. Substrates as large as 150 mm in diameter and 1 mm thick are being produced with large crystal sizes and excellent optical and thermal properties. However, these substrates are very expensive; to be marketable the diamond growth rate must increase and the production cost must decrease.

7.3.2 Conductor Materials

The conductor material system for TFML interconnections consists of the primary current-carrying conductor, various interface metals for adhesion and/or diffusion barriers, and top layer metals that are compatible with the assembly process. The requirements and options for each of these materials is different.

Primary Conductor

While many conductor materials may be used for signal interconnection and power distribution, TFML technologies use the highest conductivity metals that are stable and processable, namely, Cu, Al and Au. Copper has the highest electrical conductivity (0.596×10^6 S/cm) and high thermal conductivity. Cu is

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also inexpensive. It can be deposited by sputtering or by low cost electroplating processes, and is readily wetted by lead/tin solders. However, Cu has poor adhesion to polyimide. Furthermore, when polyamic acid (a precursor to polyimide) is deposited on Cu, the Cu is oxidized and forms precipitates that migrate several microns into the polyimide during curing [12]. For this reason, it is necessary to have adhesion/barrier metal layers between the Cu and certain polymer dielectrics.

Au has the advantages of high electrical conductivity (0.452×10^6 S/cm), excellent corrosion resistance and good compatibility with assembly processes such as wire bonding. It requires adhesion metals due to its weak interaction with polymer dielectrics. However, Au is prohibitively expensive for most MCM applications. It is more commonly used as a top layer metal (discussed later).

Al has been widely used as a conductor material because the semiconductor industry has extensive experience in depositing and patterning Al (or Al-4% Cu alloys) for IC interconnections. Also, Al has relatively good adhesion to polymer dielectrics. This simplifies the processing by eliminating adhesion metals. The biggest drawback to Al is its low electrical conductivity (0.377×10^6 S/cm, about 60% of the conductivity of Cu), which limits the high speed performance of interconnections.

To summarize the choices in selecting a conductor material: Al is preferred for low cost and low speed applications; Cu is preferred for the highest speed applications, and Au may be used occasionally where the highest reliability is required. Because of its extendability to future high speed applications, Cu is the conductor material most widely used in the industry.

Interface Metals

Interface metals are used to achieve good adhesion between the primary conductor (particularly Cu) and the polymeric dielectric, or to prevent chemical attack of the metal or interdiffusion of metals. The most frequently used interface or barrier metals include chromium (Cr), titanium (Ti), 10% Ti/90% W, nickel (Ni) and Mo. Most of the barrier metals are deposited by sputtering to a thickness of 20 - 200 nm. The polymer interface studied most widely is polyimide.

Cr has excellent adhesion to polyimide, even after temperature/humidity aging. There is extensive reliability data for the Cr/Cu/Cr material system used by IBM and others in thin film interconnections. However, because Cr interacts so strongly with polyimide, it may leave a conductive residue after being etched. (The correct etch process eliminates this residue.) Ti also has excellent adhesion to polyimide and is easily etched. However, its conductivity is somewhat lower than Cr. TiW has good adhesion and is a common diffusion barrier for gold metallization. However, TiW is prone to being deposited with high internal

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