

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00387
Patent 8,841,778 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and
FRANCES L. IPPOLITO, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively “Petitioner”) filed a Petition for *inter partes* review of claims 1, 2, 8, 14, 31, 32, 44, 46, and 52–54 of U.S. Patent No. 8,841,778 B2 (Ex. 1001, “the 778 patent” or “the challenged patent”). (Paper 1, “Pet.”). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition (Paper 10, “Prelim. Resp.”).

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Upon consideration of the information presented in the Petition and Preliminary Response, we determine that the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of claims 1, 2, 8, 14, 31, 32, 44, 46, and 52–54 (“the challenged claims”).

A. *Related Proceedings*

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 8 (Patent Owner’s Mandatory Notices). Petitioner indicates that the challenged patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

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Additionally, patents related to the challenged patent are the subjects of petitions filed in IPR2016-00386 (U.S. Patent No. 8,653,672), IPR2016-00388 and IPR2016-00393 (U.S. Patent No. 7,193,239); IPR2016-00389 (U.S. Patent No. 8,035,233); IPR2016-00390 (U.S. Patent No. 8,629,542); IPR2016-00391 (U.S. Patent No. 8,796,862); IPR2016-00394 (U.S. Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (U.S. Patent No. 8,928,119); IPR2016-00691 (U.S. Patent No. 7,474,004); IPR2016-00703 (U.S. Patent No. 8,791,581); IPR2016-00706 (U.S. Patent No. 8,791,581); IPR2016-00786 (U.S. Patent No. 8,933,570); IPR2016-00708 (U.S. Patent No. 8,907,499); and IPR2016-00770 (U.S. Patent No. 8,907,499).

B. Time Bar under 35 U.S.C. § 315(b)

Patent Owner argues that Petitioner is time-barred under 35 U.S.C. § 315(b) because two of the real-parties-in-interest, Samsung Austin Semiconductor, LLC (“SAS”) and Samsung Semiconductor, Inc. (“SSI”), were served with a complaint alleging infringement of the challenged patent on December 24, 2014. Prelim. Resp. 5–10; *see* Pet. 1 (identifying real parties-in-interest). Patent Owner contends that the Petition was filed on December 28, 2015, which was four days after the statutory one year period for SAS and SSI had expired. *Id.* at 6; *see* Paper 5 (According filing date of December 28, 2015 to the Petition).

In the Petition, Petitioner explained that it filed its Petition on December 28, 2015 because the Office considered December 22–24, 2015, to be a “Federal holiday within the District of Columbia” pursuant to 35 U.S.C. § 21. Pet. 3. On December 22, 2015, the Office experienced a major power outage at its headquarters in Alexandria, Virginia, resulting in

damaged equipment that required the subsequent shutdown of many USPTO online and information technology systems. On December 28, 2015, the Office announced that

[i]n light of this *emergency situation*, the USPTO will consider each day from Tuesday, December 22, 2015, through Thursday, December 24, 2015, to be a “Federal holiday within the District of Columbia” under 35 U.S.C. § 21 and 37 C.F.R. §§ 1.6, 1.7, 1.9, 2.2(d), 2.195, and 2.196. Any action or fee due on these days will be considered as timely for the purposes of, e.g., 15 U.S.C. §§ 1051(b), 1058, 1059, 1062(b), 1063, 1064, and 1126(d), or 35 U.S.C. §§ 119, 120, 133, and 151, if the action is taken, or the fee paid, on the next succeeding business day on which the USPTO is open (37 C.F.R. §§ 1.7(a) and 2.196).

Ex. 3001 (emphasis added). Section 21(b) states that “[w]hen the day, or the last day, for taking any action or paying any fee in the United States Patent and Trademark Office falls on Saturday, Sunday, or a federal holiday within the District of Columbia, *the action may be taken, or the fee paid, on the next succeeding secular or business day.*” Emphasis added.

Petitioner has complied with the requirements of § 315(b) given the circumstances of the power outage during the December 22–24, 2015 period and the announcements by the Office regarding the same. December 28, 2015, which was a Monday, was the next succeeding business day after December 24, 2015, because Friday, December 25, 2015, was a federal holiday. Moreover, we disagree with Patent Owner’s arguments that the Office lacks the authority to treat December 22–24, 2015 as federal holidays. *See* Prelim. Resp. 7–8.

C. The Challenged Patent

The challenged patent relates generally to a three-dimensional structure (3DS) for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

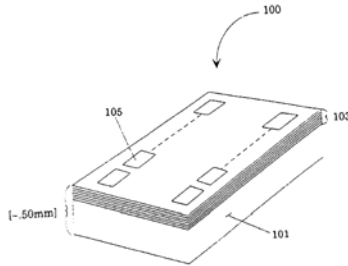


Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all circuit layers. *Id.* at 3:66–4:3. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:19–21. The challenged patent discloses that “each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:24–27. The challenged patent further discloses that the “thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm²) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.” *Id.* at 8:47–52.

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