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Class / Subclass:	361/760	Patent Number:	-
First Named Inventor:	Glenn J. Leedy , Parkland, FL (US)	Issue Date of Patent:	-

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Title of Invention: Three dimensional structure memory

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

RESPONSE

Sir:

Responsive to the prior Office Action, please amend this application as follows.

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REMARKS

The prior Office Action has been carefully considered. Reconsideration in view of the foregoing amendments and the present remarks is respectfully requested.

The undersigned thanks Examiner Chen for courtesies extended during the telephone interview of May 31, 2012. The claims have been amended to recite in part a substrate that "extends throughout at least a substantial portion of the area of an integrated circuit die." As discussed in greater detail below, no such feature, in combination with the other claimed features, is believed to be taught or suggested by the cited references. Support for the amendment is also set forth.

New claims 53-58 have been added. Of these, independent claims 56, 57 and 58 correspond generally to claims 1, 8 and 21, respectively. The newly added claims recite first and second circuit layers bonded to one another. In other respects, many of the recited features are the same as features recited in claims 1, 8 and 21.

Compliance With 35 USC Sections 102 and 103

Claims 1-52 were rejected as being anticipated by or unpatentable over Leedy. The claims have been amended to more clearly distinguish over the cited reference. Reconsideration is respectfully requested.

During the telephone interview, contrast was drawn between the present invention as shown in Figure 1d of the present specification, for example, and the primary reference (Leedy).

In particular, in the Figure 8 stacking embodiment of Leedy (described in the paragraph bridging columns 15 and 16), the semiconductor substrate is removed. What remains is a dielectric membrane (160a, 160b, 160c) having islands of semiconductor material embedded therein. Semiconductor devices 162, 164, 166 are formed in the islands of semiconductor material, and interconnections are made between the devices of

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a given layer and between devices of different layers. The "islands of semiconductor" having only one or a few circuit devices, which goes to the intent of the invention which is to isolate the electrical coupling between circuit devices. Note, for example, column 10, lines 9-18 of Leedy:

> The low stress dielectric membrane formed on the semiconductor substrate (along with interconnect metallization) becomes the only structural circuit membrane component after *the semiconductor substrate portion of the membrane is etched or trenched into independent semiconductor devices*. An additional layer (not shown) of low stress dielectric over the interconnect metallization may be applied for passivation and to increase the thickness of the resulting membrane 20 to achieve a specific desired level of durability. (Emphasis added)

In Figure 1d of the present specification, by contrast, circuit layers are formed from substrates 103a, 103b including a substrate made from a semiconductor wafer. As now recited in independent claims 1 and 8, at least one of the substrates is "extends throughout at least a substantial portion of the area of the integrated circuit die." That is, throughout at least a substantial portion of the area of the integrated circuit die, there are no "islands of semiconductor" whereby individual circuit devices or small groups of same are isolated.

In the Leedy reference, by action of the etching or trenching described, what was the semiconductor substrate ceases to be a substrate, i.e., a continuous stratum. Hence, the feature of a substrate that is "extends throughout at least a substantial portion of the area of the integrated circuit die" is absent from, and not taught or suggested by, Leedy.

The foregoing feature has not been recited in claim 21. However, claim 21 has been amended to recite in part "at least one vertical conductive path that passes vertically through at least one of the first substrate and the second substrate and is insulated from the substrate by a non-conductive material having a stress of 5 x 10^8 dynes/cm^2 or less." No such feature is believed to be taught or suggested by Leedy. In particular, in Leedy, vertical interconnects pass through a dielectric matrix that surrounds the multitude of device islands. The vertical interconnects do not pass through a semiconductor substrate nor are they insulated from that substrate.

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Accordingly, claims 1-52 are believed to patentably define over Leedy.

Compliance With 35 USC Sections 112 Second Paragraph

The Office Action took the position that the addition of the word "monocrystalline" to the claims introduced new matter. Applicant respectfully disagrees. Nevertheless, "monocrystalline" has been deleted.

In the present amendment, the claims have been amended to recite in part a substrate that extends throughout a substantial portion of the area of an integrated circuit die. Such addition is believed to be clearly supported by the specification. The specification makes clear that in one embodiment, a thick, processed semiconductor wafer of a standard, well-known type (for example 500 microns thick) is thinned to 50 microns or less in thickness (Method A, 3DS Memory Device Fabrication Sequence, specification pages 14-17; specification, page 12, first full paragraph). The thick semiconductor wafer clearly extends throughout the area of an integrated circuit die—it is a single piece of material. When it is thinned to 50 microns, it remains a single piece of material. This nature of the thinned semiconductor substrates may be observed, for example, in Figure 1d with respect to substrates 103a, 103b and 103c.

Compliance With 35 USC Section 101 and Section 112 Second Paragraph

Claims 38, 40 and 42 were object to as being duplicates. Claims 41, 43, and 45 were likewise objected to as being duplicates. The present amendments eliminate duplication by changing dependencies and canceling selected claims.

Although not mentioned in the Office Action, in the interview, the Examiner raised a question as to whether limitations in an apparatus claim directed to process steps previously performed on elements of the apparatus claim (for example "polished," "thinned") were proper. Incidentally, the word "polished" occurs in the claims of upwards of 8,000 patents, and the word "thinned" occurs in the claims of upwards of 3,000 patents.

The present claims are very different than the kind of impermissible "hybrid" claims that case law disallows. That type of disallowed hybrid claim sets forth both an

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apparatus and a method of using the apparatus. The present claims, on the other hand, merely specify particulars of the claim elements of the apparatus. Applicant is not aware of any case that forbids an apparatus claim from specifying elements partly in terms of preparatory steps carried out on those elements.

To take a hypothetical example, the element "a sintered brake pad" requires that the brake pad have been sintered. (Not surprisingly, the word "sintered" occurs in the claims of numerous issued patents over the period of 1976 to 2012--16,647 patents, to be exact. It may be expected to occur in the claims of equally numerous patents prior to 1976.) Sintering is a process in which a powdered material is made to coalesce into a solid or porous mass by heating it (and usually also compressing it) without liquefaction. This type of claiming has long been allowed and is clearly distinguishable from recent cases addressing hybrid claims, which have never been allowed.

Accordingly, withdrawal of the rejections and allowance of the claims is respectfully requested.

Respectfully submitted,

/MichaelJUre/

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Michael J. Ure, Reg. 33,089

Dated: 7/2/2012

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