

[54] METHOD OF MAKING AND TESTING AN INTEGRATED CIRCUIT

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[51] Int. Cl.<sup>5</sup> ..... H05K 3/30

[52] U.S. Cl. .... 29/832; 29/407; 29/846

[58] Field of Search ..... 437/8; 324/73 PC; 29/846, 832, 407, 593

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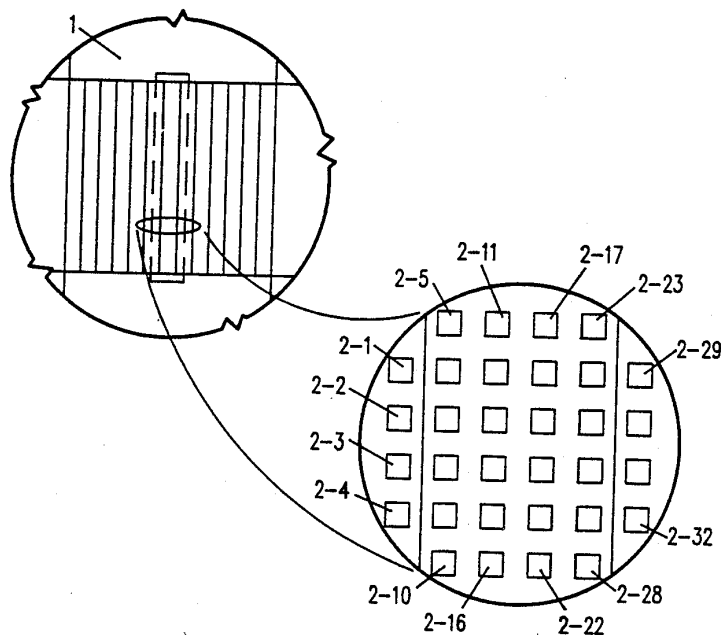
Primary Examiner—Carl J. Arbes  
Attorney, Agent, or Firm—Skjervén, Morrill, MacPherson, Franklin & Friel

[57] ABSTRACT

Each transistor or logic unit on an integrated circuit wafer is tested prior to interconnect metallization. By CAD means, the transistor or logic units placement net list is revised to substitute redundant defect-free logic units for defective ones. Then the interconnect metallization is laid down and patterned under control of a CAD means. Each die in the wafer thus has its own interconnect scheme, although each die is functionally equivalent, and yields are much higher than with conventional testing at the completed circuit level.

The individual transistor or logic unit testing is accomplished by a specially fabricated flexible tester surface made in one embodiment of several layers of flexible silicon dioxide, each layer containing vias and conductive traces leading to thousands of microscopic metal probe points on one side of the test surface. The probe points electrically contact the contacts on the wafer under test by fluid pressure. The tester surfaces traces are then connected, by means of multiplexers, to a conventional tester signal processor.

20 Claims, 16 Drawing Sheets



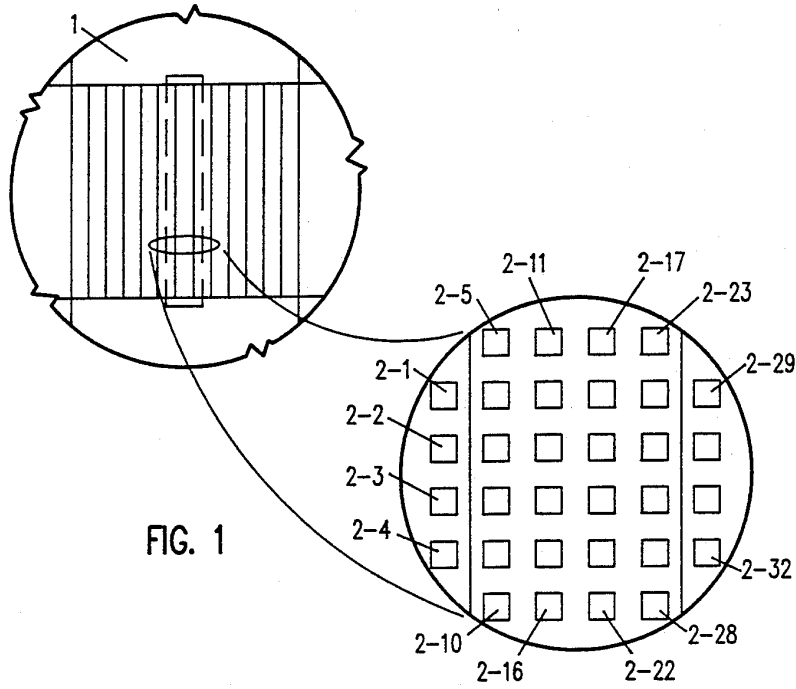


FIG. 1

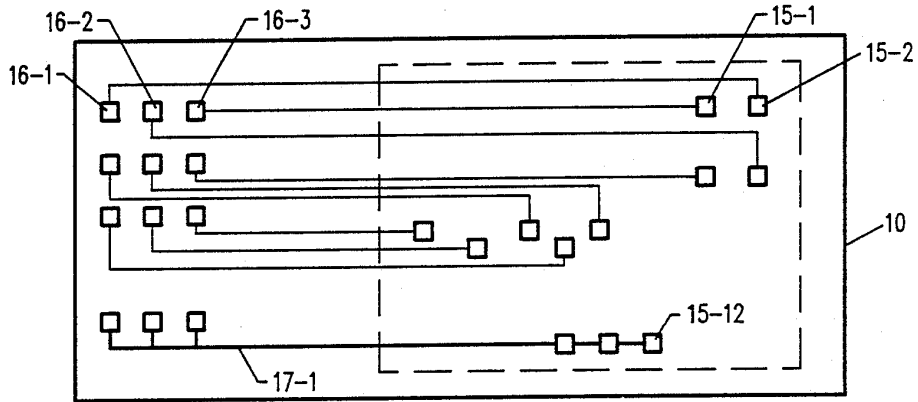


FIG. 2

TESTER CONNECTION ARRAY  
TESTER CONNECTION ARRAY

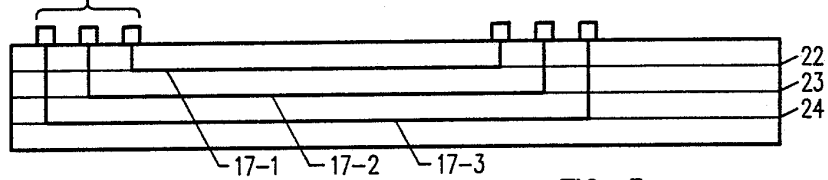


FIG. 3

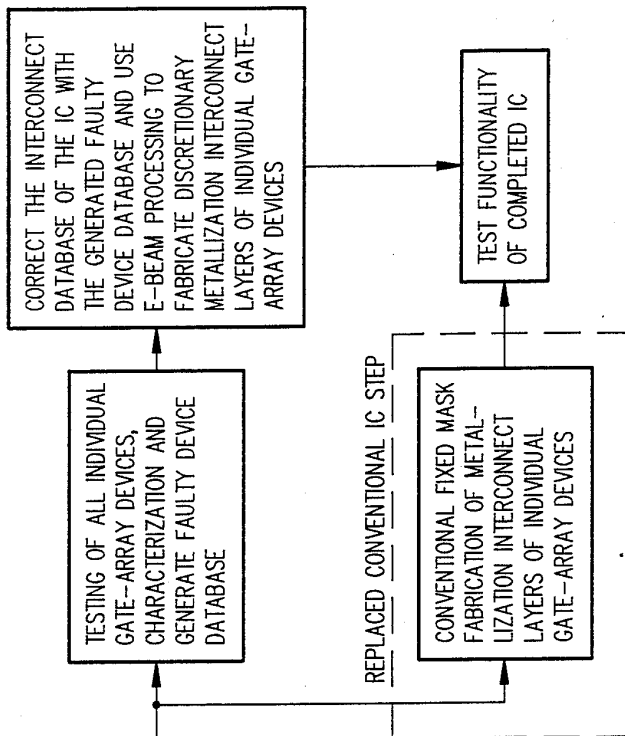


FIG. 4b

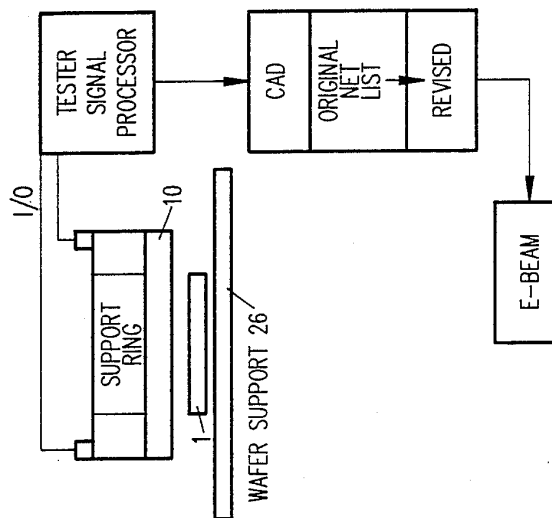


FIG. 4a

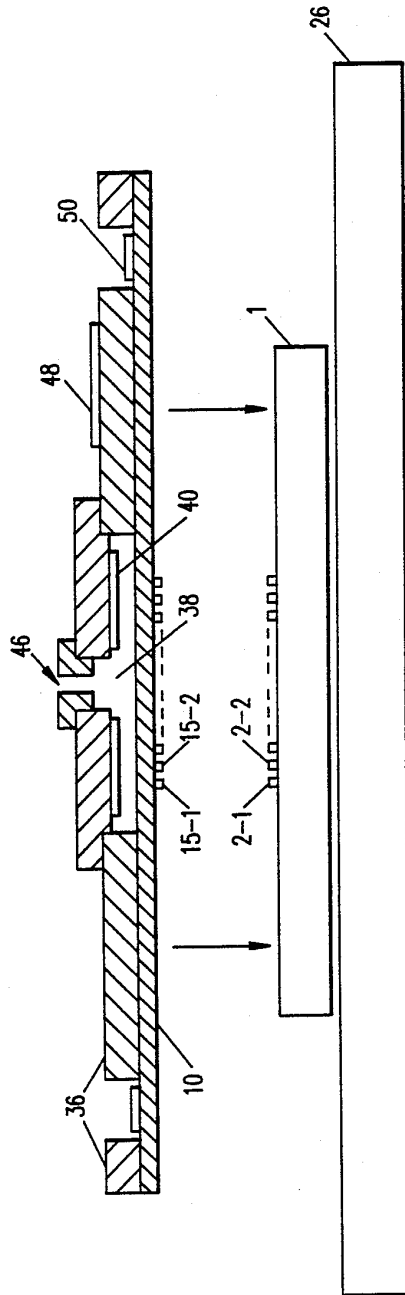


FIG. 5

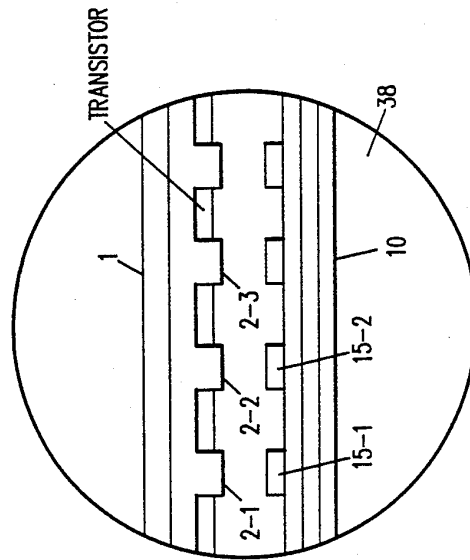


FIG. 6

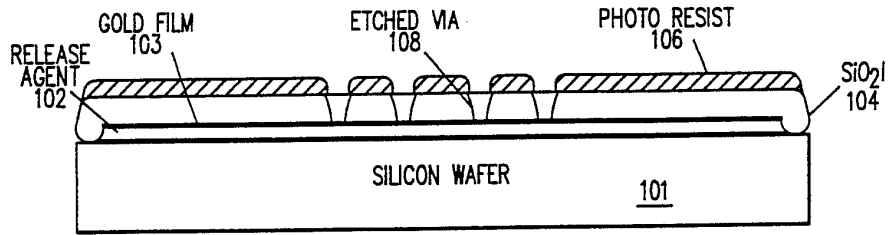


FIG. 7

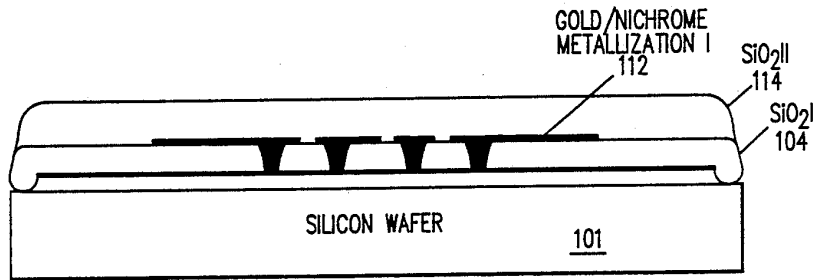


FIG. 8

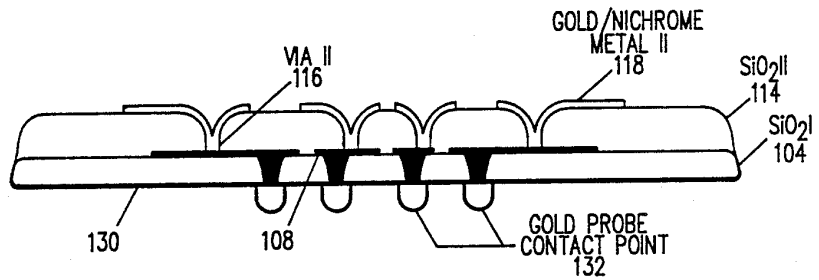


FIG. 9

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