Source/Drain Dislocations and Electrical Leakage in Titanium-Salicided CMOS Integrated Circuits

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ABSTRACT

This investigation explored the dependencies of source/drain (S/D) dislocation density, test circuit quiescent current, and junction leakage on processing variables in a titanium-salicided submicron CMOS process using Taguchi methodology. The primary factor affecting both gate and field edge dislocation densities was the type of polysilicon-to-metal dielectric (PMD) film. PECVD oxide PMD leads to lower defect densities than LPCVD oxides. Primary factor affecting quiescent current (I_{CCQ}) include PMD film type and S/D implant conditions. The observation of both lower dislocation density and lower I_{CCQ} leakage for similar PMD film type is taken as strong evidence linking dislocations with device electrical performance.

Previous investigations have shown that dislocations at gate and field oxide edges in As-implanted S/D regions can be responsible for electrical leakage.[1-6] These dislocations have been identified as vacancy-type half loops originating during the recrystallization of amorphized S/D regions.[6] It is well known that metal precipitates in dislocations exacerbate junction leakage.[7,8] A recent study indicates that leakage may also result from the propagation of localized dislocations into extended defects.[6]

This investigation explored the dependencies of S/D dislocation density, test circuit quiescent current, and junction leakage on processing variables in a titanium-salicided submicron complementary metal oxide semiconductor (CMOS) process using Taguchi methodology. The relationship between physical defects and electrical leakage is explored by identifying the factors that control dislocation density and correlating them with those that control I_{CCQ}. This approach is taken because we observe dislocations in device active regions that do not fail electrically. Hence, we use I_{CCQ} as a measurement of leakage over a large area involving hundreds of thousands of cells. This procedure provides a good statistical technique for sampling electrical leakage over a large area and numerically allocating the leakage to different physical phenomena. We supplement that technique by measuring junction leakage on isolated individual test structures fabricated adjacent to test circuits.

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Table I. List of Taguchi variables investigated.

	Taguchi variables	Reason
1	PECVD *vs.* LPCVD TEOS[a] sidewall oxide	Differential stress adjacent to gate conductor
2	PECVD *vs.* LPCVD TEOS screen oxide	Silicon to SiO_2 interfacial reactions
3	n^+ and p^+ S/D dose and energy As^+ (1×10^{15}, 120 keV *vs.* 3×10^{15}, 150 keV) B^+ (2×10^{15}, 15 keV *vs.* 3×10^{15} 20 keV)	Implant damage
4	S/D surface at anneal (bare *vs.* SiO_2)	Silicon vacancies
5	S/D preanneal temperature (450 *vs.* 600°C)	Solid-phase epitaxy
6	Titanium thickness (85 *vs.* 100 nm)	Stress from $TiSi_2$ Damage consumption by $TiSi_2$
7	PECVD *vs.* LPCVD TEOS PMD	Differential stress at steps

n^+ S/D implant consisted of a 4×10^{14}, 100 keV phosphorus implant in addition to the arsenic implant described as a Taguchi variable. Phosphorus implant conditions were identical for all splits.

[a] Tetraethylorthosilicate.

The process variables in the current investigation (Table I) were expected to affect dislocation formation and propagation as well as junction leakage current. For example, the use of plasma-enhanced chemical vapor deposition (PECVD) oxide as a PMD layer has been shown to result in reduced S/D dislocation density.[9] Therefore, a gate sidewall spacer oxide deposited by PECVD may be advantageous in regard to dislocation formation when compared to a low-pressure chemical vapor deposition (LPCVD) oxide. Similarly, optimized titanium salicide thickness is important for reducing junction leakage and eliminating residual crystalline damage from implant and anneal.[10-13] Implant parameters such as species, dose, energy, and screening film also affect the extent of crystalline damage,[2,5,14,15] and a low temperature (450°C) preanneal has been proposed to reduce residual damage in B-implanted areas.[16] The condition of the implanted surface (bare silicon or oxide capped) during anneal was investigated here to test the possibility of forming silicon lattice vacancies that reduce defect formation. PECVD and LPCVD oxides were also investigated as implant screening films. Si-deficient screening films such as PECVD SiO_2 may mitigate dislocation formation if high temperature interfacial reactions lead to the creation of Si lattice vacancies.

Table II. Taguchi matrix summary.

		Split identification							
Factor	Name	A	B	C	D	E	F	G	H
1	Sidewall oxide								
	PECVD	X	X	X	X				
	LPCVD					X	X	X	X
2	Screen oxide								
	PECVD	X	X			X	X		
	LPCVD			X	X			X	X
3	S/D dose/energy								
	Low As = 1×10^{15}, 120 keV P = 4×10^{14}, 100 keV B = 2×10^{15}, 15 keV	X	X					X	X
	High As = 3×10^{15}, 150 keV P = 4×10^{14}, 100 keV B = 3×10^{15}, 20 keV			X	X	X	X		
4	S/D anneal surface								
	Bare silicon	X		X		X		X	
	Oxide present		X		X		X		X
5	S/D anneal								
	450°C preanneal	X		X			X		X
	600°C preanneal		X		X	X		X	
6	TiSi								
	85 nm Ti	X			X	X			X
	100 nm Ti		X	X			X	X	
7	PMD								
	PECVD	X			X		X	X	
	LPCVD		X	X		X			X

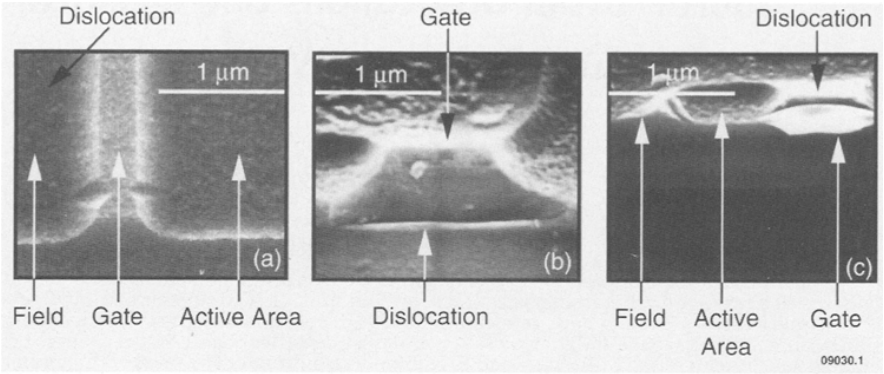

Fig. 1. (a) Top-angled SEM view and (b and c) cross-sectional views of gate edge dislocations near field boundary after Schimmel etching.

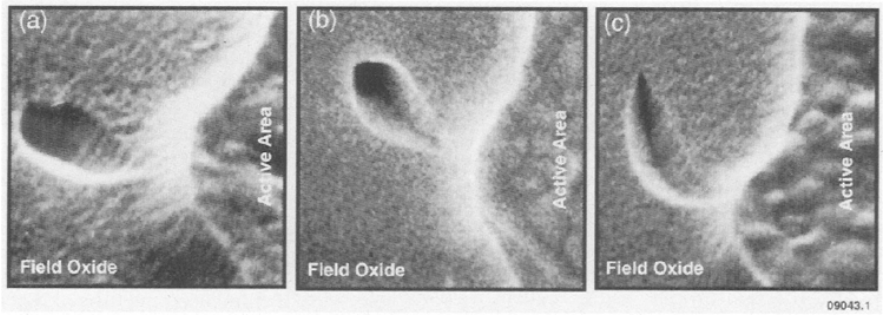

Fig. 2. Top view SEMs of field edge dislocations after Schimmel etching.

Experimental

This investigation analyzed test devices using a Taguchi L8 matrix (Table II) to identify the factors responsible for controlling gate and field edge dislocation density, overall test circuit quiescent leakage current, and diode leakage currents in n-well and p-well. The fabrication process employed localized oxidation of silicon (LOCOS) isolation and Ti-salicided polysilicon and active areas. Two full Taguchi lots were processed with four wafers per split. Following electrical testing, wafers for defect study were deprocessed to bare silicon before Schimmel etching[17] to bring out dislocations. Defect-etching methods have been described previously.[9] Defect densities were counted using scanning electron microscopic (SEM) photomicrographs. Various active area patterns were studied extensively using SEM to select a particular set of structures most prone to exhibit dislocations. These structures were then taken as a standard area for counting defects so we may compare different wafers and different process conditions. We observed that the defects revealed by this procedure corresponded to those found using cross-sectional transmission electron microscopy (XTEM), always occurring at gate or field edges.

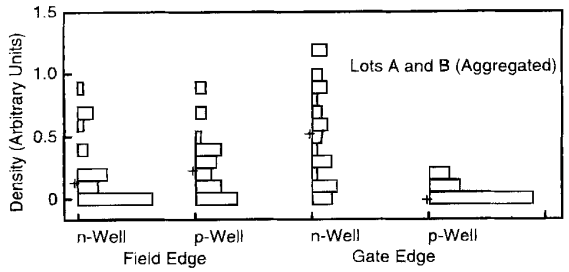

Fig. 3. Histogram of dislocation density vs. dislocation type showing distributions at n-well and p-well field edges and n-well and p-well gate edges, respectively.

Test circuit quiescent leakage current at room temperature was determined by setting register files, input latches, and output buffers to known high and low states, measuring I_{CCQ}, inverting these known states, and then remeasuring. Checkerboard (0-1-0-1) loading of the register file provided greatest electrical stress between elements. Measurements were taken on a Polaris very large scale integrated (VLSI) tester made by Megatest Corp.

We measured diode leakage currents on a Keithley Yieldmax 450 automatic test station. Arrays of area devices, finger devices, and gate diodes were analyzed.

Results

Dislocation density.—Schimmel etching revealed two types of dislocations: (*i*) gate edge defects protruding from S/D regions beneath sidewall oxide (Fig. 1) and (*ii*) field edge defects protruding into field oxide from edges of S/D regions (Fig. 2). Field edge dislocations are layout dependent, typically occurring at points where the boundary between active area and field is curved.[9] Both types of dislocations originate when the amorphous implanted region recrystallizes during anneal, leaving incipient crystalline damage that is propagated into extended dislocations by stress.[5,6,18,19]

Figure 3 shows a histogram of the distribution of defects for different dislocation types. The distributions of field edge dislocations in both wells are remarkably similar, but gate edge dislocations are significantly more numerous in n-well than in p-well.

The factor effects plot and Anova summary for n-well gate edge dislocation density are shown in Fig. 4a. These represent analysis of aggregated data from both lots. Numerical entries under each factor along the x-axis of Fig. 4a specify the factor effect, which is the difference between the mean values with that particular factor set

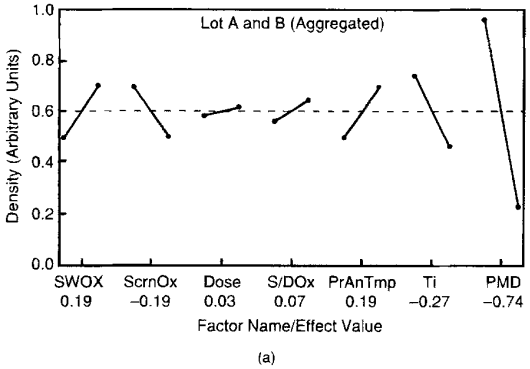

Fig. 4. Factor effects plot for (a) n-well gate edge dislocations and (b) n-well field edge dislocations. Lots A and B are aggregated. Minimum hurdles, or 2 − σ confidence level, are 0.20 and 0.08, respectively.

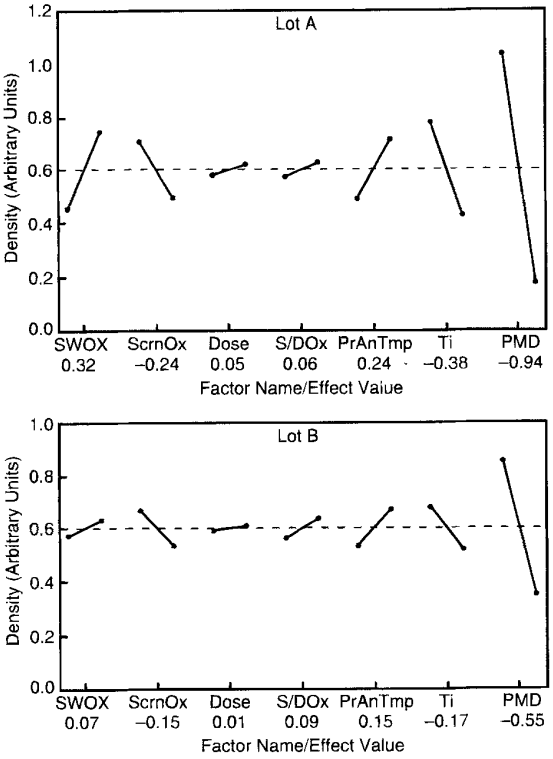

Fig. 5. Factor effects plot for n-well gate edge dislocations (lots A and B separately). Minimum hurdles are 0.16 and 0.13 for lots A and B, respectively.

high or low. The primary Taguchi factor affecting the gate

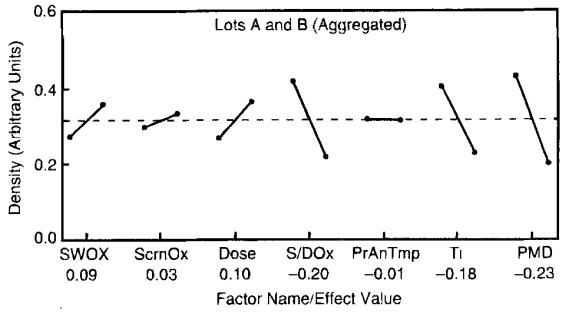

Fig. 6. Factor effects plot for p-well field edge dislocations. Minimum hurdle is 0.09.

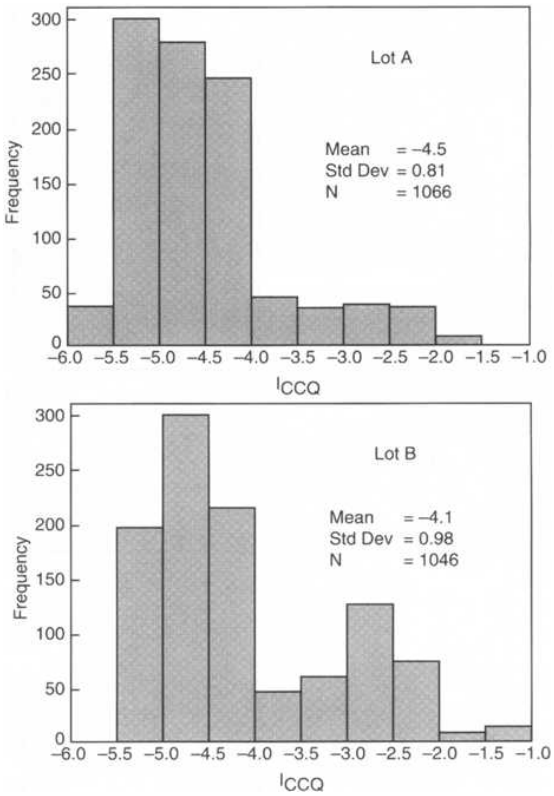

Fig. 7. Histograms of log (I_{CCQ}) for lots A and B.

temperature PECVD oxide results in a reduced density of extended dislocations compared to the case of LPCVD oxide. One reaches the same conclusion if the data from each lot are analyzed separately, as shown in Fig. 5. The influence of the PMD film on the control of dislocation density is remarkable. For example, the percentage of n-

Table III. Summary of important control parameters for dislocation density.

Well type	Dislocation type	Control factor	PC variance factor (%)	Confidence level (%)
n	Gate edge	PMD film	71	>99
n	Field edge	PMD film	43	>95
		Titanium thickness	25	>95
p	Field edge	PMD film	34	>95
		S/D surface (anneal)	26	>95

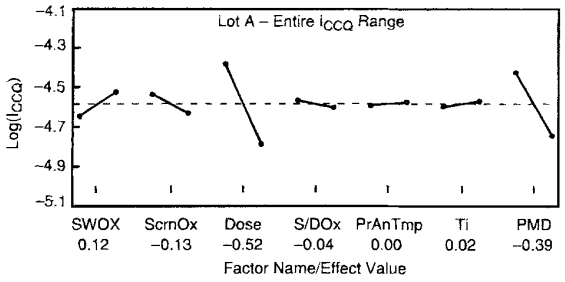

Fig. 8. Factor effects plot for I_{CCQ}-mean (lot A). Minimum hurdle is 0.09.

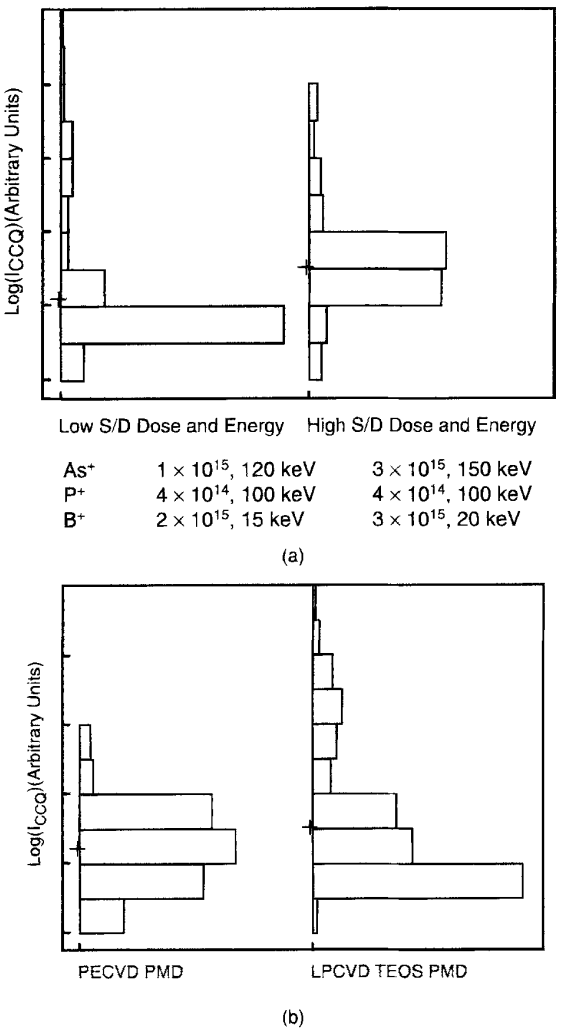

Fig. 9. Histograms of log (I_{CCQ}) comparing distributions for different process conditions: (a) S/D implant dose and energy conditions and (b) different types of PMD.

well gate edge dislocation density attributable to the PMD film type is 68 and 75% for the two lots, respectively. The beneficial effects of PECVD oxide PMD on dislocations have been attributed to reduced differential stress in regions where the PMD crosses topological steps.[9]

In n-well field edge dislocations (Fig. 4b), two primary control factors are observed, PMD film type and titanium thickness, accounting for 43 and 25% of the variation, respectively. The conditions that promote lower dislocation density in n-wells are PECVD oxide PMD and thin titanium. The observation of reduced dislocation density for

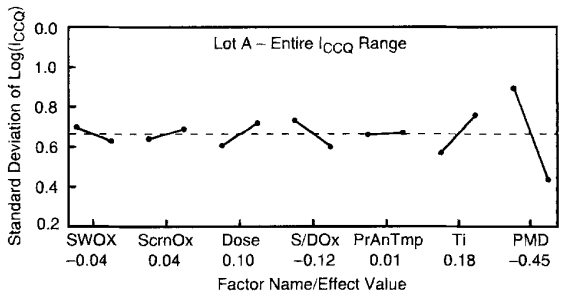

Fig. 10. Factor effects plot for I_{CCQ}-σ (lot A). Minimum hurdle is 0.08.

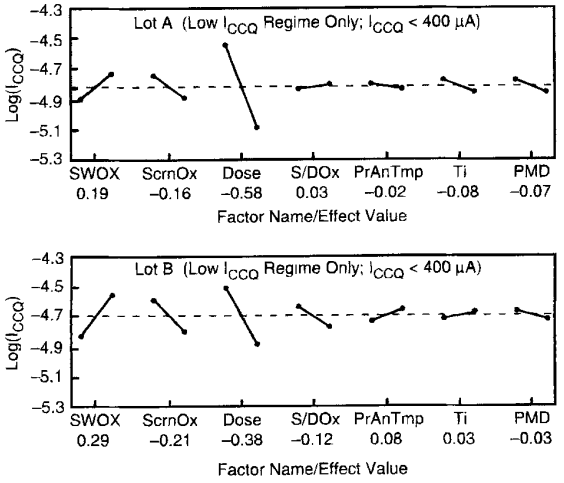

Fig. 11. Factor effects plot for I_{CQQ}-mean (lower I_{CCQ} range, I_{CCQ} < 400 A). Minimum hurdles are 0.08 and 0.10 for lots A and B, respectively.

thinner salicide is consistent with the high stress level of titanium salicide, which is an order of magnitude greater than stresses associated with grown or deposited oxides.[20]

Analysis of p-well field dislocation density (Fig. 6) again reveals that PMD film type is the primary control variable, with PECVD films showing lower defect density than LPCVD films. For p-well field edge dislocations, however, a secondary control factor is the condition of the S/D sur-

Table IV. Effects summary for quiescent circuit (I_{CQQ}).

Lot	Parameter	Factor	Low I_{CCQ} condition	Effect ($\log^{10}$)	Percent variation ($\log^{10}$)
Entire I_{CCQ} distribution					
A	Average I_{CCQ}	S/D dose and energy	Low	−0.52	58
A	Average I_{CQQ}	Poly-to-metal dielectric	PECVD	−0.39	33
A	I_{CQQ} sigma	Poly-to-metal dielectric	PECVD	−0.45	76
Low I_{CQQ} distribution-Log (I_{CQQ}) < −3.5					
A	Average I_{CQQ}	S/D dose and energy	Low	−0.58	82
B	Average I_{CQQ}	S/D dose and energy	Low	−0.38	47

Table V. Test circuit diode leakage structures.

Structure type	Number of units	Size (μm)	Area (μm^2)	Perimeter (μm)
Area diode	1 cell	100 × 280	28,023	760
Island diode	1,914 islands	2.5 × 2.5	6,338	10,140

Table VI. Effects summary for n^+ diode leakage.

Diode type	Lot	Factor	Low leakage condition	Effect ($\log^{10}$)	Percent variation ($\log^{10}$)	I ($\log^{10}$)
Finger	A	PMD	PECVD	−0.1	45	−10.9
	B	PMD	PECVD	−0.1	19	
	B	Sidewall oxide	PECVD	−0.1	19	
Island	A	Poly-metal dielectric	PECVD	−0.2	34	−11.1
	B	S/D preanneal temperature	450°C	−0.1	24	
Area	A	PMD	PECVD	−0.2	59	−11.0
	B	Titanium thickness	85 nm	−0.1	33	
Gated[a]	A	Titanium thickness	85 nm	−0.2	20	−11.1
	B	Screen oxide	PECVD	−0.1	55	

[a] Gated diode leakage is measured under accumulation.

Table VII. Effects summary for p^+ diode leakage.

Diode type	Lot	Factor	Low leakage condition	Effect ($\log^{10}$)	Percent variation ($\log^{10}$)	I ($\log^{10}$)
Finger	A	Sidewall oxide	LPCVD TEOS	0.9	56	−8.9
	A	S/D dose and energy	Low	−0.8	36	
	B	S/D dose and energy	Low	−0.7	47	
	B	Sidewall oxide	LPCVD TEOS	0.7	40	
Island	A	Titanium thickness	85 nm	−0.7	40	−10.6
	B	S/D dose and energy	High	2.2	27	
	B	S/D preanneal temperature	450°C	−2.2	25	
	B	Titanium thickness	85 nm	−2.0	20	
Area	A	S/D dose and energy	Low	−0.2	46	−11.1
	B	Titanium thickness	85 nm	−0.6	45	
	B	Screen oxide	PECVD	−0.5	26	
Gated[a]	A	S/D dose and energy	Low	−0.1	47	−11.3
	B	Titanium thickness	85 nm	−0.2	35	
	B	Screen oxide	PECVD	−0.1	23	

[a] Gated diode leakage is measured under accumulation.

face during anneal, with a bare surface giving fewer dislocations than an oxide-capped surface. It appears that a silicon surface with native oxide may provide a source of silicon lattice vacancies that mitigate implant damage. The volatilization of SiO gas from a thin native oxide on silicon in an oxygen-deficient atmosphere has been reported for temperatures as low as 900°C;[21] the loss of SiO from native oxide leading to silicon-deficient SiO_x may lead to an interaction at the oxide-to-silicon interface that produces silicon vacancies.

Another secondary factor for controlling p-well field edge dislocations is the titanium thickness. Again, thinner titanium results in fewer dislocations, in agreement with results reported previously.[10]

Table III summarizes the major control factors for each dislocation type. PMD film type is important for controlling all three types of dislocations, while the titanium thickness plays a smaller role at field oxide edges and the condition of the S/D surface during anneal is influential at p-well field edges. At first glance, it is somewhat surprising that As-implant conditions (dose/energy) do not play a major role in controlling dislocation density, since previous studies have observed dose-related effects.[22-24] This apparent discrepancy arises because, for the case of dual As and P S/D implants used in the current investigation, the P implant alone is sufficient to amorphize silicon, leading to incipient recrystallization damage.[9]

Quiescent leakage current.—Histograms of I_{CCQ} distributions in lots A and B show distinctively different character (Fig. 7). The majority of I_{CCQ} values in lot A fall into the low leakage regime, while lot B exhibits a bimodal I_{CCQ} distribution with an anomalous secondary peak at values of I_{CCQ} above 400 μA. Not surprisingly, separate Taguchi analyses on a by-lot basis indicate inconsistency between the important Taguchi factors found for each lot. For this reason, we believe that the two leakage current peaks in lot B are affected by different physical mechanisms. For example, physical particles may be responsible for high leakage current mechanism in lot B is not correlated to dislocations, which are present at the same levels in both lots.

On the basis of the above observations, a two-pronged approach was taken to circumvent the difficulties encountered from the bimodal distribution. First, the data from lot A were used to represent typical I_{CCQ} behavior over the complete I_{CCQ} range. Then, to understand the lower I_{CCQ} regime, data from both lots were analyzed separately, and the important Taguchi factors for this regime are common to both lots.

Analysis of entire I_{CQQ} distribution-mean I_{CCQ} value.—Figure 8 shows the factor effects plot and Anova summary for the I_{CCQ}-mean of lot A. Primary control factors are S/D implant dose/energy and PMD film type, which account for 58 and 33%, respectively, of the observed variation. Lowest leakage occurs for reduced S/D dose and energy as well as for PECVD oxide as the PMD layer. The impact of S/D dose and energy, as well as PMD oxide film type, is illustrated by Fig. 9, which shows that the main part of the I_{CCQ} distribution is shifted to lower values by using low dose and energy, while the higher current events are virtually eliminated by using PECVD oxide PMD. The observation of both lower dislocation density and lower I_{CCQ} leakage with similar PMD film type is taken as strong evidence linking dislocations with device electrical performance.

Several possibilities exist for the role of the S/D implant in affecting leakage, including (*i*) electrical charging effects, (*ii*) junction profile effects, and (*iii*) physical damage related to dislocations. Analysis of gate oxide integrity (GOI) data provides no evidence of unusual gate oxide weakening normally associated with electrical charging. Junction profile effects, however, may be important because S/D dose and energy are primary Taguchi factors controlling p^+ diode leakage (see section on Diode leakage). The transistor characteristics, however, are not appreciably affected by the choice of implant dose and energy within the range investigated. There also may be an interaction between junction depth and dislocation electrical activity. More specifically, although the density of disloca-

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