CHARACTERISTICS OF CMOS DEVICES FABRICATED USING HIGH QUALITY THIN PECVD GATE OXIDE

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ABSTRACT

N- and p- channel FETs at 0.25μm channel length are fabricated utilizing very thin (35-70 Å) PECVD oxide as the gate dielectric. This oxide can be deposited at very low substrate temperature ($\leq$350 °C) in a low pressure PECVD system. A helium plasma treatment is applied prior to the deposition in order to reduce the surface roughness and lower the surface state induced mobility degradation. Measured oxide quality is similar to the thermally grown SiO_2 in terms of the oxide charges and breakdown characteristics. The device characteristics are similar to the same devices fabricated with thermally grown gate oxide although the device transconductances are slightly reduced. The potential of using this kind of oxide for the deep sub-micron devices is discussed.

INTRODUCTION

Plasma enhanced chemical-vapor deposition (PECVD) has the advantage of depositing oxide in a clean processing vicinity at very low temperature. The thermal oxidation process and dopant segregation/redistribution can be eliminated by depositing oxide directly on the device substrates in a low temperature environment. This is very desirable for the deep submicron silicon MOSFET applications and for other novel semiconductor FET devices required low temperature processing. However, the oxide to substrate interface properties and the film quality are the major concerns to use the PECVD oxide as gate dielectric in the device fabrication. It has been reported that high temperature annealing after the deposition is required to densify the film and to improve the oxide quality as gate dielectric in MOSFET applications [1-3]. Recently we have successfully practicing a modified PECVD process to deposit very thin (35-70Å) oxides as gate insulator of polysilicon gate CMOS devices at very low substrate temperature ($\leq$350°). A helium plasma treatment prior to the deposition is introduced in order to improve the oxide to silicon interface roughness. The oxide is deposited in a high flow rate of helium carry gas at low deposition rate to ensure a near ideal chemical vapor deposition process. Excellent device characteristics are obtained at channel length as low as 0.25μm. This is the first demonstration that very thin PECVD oxides used in the fabrication of silicon gate FETs. For the comparison purpose the same 0.25μm FET devices with thermally grown gate oxide are also fabricated in this experiment. In this paper, the PECVD oxide properties, the FET device characteristics and the comparison between devices with PECVD and thermally grown gate oxides will be discussed.

EXPERIMENT

The PECVD oxide films are deposited at very low substrate temperature ($\leq$350°C) in a low pressure PECVD system as shown in figure 1. The process parameters of this deposition system are listed in table I. A base pressure at 1×10^{-4} is routinely achieved before each deposition process. The substrate is pre-cleaned in the dilute HF and rinsed in DI water before loaded into the system. A helium plasma treatment prior to the film deposition is applied to minimize the FET mobility degradation from the surface roughness [1]. The film deposition is operated in a gas flow consisting of diluted SiH_4/helium, N_2O and helium carrying gas. At a low deposition rate (14Å/min.) the gas phase nucleation is minimized to accomplish a true heterogeneous CVD process.

The FET devices are fabricated using a 0.25μm CMOS process [4]. The wafers are separated into different groups at the gate oxide step. In our experiment the PECVD oxides are deposited at a thickness 70Å. Thermal oxides of the same thickness are also grown on the control wafers for the comparison purpose. Also a 40Å thick PECVD oxides are deposited on some of the wafers in order to study the FET characteristics with thinner PECVD gate oxides. Optical lithography is used at all patterning levels through out the entire device fabrication. The polysilicon gate dimension as low as 0.3μm can be patterned in a I-line stepper using contrast enhancement lithography followed by a high selectivity reactive ion etching process. In this process arsenic implant doped N+ polysilicon gates is used for the n-channel FETs and boron doped P+ gates are used for p-channel devices. The N+ and P+ poly gates are doped during the source/drain for-

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mation steps. The arsenic doped N+ source/drain junctions at a depth around 0.1μm is achieved by a 900°C annealing process. The boron doped P+ junctions at 0.12μm deep are formed by germanium amorphorization implant prior to the BF_2 implant and subsequently driven in at 850°C. After the drive-in of source and drain junctions, a 350Å thick self aligned titanium silicide is formed by a rapid thermal annealing process on the source/drain and poly gates simultaneously to obtain a sheet resistance of around 7 Ω/square. The fabricated devices are passivated by LPCVD oxide and a Al-Cu-Si metal with titanium barrier layer is used as the final metallization.

DEVICE CHARACTERISTICS

The thin oxide breakdown characteristics are compared using capacitors isolated by thick oxides. A typical breakdown current voltage characteristics is described in figure 2(a). There is little difference in the breakdown voltages between the PECVD oxide and thermal grown oxides at this thickness. Figure 2(b) shows the distribution of the breakdown voltages of the 7 nm thick PECVD oxide from a large number of samples. Other oxide parameters measured from the C-V characteristics are listed in Table II. Although the midgap interface trap density D_u and the fix charge density D_f are larger than most thermally grown oxides, they are still acceptable for the device applications.

The I_d-V_d characteristics of the 0.25μm n- and p-channel FETs are shown in figure 3 for both PECVD and thermally grown gate oxides. The transistor transconductance from both n- and p-channel FETs with PECVD gate oxide are slightly reduced due to lower mobility. The mobility reduction is attributed to the higher surface state density and/or the rougher interface of the PECVD oxide. The helium plasma treatment prior to the oxide deposition has improved the interface quality compared to the prior works [1-3]. The FET parameters derived from this figure are summarized in Table III. The n-channel FETs suffer more on transconductance degradation may due to the higher electron mobility. P-channel FETs with thinner (40Å) gate oxides are also fabricated with the same device structure. The I_d-V_d characteristics is shown in figure 4(a). Although the threshold voltage of this device is lower due to the thinner gate oxide is used. It shows a transconductance at 108 mS/mm and there is no indication of boron penetration from the boron doped P+ polysilicon gate. However the gate current of this device is much higher at the same gate bias voltages (figure 4(b)) due to the tunneling of the holes through the thin gate oxide. The hot carrier stress induced threshold voltage shift result is shown in figure 5. After the 10^5 second of hot carrier stress the device threshold voltage is only shifted by 110 mV induced by the electron trapping in the PECVD gate oxides. These results suggest that the PECVD oxide can be used as gate dielectric even for the further scaled down FET devices.

CONCLUSIONS

In conclusion a high quality thin PECVD gate oxide has been used in the fabrication of 0.25μm CMOS devices. These devices are comparable to thermal oxide devices without the need of high temperature process and oxidation steps. Although the carrier mobility from both n- and p-channel devices are slightly reduced as indicated from the transconductance measurement. The PECVD deposit oxide provide a potential alternative as the gate dielectric for deep sub-micron FETs as well as other non-silicon FET devices with thermal process limitations.

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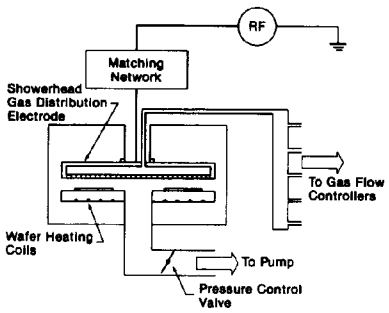
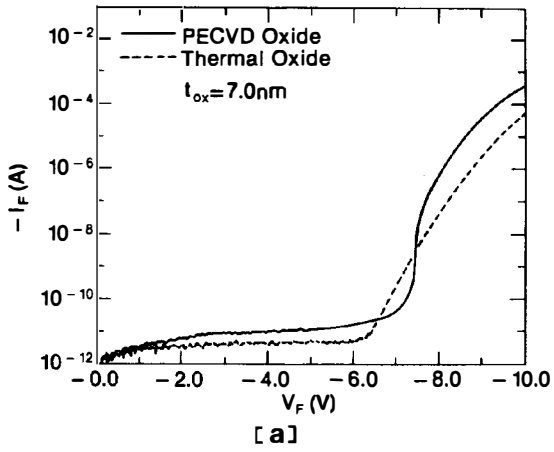


Figure 1 Schematic diagram of the PECVD system.

Temperature	**350**	**°C**
Base pressure	**2×10^{-4}**	**torr**
Surface preparation:		
He flow rate	**1000**	**sccm**
pressure	**1.0**	**torr**
power	**100**	**watt**
Deposition:		
gas flow rate:		
SiH_4(2%)/He	**38**	**sccm**
N_2O	**250**	**sccm**
He	**2150**	**sccm**
pressure	**0.5**	**torr**
power	**200**	**watt**
Deposition rate	**14**	**Å/min.**

Table I PECVD oxide process parameters.



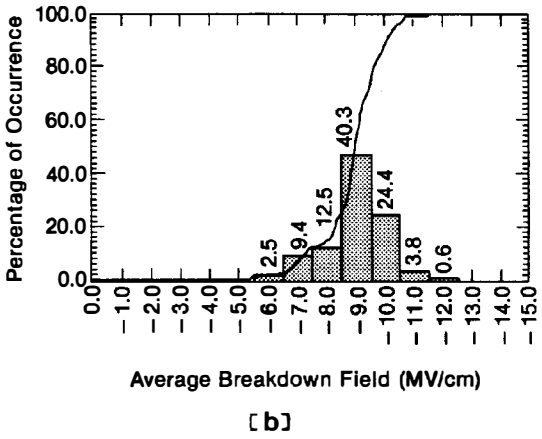
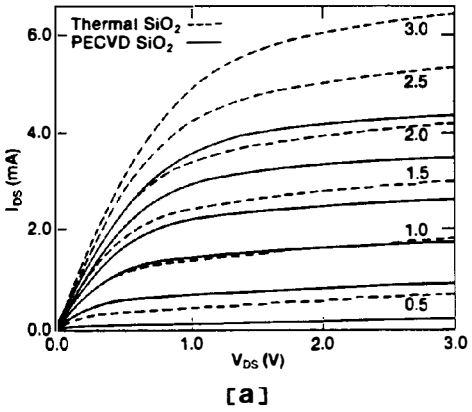


Figure 2 (a) Breakdown field distribution of 7 nm PECVD and thermally grown oxides. (b) Breakdown field distribution of 7 nm PECVD oxide.



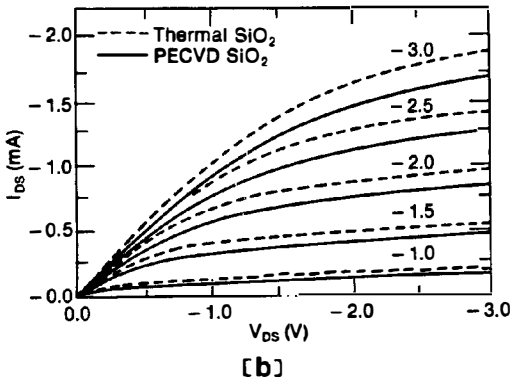
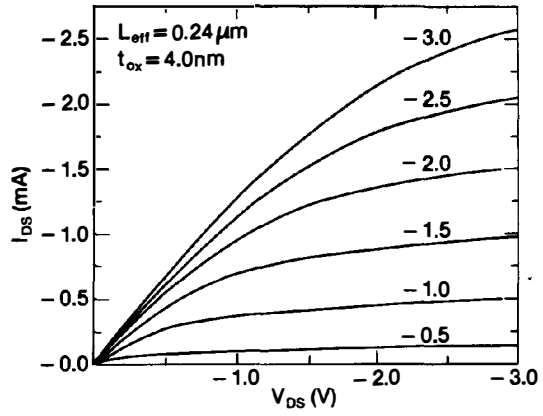


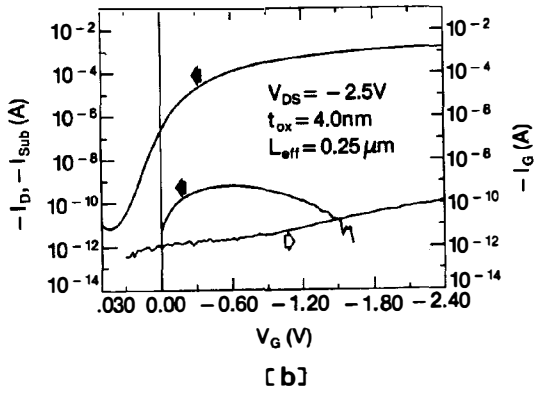
Figure 3(a) I-V characteristics of 0.25μm L_{eff} n-channel FETs with 7 nm thermally grown and PECVD gate oxides. (b) I-V characteristics of 0.25μm L_{eff} p-channel FETs with 7 nm thermally grown and PECVD gate oxides.

Thicknessre	7.2	nm
Breakdown field	9	MV/cm
D_s	6×10^{10}	$cm^{-2}eV^{-1}$
D_f	6×10^{11}	cm^{-2}
Leakage current	1.6	nA/cm^2

Table II Parameters of 7 nm PECVD oxide.



[a]



[b]

Figure 4(a) I-V characteristics and (b) Gate current and substrate current of a 0.25μm p-channel MOSFET with 4 nm PECVD gate oxide.

Parameter	Thermal oxide		PECVD oxide	
N-channel FET:				
t_{ox}	73	Å	71	Å
subV_t slope	81	mV/dec.	83	mV/dec.
G_m(Vd=2.5 V)	220	mS/mm	177	mS/mm
P-channel FET:				
t_{ox}	74	Å	71	Å
subV_t slope	82	mV/dec.	83	mV/dec.
G_m(Vd=-2.5 V)	88	mS/mm	80	mS/mm

Table III Comparison of device characteristics of n- and p- channel devices with thermal and PECVD gate oxides.

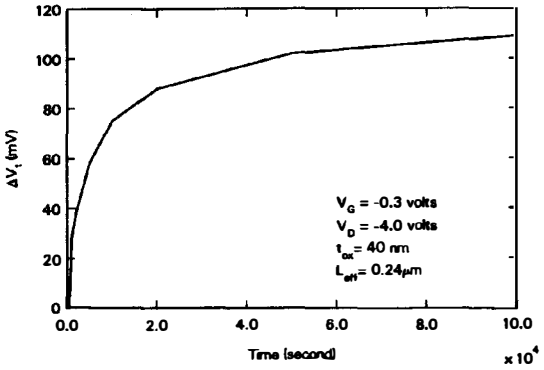


Fig. 5 Threshold voltage shift as a function of the hot electron stress time for a 0.24μm p-channel MOSFET with 4.0 nm PECVD gate oxide. (V_{DS}= 4.0 volts, V_{GS} = 0.3 volts)