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EFFECT OF ANNEALING AND PLASMA PRECLEANING ON THE ELECTRICAL PROPERTIES OF N_2O/SiH_4 PECVD OXIDE AS GATE MATERIAL IN MOSFETs AND CCDs

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Abstract—Pure SiH_4 and N_2O involving low total inflow of gases and very high deposition rate (1400 Å/min) have been used to deposit PECVD oxide films in a parallel-plate reactor system. The effect of long time (40 min) low temperature (450°C) annealing in N_2 ambient and plasma precleaning with different gases like Ar, N_2, H_2, O_2, CF_4/50% H_2, on the electrical properties of the deposited films have been studied. Flatband voltage, V_{fb}, fixed oxide charge density, D_f, interface trap level density, D_{it}, dielectric breakdown strength, hysterisis and bias stress stability are the properties studied. These properties are relevant to the gate oxide in MOSFETs and CCDs. The deposited films involving annealing and plasma precleaning have been found to show electrical properties comparable to those of dry thermal oxide films grown at 1100°C. In particular films deposited on H_2 plasma precleaned wafers showed no bias stress instability.

1. INTRODUCTION

Plasma processing is now widely used in VLSI technology. Inorganic insulator films are being deposited by plasma deposition (PD) process where low deposition temperature (25–500°C) cannot affect the previous process steps. The low temperatures involved overcome the disadvantages associated with the high temperature (900–1200°C) thermal oxidation process, which is becoming incompatible with developments in submicron technology. These disadvantages are: (1) formation of stacking faults which originate at the sites of mechanical damage at the wafer surface[1,2] and then expand during oxidation by emission of vacancies to the growing Si–SiO_2 interface[3,4]; (2) formation of the bird's "beak" profile during the dielectric isolation process which creates abrupt topographical features on the surface causing breaks or discontinuities in the film covering them. It also reduces the available active surface area and therefore affects the packing density of the integrated circuits[5]; (3) doping impurity redistribution takes place because of the high oxidation temperatures.

PD is useful in controlled doping of layers, alloying and multilayering[6] and is fast replacing the chemical vapour deposition (CVD) SiO_2 because of its better results[7]. PECVD SiO_2 films can be formed by reacting precursor gases like silane (SiH_4) or silane derivations with an oxidant like CO_2, O_2, N_2O etc. in an RF or microwave discharge. This dates back 27 years[8–20]. Usually the precursors are diluted in Ar or He to 1–5% before being used, but pure gases can be used as well[14]. The overall reaction leading to the formation of plasma SiO_2 is:

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2H_2 + 2N_2$$

and one of the suggested mechanisms has been reported by Dun *et al.*[21]. The electrical energy in the reactors used is either inductively coupled, indirect capacitively coupled through the walls of the vacuum chamber using external electrodes or direct capacitively coupled using internal electrodes. The latter provides better control over the process and flexibility in the reactor design and uniform electric fields can be created over large areas resulting in uniform deposition over larger areas. The choice of the reactor affects the physical and electrical properties of the plasma SiO_2, as one of the limitations of PD is the non-linear effect of a volumetric increase in size of the reactor on the process parameters such as substrate temperature, RF power, gas ratio and total pressure. Due to the type of applications of this plasma SiO_2 as injector in EEROM[16], insulator films for diffusion masks, interlayer dielectric[7] and as passivation layer, most of the above mentioned research papers have concentrated on the physical properties of the film like refractive index, density, stress, stoichiometry, etch rate, deposition rate, step coverage, and annealing behaviour.

The electrical properties which are important if the film has to be used as an insulator in active devices like MOSFETs and CCDs, have been studied[18–20] and have been shown to compare well with the thermal oxides. Very low deposition rates of 50–60 Å/min using dilution with inert gas like He, have been used in these studies. One or two particular substrate temperatures have been chosen in these studies with not much reason indicated for the choice as also in the case of previous research. We have studied the electrical properties by depositing the film using pure SiH_4 and N_2O giving very high deposition

rate of 1400 Å/min at the substrate temperature range of 200–400°C. This temperature range has been chosen because it has already been shown that films deposited in this range have stable physical properties[15]. Using this rate and pure gases, the effect of long time low temperature annealing and plasma precleaning on the electrical properties have not yet been reported. Also, using such high rates, the physical properties have already been shown to compare well with those of thermal oxide[14] and as shown in the present study, the electrical properties are comparable too.

Plasma precleaning of the silicon wafer surfaces has been performed using different gases like Ar, N_2, H_2, O_2, CF_4/50% H_2, and their effect on the electrical properties have been studied by us. The importance of cleaning of wafers is more here because in PD, the film grows on the cleaned wafer surface which forms the Si–SiO_2 interface, unlike in thermal oxide where the silicon is consumed and the Si–SiO_2 interface moves into the silicon during oxidation so that the final temperature and oxidation time determine the interface. The importance of surface preparation have also been highlighted by Stasiak *et al.*[20].

At the deposition rate used, it would require 4 s to deposit 100 Å thick films being used in today's devices and it is thus difficult to control the flow of gases, manually. Therefore, 700 Å thick oxides have been studied, keeping in mind that the properties studied (e.g. D_f, D_{it}) are not greatly affected by the thickness of the oxide[22]. Therefore, the results are very much applicable to thin films also. The results of the present study (e.g. D_{it}) are similar to the values obtained for <100 Å thin films[18]. Breakdown strength has also been shown to remain the same for oxide thickness range of 250–1579 Å[19] to further support the validity of the results obtained for 700 Å thick films.

2. EXPERIMENTAL

The reactor used in the present study is a parallel-plate Reinberg type in high pressure configuration. The top electrode is supplied by the RF power at 13.56 MHz frequency and the bottom electrode is grounded. The operating pressure range is 0.133–1.33 mbar for deposition in this type of reactor. The reactor system, PD-10, is supplied by Samco International Inc., Kyoto, Japan. The bell-jar of the reactor is 30 cm in diameter with the bottom electrode 20 cm in diameter, provided with the heater to heat up to 400°C, and can rotate at 1 rpm. The electrode distance is variable from 2 to 4 cm. The RF power supply consists of 13.56 MHz crystal controlled generator to supply 150 W power with manual impedance matching provision. The vacuum line has a diffusion pump of 300 l/s capacity and a rotary pump of 200 l/min capacity.

1 mbar total pressure and 50 RF W power for 30 s giving an average deposition rate of 1400 Å/min in all depositions. Only the substrate temperature was varied from 200 to 400°C in steps of 50°C with the intention of studying its effect on the electrical properties of the oxide film. A typical deposition run involved the following steps after setting the sample on the substrate:

1. The chamber is evacuated to 10^{-3} mbar using the rotary and diffusion pump.
2. N_2O is flown in at 20 ml/min using only the rotary pump and plasma is generated setting the power to 50 RF W.
3. SiH_4 is flown in at 1 ml/min for 30 s to given an oxide thickness of about 700 Å.
4. The power is then terminated and the chamber again evacuated to 10^{-3} mbar followed by N_2 purging for 15 min.

The above typical run was preceded by plasma precleaning in various gases like Ar, N_2, H_2, O_2, and CF_4/50% H_2. All the precleaning was done at 0.4 mbar total pressure, except the CF_4/50% H_2 precleaning in one experiment where the total pressure was 0.6 mbar. 50 RF W power was supplied during precleaning also and the substrate temperature was in the 200–400°C range. The precleaning was performed for 15 min. MOS capacitors were fabricated on these films using high purity Al, evaporated through a clean metal mask to form 1 mm diameter dots on the deposited SiO_2 film. Al was also evaporated on the backside for ohmic contact. Similarly, MOS capacitors were also fabricated on the dry thermally grown oxide film, grown at 1100°C for 24 min giving a thickness of approximately 800 Å. The electrical properties of the thermal SiO_2 were studied to compare with the electrical properties of PECVD oxide in our laboratory conditions. The wafers used were p-type with $\langle 100 \rangle$ orientation and 1–6 Ω-cm resistivity. These wafers were cleaned by the RCA standard clean procedure[23] including 1% HF solution dip for 15 s before cleaning with standard clean-1 solution. Postmetallization annealing was performed in N_2 ambient for a total of 40 min at 450°C as a study parameter. 10 min annealing for fabricated devices is essential for good contact. However, in our case, further 30 min annealing has affected the electrical properties of the deposited film.

The electrical properties studied were flatband voltage (V_{fb}), fixed oxide charge density (D_f), interface trap level density (D_{it}), and the dielectric breakdown strength. A practical implementation of the methods used in finding these properties can be found in the authors' earlier work[24]. Hysterisis, by way of retrace on the CV-plotter, and bias stress stability were also studied for the devices. A bias stress of

Table 1. Values of the electrical properties of films deposited at different substrate temperatures, before and after postmetallization annealing. The wafers underwent no plasma precleaning

Electrical properties		Deposition temperature (°C) 200	250	300	350	400
V_{fb} (V)	Unannealed	14.0	3.5	16.0	13.75	−15.5
	Annealed for 10 min	4.5	3.5	0.25	2.5	−4.5
D_f (charges-cm^{-2})	Unannealed	-4.09×10^{12}	-1.57×10^{12}	-7.13×10^{12}	-5.83×10^{12}	6.04×10^{12}
	Annealed for 10 min	-1.46×10^{12}	-1.54×10^{12}	-3.94×10^{11}	-1.12×10^{12}	1.48×10^{12}
D_{it} (cm^{-2}eV^{-1})	Unannealed	3.13×10^{12}	1.00×10^{13}	3.43×10^{12}	1.97×10^{12}	5.94×10^{12}
	Annealed for 10 min	7.14×10^{11}	2.78×10^{12}	1.17×10^{12}	9.53×10^{11}	1.27×10^{12}

3. RESULTS AND DISCUSSION

At first, the electrical properties of the dry thermal oxide was studied to later on compare with the properties of PECVD oxide films. It was found that for thermally grown oxide, V_{fb} was −2.0 V, D_f was 3.00×10^{11} charges/cm^2, D_{it} was 2.27×10^{11}/cm^2-eV and an average dielectric breakdown strength of 5.26 MV/cm in our laboratory conditions. Retrace on the CV-plotter showed no hysteresis and a bias stress of ±10 V for 1 min each showed no shift in V_{fb}, characterizing the usual charge stability of the thermal oxide. A typical I–V characteristic showed a steep rise in the current from 1 to 100 μA within 1V change in the step voltage applied through a Hewlett–Packard pA meter/d.c. voltage source, model 4140B, signifying the breakdown. Hence, when 1 μA current was emitted through the 1 mm diameter dot capacitor, it was assumed that the breakdown has occurred.

PECVD SiO_2 films grown directly after the conventional RCA standard clean wet chemical cleaning process with the substrate temperature in the range of 200–400°C, and no annealing, showed high V_{fb}, of the order of 14V. V_{fb} for films deposited at 400°C was −15.5 V. D_f values were large ranging from -1.57×10^{12} charges/cm^2 to -7.13×10^{12} charges/cm^2. D_f for films deposited at the substrate temperature of 400°C was 6.04×10^{12} charges/cm^2. D_{it} values were large too, ranging from 1.97×10^{12} cm^{-2}-eV^{-1} to 1.00×10^{13} cm^{-2}-eV^{-1}. Also, the accumulation and inversion regions showed instability. A 10 min postmetallization anneal at 450°C in N_2 ambient showed large changes in the property values and this is summarized in Table 1. The values of the electrical properties in Table 1 shows the importance of annealing as compared to no annealing.

Gereth and Scherber[25] have studied the effect of plasma precleaning using different gases on the bias stability and hysteresis of the PECVD nitride films deposited using N_2/SiH_4 gas mixture. Here, the authors have used Ar, N_2, H_2, O_2 and CF_4/50% H_2 gases for plasma precleaning the wafer surfaces with interesting favourable results. Ar plasma precleaning was tried first for 15 min on the wafers at three different substrate temperatures—250, 300 and 350°C, and PECVD oxide films deposited at the same individual temperatures. The electrical properties of the deposited films were evaluated after a 10 min postmetallization anneal, followed by evaluation after a further 30 min annealing. These values are summarized in Table 2. A comparison of the values in Tables 1 and 2 after 10 min anneal favours plasma precleaning. Also, a further 30 min anneal improves the D_f values, but increases the D_{it} values a little. Long time, low temperature postmetallization annealing had previously been shown to change the properties of the film[15], particularly, loss of H_2O, SiOH and SiH groups had been observed. This is believed to affect the electrical properties as well. On performing retrace, the hysteresis that was present after a 10 min anneal was eliminated after a further 30 min anneal. Gereth and Scherber[25] had supported Zebrst[26] in his theory that the hysteresis behaviour is related to the presence of the native oxide layer between Si_3N_4 and Si in their plasma nitride films. According to Zebrst, traps are located at the interface between the oxide and the nitride which charged and discharged through the native oxide during C–V measurements causing hysteresis of the C–V curve. Further, the charge transport occurs through tunneling as the native oxide layer is very thin. In our experiments, further 30 min annealing completely eliminated the hysteresis at ±10 V bias sweep. This either puts the above theory of tunneling

Table 2. Values of the electrical properties of the films deposited after Ar plasma precleaning. The devices fabricated were annealed for 10 min and a further 30 min

Electrical properties		Deposition temperature (°C) 250	300	350
V_{fb} (V)	10 min annealing	−2.47	−3.37	−4.53
	30 min annealing	−2.19	−2.68	−2.02
D_f (charges-cm^{-2})	10 min annealing	4.37×10^{11}	6.63×10^{11}	1.14×10^{12}
	30 min annealing	3.46×10^{11}	4.79×10^{11}	3.31×10^{11}

in question or the annealing removes the imperfections at the native oxide and PECVD oxide interface in our case. When bias stress of ± 10 V was applied for 1 min each, V_{fb} shifted from 0.1 V to as much as 0.4 V characterizing bias stress instability. The dielectric breakdown strength of these films annealed for a total of 40 min was determined. Films deposited at substrate temperatures of 250, 300 and 350°C showed breakdown strengths of 6.07, 4.25 and 9.39 MV/cm respectively. No particular trend was observed relative to the increase in the substrate temperature and therefore the dielectric breakdown strengths of PECVD oxide films can be said to vary in the range of 4–10 MV/cm. This has also been shown by Adams *et al.*[15].

N_2, H_2 and O_2 plasma precleaning for 15 min at the substrate temperature of 300°C was tried next after establishing that plasma precleaning and long time low temperature postmetallization annealing improve the electrical properties. V_{fb}, D_f and D_{it} values of the films deposited after plasma precleaning using these gases and 40 min annealing are summarized in Table 3. It can be observed that while the electrical properties of the films deposited on N_2 and H_2 plasma precleaned wafers are comparable to those of dry thermal oxide films, there is a significant reduction in the values of the electrical properties of PECVD oxide films deposited on the O_2 plasma precleaned wafers. This has also been reported by Gereth and Scherber[25] for their plasma nitride films precleaned by O_2 plasma. But these films on O_2 plasma precleaned wafers showed hysteresis behaviour on performing retrace, and shift in V_{fb} was observed upon bias stress application of ± 10 V for 10 min each of as much as 0.9 V. This makes O_2 plasma precleaning, which adds diffusion-limited plasma oxide of up to 45 Å in 15 min[25], an unsuitable process. Figure 1 shows the bias stress instability.

PECVD SiO_2 films deposited on N_2 plasma precleaned wafers showed no hysteresis on retrace but showed bias stress instability. With an application of 10 V bias stress for 1 min, the V_{fb} shifted by 0.5 V towards the negative voltage axis of the C–V plot and with a -10V bias stress for 1 min, the V_{fb} shifted by 0.3 V towards the negative voltage axis of the C–V plot. This made N_2 plasma precleaning also unsuitable.

Films deposited on H_2 plasma precleaned wafers show values of the electrical properties comparable to those of the dry thermally grown oxide. Also, the films show no hysteresis and no shift in V_{fb} upon bias

Table 3. Values of the electrical properties of films deposited after N_2, H_2 and O_2 plasma precleaning at 300°C. The devices fabricated were annealed for 40 min

	Plasma precleaning gas at 300°C		
Electrical properties	N_2	H_2	O_2

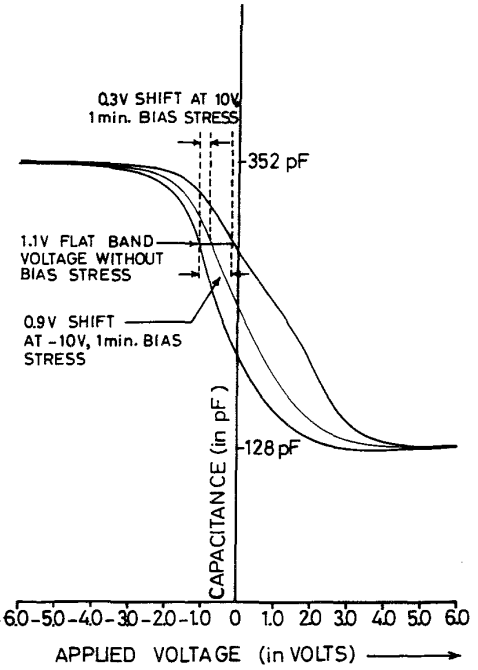

Fig. 1. C–V plot of the MOS test structure fabricated on the deposited film after O_2 plasma precleaning, showing shift in flatband voltage upon bias stress application.

stress application. This makes H_2 plasma precleaning a suitable process in the deposition of PECVD SiO_2. H_2 plasma is also known to etch SiO_2[27] and Si[28–30]. So after etching the native oxide during precleaning, it can go on to etch the underlying Si resulting in roughening the Si surface and some H incorporation in the bulk[31]. To avoid this etching of the underlying Si, the time of exposure of the wafer to the H_2 plasma needs to be controlled. This is difficult. A remedy for this difficulty was thought to be the use of CF_4/50% H_2 plasma in place of H_2 plasma, which can eliminate Si etching due to high H_2 content[32]. CF_4/H_2 plasma was tried next for 1 min preceded by N_2 plasma precleaning for 15 min but with unfavourable end result. In the high pressure mode of the plasma reactor, etching is known to be performed by the neutral species[33]. In our case, the HF formed in the CF_4/H_2 plasma etches the native oxide without etching the underlying Si. Larger V_{fb} (up to -4.0 V), D_f and D_{it} values were observed although there was no hysterisis or shift in V_{fb} upon bias stress application. CF_4/50% H_2 plasma precleaning was followed by O_2 plasma exposure of the wafer for 10 min at 0.6 mbar total pressure, *in situ*, on another wafer because O_2 plasma precleaning had shown to significantly improve the V_{fb}, D_f and D_{it} values (Table 3) earlier. No diffusion-limited plasma oxide growth resulted as shown by the un-

after CF_4/H_2 plasma precleaning. This is possibly due to the formation of thin carbon containing fluorocarbon film that does not allow O atoms to react with Si during O_2 plasma exposure of the wafer[34]. The reactor configuration being in the high pressure mode did not allow support of ionic bombardment to clear the above film as it happens in the reactive ion etching low pressure mode due to the presence of negative self-bias on the insulated electrode.

Choosing a substrate temperature for deposition has not been given enough importance in the past. In previous research one or two particular substrate temperatures have been chosen for deposition with no particular reason indicated for the choice[14,16,18–20]. All the mentioned references only indicate a varying upper limit and a consensus exists that it is less than or equal to 400°C. Adams *et al.*[15] has systematically varied the substrate temperature from 100–340°C and has studied the variation in film properties like refractive index, stress, etch rate, density and deposition rate. Most of these properties have shown a transition temperature of 200°C beyond which the properties either become stable or are better than for those below 200°C. Based on this, the lower limit on the choice of substrate temperature can be set to 200°C although, in view of these properties, a higher temperature can also be chosen. In the present work, the substrate temperature has also been varied systematically from 200–400°C in steps of 50°C, keeping in mind the 200°C as the lower limit from the works of Adams *et al.*[15], and the electrical properties have been studied. The deposited oxide on wafers with no plasma precleaning show a strong but random dependence of these properties on the substrate temperature as indicated in Table 1. However, the following observations have to be made further in this regard:

1. $V_{fb} = -2.19$ V, deposition temperature = 250°C, total annealing time = 40 min, Ar plasma precleaning used, value indicated in Table 2.
2. $V_{fb} = -2.02$ V, deposition temperature = 350°C, total annealing time = 40 min, Ar plasma precleaning used, value indicated in Table 2.
3. $V_{fb} = -1.95$ V, deposition temperature = 300°C, total annealing time = 40 min, N_2 plasma precleaning used, value indicated in Table 3.
4. $V_{fb} = -2.08$ V, deposition temperature = 300°C, total annealing time = 40 min, H_2 plasma precleaning used, value indicated in Table 3.

All these V_{fb} values are almost the same for deposition temperatures of 250, 300 and 350°C. These V_{fb} values reflect on the values of D_f and the corresponding D_{it} values are also very close to each

that the substrate temperature can be chosen from 200–350°C, where 200°C lower limit has been decided by the earlier argument from the works of Adams *et al.*[15], and provided long time low temperature postmetallization annealing and plasma precleaning has been performed.

Density close to 2.27 g/cm^3 (pure SiO_2) is essential in device applications as it is related to the physical and electrical properties, where lower density may give inferior properties. Densification may be needed, or will occur, only if the density of the deposited film is less than 2.27 g/cm^3. The density of the deposited film in the works of Pan *et al.*[16] was low and after 1000°C post-oxidation anneal in N_2, the value approached 2.27 g/cm^3, keeping in mind that only the stoichiometric films have to be considered (first two values in Table 2[16]). The density of the deposited film in the work of Adams *et al.*[15] was higher than 2.27 g/cm^3 and after long time (1 h) low temperature (400°C) annealing in air, the film became less dense, again approaching 2.27 g/cm^3. Hollahan[14] has shown that when pure gases were used, as in our case, having high deposition rates, the densities of the deposited films were higher and after dilution with Ar, which lowers the deposition rate, the density of the film reduced drastically. This is contrary to the claim made by Batey and Tierney[19] that having lower deposition rates due to dilution with inert gas, gives denser films. Also, Adams *et al.*[15] used deposition rates of 200–360 Å/min (much higher compared to 50–60 Å/min rates in the works of Batey and Tierney[19]) involving 47.2% Ar dilution in the total gas flow and have achieved higher density films (> 2.27 g/cm^3) which after long time low temperature annealing reduces to near 2.27 g/cm^3. This supports the above mentioned contradiction. It has also been reported[15] that the density is nearly independent of all deposition variables, except power, and high film densities are observed for low powers. The authors in the present work have used 50 RF W power, which is low. Annealing affects the density significantly and in order to retain the low temperature advantage, long time low temperature postmetallization annealing is an alternative to high temperature postoxidation anneal. The authors have taken this approach and have shown the importance of postmetallization annealing for a further 30 min at 450°C in N_2 ambient by evaluating the values of the properties after 10 min annealing, which is usually needed for good contact. The density will approach 2.27 g/cm^3 anyway and use of low power and long time low temperature annealing seems to be the method for achieving that. With this in view, the density of the films processed in the present study is expected to be near 2.27 g/cm^3.

4. CONCLUSION

It is concluded from the experimental results that PECVD SiO_2 deposited using pure N_2O/SiH_4 mixture

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