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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/900,047 07/24/97 YEN

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EXAMINER

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ART UNIT PAPER NUMBER

2503


DATE MAILED:

02/24/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

<b>Office Action Summary</b>	Application No. <b>08/900,047</b>	Applicant(s) <b>Yen</b>
	Examiner <b>Valencia Martin Wallace</b>	Group Art Unit <b>2503</b>



Responsive to communication(s) filed on Jan 9, 1998.

This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claims**

Claim(s) 2-6 and 8-17 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

Claim(s) \_\_\_\_\_ is/are allowed.

Claim(s) 2-6 and 8-17 is/are rejected.

Claim(s) \_\_\_\_\_ is/are objected to.

Claims \_\_\_\_\_ are subject to restriction or election requirement.

**Application Papers**

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

The proposed drawing correction, filed on \_\_\_\_\_ is  approved  disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All  Some\*  None of the CERTIFIED copies of the priority documents have been

received.

received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

Notice of References Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

**Claims 4-6 and 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claims 4-6 and 10-12 recite the limitation "said electrically conducting plug". There is insufficient antecedent basis for this limitation in the claims.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

**Claims 3-6 and 9-14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chappell et al. (U.S. Patent No. 5,541,427).**

Chappell et al. disclose a semiconductor structure and a method of forming a local interconnect in a semiconductor structure, comprising:

a silicon substrate (10) having a top surface;

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a diffusion region (43) formed in said substrate adjacent to said top surface;

a polysilicon gate (18) formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region;

a sidewall spacer (28) adjacent to said polysilicon gate and disposed above said diffusion region;

an insulator layer (36) substantially covering said polysilicon gate and said diffusion region; and

a conducting plug (44a) at least partially filling a via in said insulation layer that exposes said sidewall spacer in the absence of said conducting plug, said conducting plug providing direct electrical communication between said polysilicon gate and said diffusion region. Note Chappell et al. Figure 8.

In re claims 3 and 9, said insulator layer is formed of a material such as silicon oxide (see Chappell et al. column 4, lines 23 and 24).

In re claims 4-6 and 10-12, said conducting plug is a metal plug formed of a refractory material such as tungsten (see Chappell et al. column 4, lines 66 and 67).

In re claim 16, said polysilicon gate and said diffusion region are exposed in said via in the absence of said conducting plug (see Chappell et al. Figure 5).

Therefore, Chappell et al. meet and anticipate the claims.

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***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 2, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. in view of Jones, Jr. (U.S. Patent No. 5,313,089), of record.**

The disclosure of Chappell et al. as discussed above. However, Chappell et al. fail to disclose forming the conductive plug with both a refractory metal layer and a layer of glue.

Therefore, to provide the device of Chappell et al. with a conductive plug comprised of an outer glue layer and a plug of a refractory metal as taught by Jones, Jr. would have been obvious to one of ordinary skill in this art because Jones, Jr. specifically teaches the process of forming a semiconductor device similar in structure and function to that of Chappell et al. having a conductive plug (32) within a dielectric layer (30) wherein said plug has a layer of glue and a plug of tungsten, as well known and commonly used in conductive plug technology (see Jones, Jr. column 3, lines 64-68 and column 4, lines 1-17). Note Jones, Jr. Figure 2.

Also, it is obvious that the diffusion regions of Chappell et al. would be of N or P type conductivity because Chappell et al. specify that the regions are. Further, Jones, Jr. specify that the diffusion regions (16, 18) are heavily doped with an impurity (see Jones, Jr. column 3, lines 23-24).

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