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**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Application of: | Ting P. Yen |
| Serial No.: | 08/561,951 |
| Title: | METAL PLUG LOCAL INTERCONNECT |
| Filed: | November 22, 1995 |
| Attorney Docket No.: | 0325.00004 |
| Examiner: | V. Wallace |
| Art Unit: | 2503 |
| In Response To: | Office Action mailed November 7, 1996 |



**AMENDMENT PURSUANT TO 37 C.F.R. § 1.116**

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed November 7, 1996, please consider the following amendment and remarks regarding the above-captioned patent application to place the patent application in condition for allowance.

**IN THE CLAIMS**

Please amend the claims as follows:

13. (AMENDED) A semiconductor structure comprising:

a silicon substrate having a top surface,

a diffusion region formed in said substrate adjacent to said top surface,

a polysilicon gate formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region,

a sidewall spacer adjacent to said polysilicon gate and disposed above said diffusion region,

an insulator layer substantially covering said polysilicon gate and said diffusion region, and

a conducting plug at least partially filling a via in said insulation layer that exposes said sidewall spacer in the absence of said conducting plug, said conducting plug providing direct electrical communication between said polysilicon gate and said diffusion region.

14. (AMENDED) A method of forming a local interconnect in a semiconductor structure, comprising the step of:

depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to

but not contacting said diffusion region, said sidewall spacer being disposed above said diffusion region, said via being in an insulating material on said gate.

**SUPPORT FOR AMENDMENTS**

Support for the above amendments can be found in FIG. 3B as originally filed along with United States Patents 4,566,175; 4,878,100; 4,962,060; 5,202,279; 5,286,674; and 5,521,118 and Wolf, Silicon Processing for the VLSI Era, Volume 2, pp. 144-145, 212-214, and 354-355 filed with the accompanying Information Disclosure Statement.

**R E M A R K S**

**Rejection Under 35 U.S.C. § 102(e)**

The rejection of claims 2-6, 8-14 and 16-17 under 35 U.S.C. § 102(e) as being anticipated by United States Patent 5,541,434 (hereinafter "Nicholls et al.") is respectfully traversed and should be withdrawn.

Nicholls et al. discloses a contact for electrically connecting adjacent portions within a semiconductor device. Nicholls et al. discloses a silicon substrate 52, a diffusion region 70, a polysilicon gate 56 which does not physically touch the diffusion region 70, a dielectric region 74, a contact via 76 and an electrically conducting plug 80. Nicholls et al. does not, however, disclose a sidewall spacer adjacent to the polysilicon

gate 56 and disposed above the diffusion region 70 in the via containing the electrically conducting plug 80. In fact, Nicholls et al. discusses etching the sidewall spacer out of the via containing the conducting plug, thus appearing to lead one of ordinary skill in the art away retaining a side wall spacer in this position. (Column 5, lines 15-20.)

Claims 13 and 14, as amended, recite a sidewall spacer adjacent to the polysilicon gate and disposed above the diffusion region in the via containing the conducting plug. Therefore, the present claims 13 and 14 overcome the rejection under 35 U.S.C. § 102(e).

**REJECTIONS UNDER 35 U.S.C. 103**

The rejection of Claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Nicholls et al. in view of United States Patent 5,313,089 (hereinafter "Jones, Jr.") is respectfully traversed.

Jones, Jr. discloses a semiconductive device including a conductive plug region 32. Glue layers are generically identified as being used in conductive plug technology.

Jones is silent with regard to a conducting plug providing electrical communication between a polysilicon gate and a diffusion region. Therefore, Jones, Jr. fails to cure the

deficiencies of Nicholls et al. with regard to the presently claimed invention. Furthermore, one ordinary skill in the art would not be motivated to include a sidewall spacer adjacent to a polysilicon gate and disposed above a different region in a via containing or to subsequently contain a conducting plug. One might reasonably expect a sidewall spacer to reduce the available surface area for direct ohmic contact between the polysilicon gate and the diffusion region thus reducing the likelihood for success, particularly when the sidewall spacer comprises an oxide, a well-known electrical insulator (see, e.g., Wolf). Therefore, the rejection under 35 U.S.C. § 103(a) should be withdrawn.

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