



United States Patent [19]
Sakamoto

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[54] CONTACT STRUCTURE OF AN INTERCONNECTION LAYER FOR A SEMICONDUCTOR DEVICE AND A MULTILAYER INTERCONNECTION SRAM

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Related U.S. Application Data

[63] Continuation of Ser. No. 845,980, Mar. 4, 1992, abandoned.

[30] Foreign Application Priority Data

Mar. 15, 1991 [JP] Japan 3-050954
Jan. 14, 1992 [JP] Japan 4-005222

[51] Int. Cl. H01L 27/11; H01L 29/786; H01L 29/417; H01L 29/43

[52] U.S. Cl. 257/67; 257/69; 257/377; 257/384; 257/755; 257/756; 257/903

[58] Field of Search 257/51, 67-69, 257/369, 377, 754-756, 903, 904, 752, 382-384, 385

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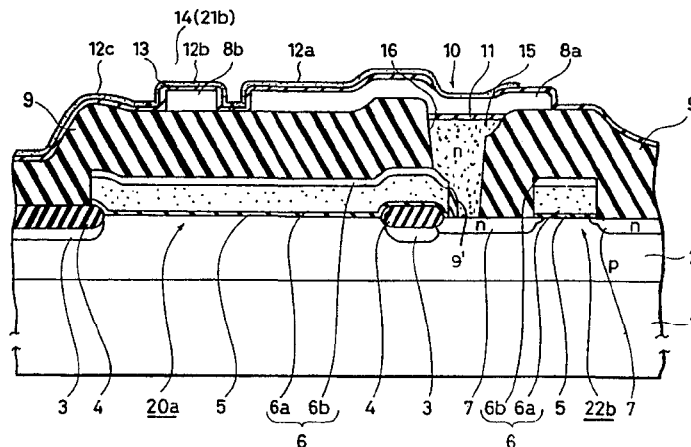
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Attorney, Agent, or Firm—Lowe, Price, LeBlanc & Becker

[57] ABSTRACT

A silicon layer in a lower layer and an interconnection layer arranged in an upper layer are electrically connected through an opening for contact. A silicon plug layer having the same conductivity type as that of the silicon layer is embedded in the opening. The silicon plug layer is embedded in the opening by an etch back method after deposited using a CVD method. The interconnection layer in the upper layer has conductivity type different from that of the silicon plug layer. A refractory metal silicide layer is formed between the upper interconnection layer and the silicon plug layer.

The refractory metal silicide layer prevents pn junction from being formed between the upper interconnection layer and the silicon plug layer.

9 Claims, 23 Drawing Sheets



INTEL 1103

FIG. 2

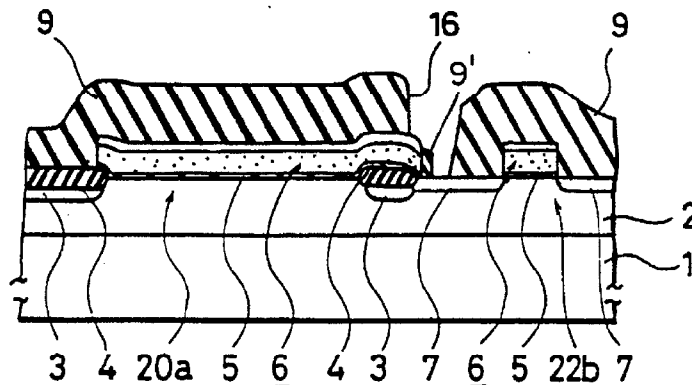


FIG. 3

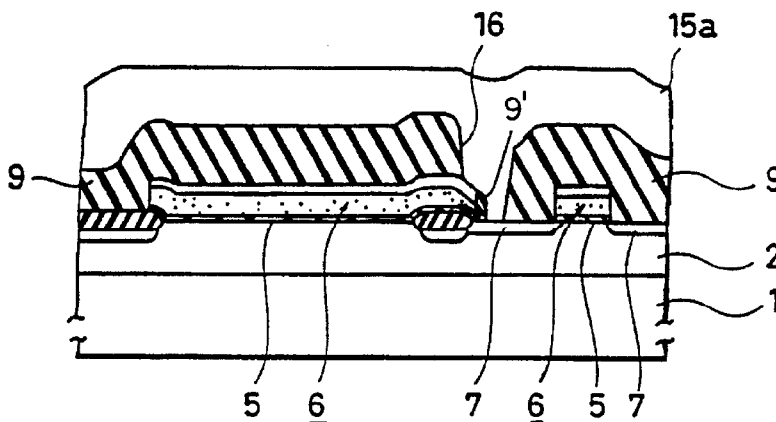


FIG. 4

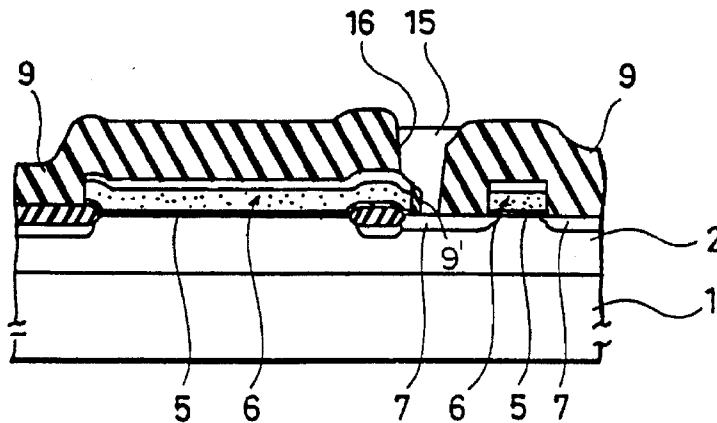


FIG. 5

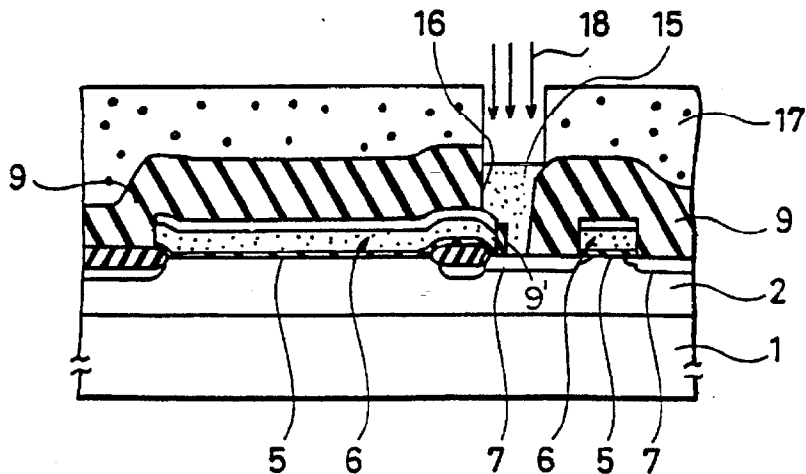


FIG. 6

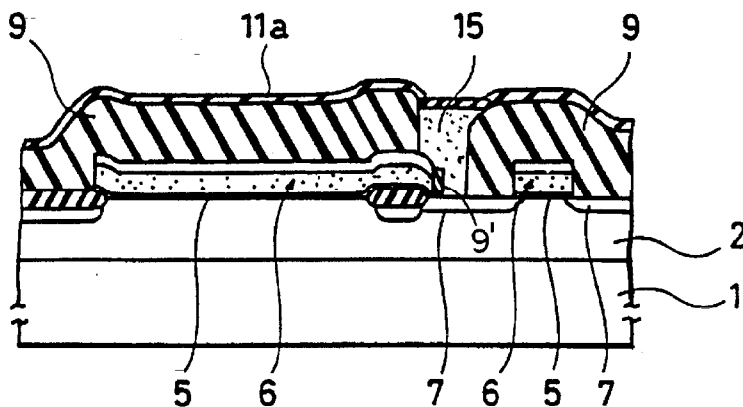


FIG. 7

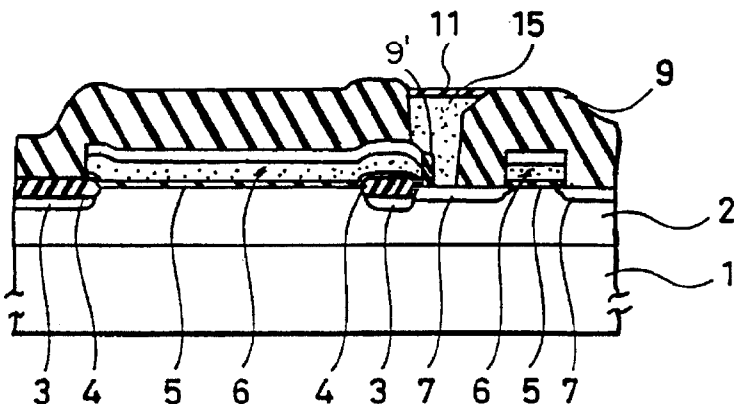


FIG. 8

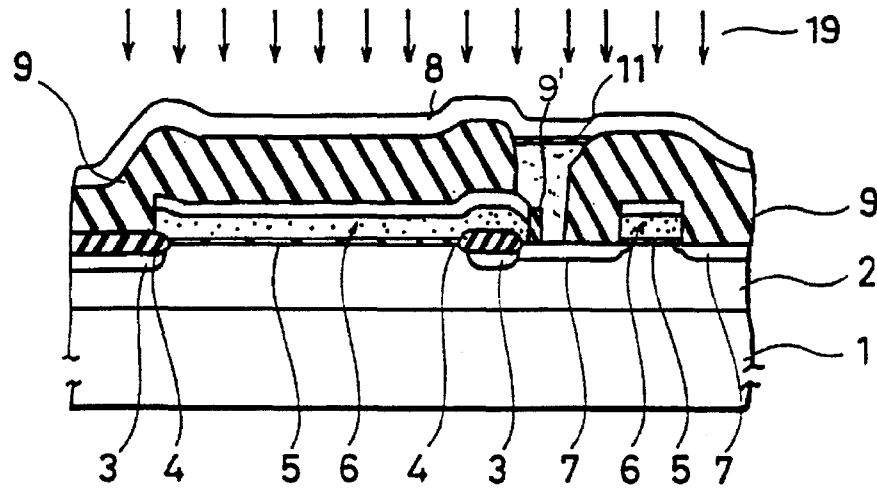
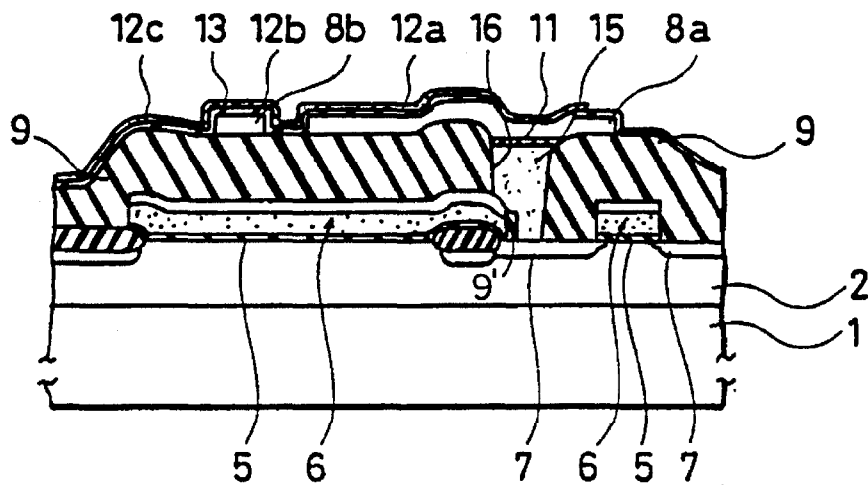


FIG. 9



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