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Paper 10
Date Entered: June 8, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2016-00290
Patent 5,965,924

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and MINN CHUNG, *Administrative Patent Judges.*

McNAMARA, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

BACKGROUND

Intel Corporation ("Petitioner") filed a petition, Paper 2 ("Pet."), to institute an *inter partes* review of claims 7–12, 15, and 17 (the "challenged claims") of U.S. Patent No. 5,965,924 ("the '924 Patent"). 35 U.S.C. § 311. DSS Technology Management, Inc. ("Patent Owner") waived filing a Preliminary Response. Paper 7. We have jurisdiction under 37 C.F.R. § 42.4(a) and 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Having considered the arguments and the associated evidence presented in the Petition, for the reasons described below, we institute *inter partes* review of claims 7–12, 15 and 17.

REAL PARTIES IN INTEREST

Petitioner identifies itself as the only real party-in-interest. Pet. 5.

PENDING LITIGATION

The parties state that Patent Owner has asserted '924 Patent in the following litigation: (1) *DSS Technology Management, Inc. v. Intel Corp.*, No. 6:15-CV-130-RWS (E.D. Tex. filed Feb. 16, 2015); and (2) *DSS Technology Management, Inc. v. Qualcomm Inc.*, No. 6:15-CV-692-JRG (E.D. Tex. filed July 16, 2015). Pet. 5; Paper 6, at 2.

Petitioner notes that it has filed a separate petition for *inter partes* review of claims 1–6, 13, 14, and 16 of the '924 Patent. Pet. 5. That proceeding has been designated IPR2016-00289. Paper 6, at 3.

THE ’924 PATENT (EXHIBIT 1101)

The ’924 Patent relates to semiconductor fabrication in general, and in particular concerns a metal plug local interconnect that is formed in the same process of forming metal plugs that are already designed as sub-metal plugged contacts. Ex. 1101, col. 1, ll. 9–11. The ’924 Patent discloses that in semiconductor fabrication, it is often necessary to make a local interconnect between a gate polysilicon layer to N+ or P+ diffusion regions. *Id.* at col. 1, ll. 16–17. According to the ’924 Patent, conventionally such local interconnects were fabricated using buried contacts, as shown in Figures 1A and 1B of the ’924 Patent (*id*. at col. 1, l. 25–col. 2, l. 11) or with a metallic local interconnect strap to shunt from a gate polysilicon to a diffusion region, as illustrated in Figures 2A and 2B of the ’924 Patent (*id.* at col. 2, l. 12–41).

The ’924 Patent discloses a semiconductor structure in which a diffusion region is formed in a silicon substrate and a polysilicon gate is formed on the top surface of the silicon substrate adjacent to, but not contacting, the diffusion region. Ex. 1101, col. 3, ll. 1–6, 14–18. A layer of insulating material is then deposited on top of the polysilicon gate and the diffusion region. *Id*. at col. 3, ll. 6–7, 19–20. A via opening is formed in the insulating material to expose a portion of the polysilicon gate and a portion of the diffusion region. *Id*. at col. 3, ll. 7–8, 20–22. An electrically conducting material is deposited to at least partially fill the via opening to provide an electrical connection between the polysilicon gate and the diffusion region. *Id*. at col. 3, ll. 8–11, 23–27.

ILLUSTRATIVE CLAIM

7. A method of forming a local interconnect in a semiconductor structure, comprising the step of:

depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said sidewall spacer being disposed above said diffusion region, said via being in an insulating material on said gate.

ART CITED IN PETITIONER'S CHALLENGES

Petitioner cites the following references in its challenges to patentability:

Sakamoto, U.S. Patent No. 5,475,240 issued Dec. 12, 1995, Ex. 1103 ("Sakamoto"); and

Cederbaum et al., U.S. Patent No. 5,100,817 issued Mar. 31, 1992, Ex. 1104 ("Cederbaum").

CHALLENGES ASSERTED IN PETITION

Claims	Statutory Basis	Challenge
7–9, 15, and 17	35 U.S.C. § 102(e)	Anticipation by Sakamoto
10–12	35 U.S.C. § 103	Obviousness over the combination of Sakamoto and Cederbaum

CLAIM CONSTRUCTION

The '924 Patent issued from an application that was a continuation of Appl. No. 08/561,951 filed on Nov. 22, 1995. Thus, the '924 Patent is expired. We construe the claims of an expired patent in accordance with the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("While claims are generally given their broadest possible scope during prosecution, the Board's review of the claims of an expired patent is similar to that of a district court's review."). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Only those terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

The only term Petitioner proposes we construe is "diffusion region in a silicon substrate." Pet. 23–26. Petitioner proposes that we construe this term to mean "conductive terminal region, such as a source or drain, that contains dopants implanted in the silicon substrate." *Id*. at 26. Petitioner states that in the co-pending litigation Patent Owner has proposed "diffusion region in a silicon substrate" be construed to mean a "conductive terminal region such as a source or drain in a silicon substrate." *Id*. at 24. Petitioner cites the portion of the '924 Patent specification referencing Figures 3A and 3B that discloses that diffusion regions 70 and 72 of either N+ or P+ doping are formed by an ion implantation in the surface of the silicon substrate 74 in

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