IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	TING P. YEN	Group Art Unit: 2503
Serial No.:	08/561,951	Examiner: WALLACE, V.
Filed:	November 22, 1995	In Response to Office Action of: April 17, 1996
For:	METAL PLUG LOCAL INTERCONNECT	Paper No. 2
Attorney Docket No.:	64,663-004	

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Date: August 14, 1996

Ellen Psujek
Ellen Psujek
(Signature of person mailing paper)

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Dear Sir:

In response to the Office Action mailed April 17, 1996, please consider the following amendments and remarks regarding the above-identified application.

IN THE CLAIMS

Please cancel claims 1 and 7, and replace with the new claims 13 and 14.

13. A semiconductor structure comprising:

a silicon substrate having a top surface,

a diffusion region formed in said substrate adjacent to said top surface,

a polysilicon gate formed on the top surface of said substrate juxtaposed to but not contacting said diffusion region,

an insulator layer substantially covering said polysilicon gate and said diffusion region, and

a conducting plug at least partially filling a via in said insulation layer, providing direct electrical communication between said polysilicon gate and said diffusion region.

14. A method of forming a local interconnect in a semiconductor structure, comprising the step of:

depositing an electrically conducting material in a via exposing at least a portion of a gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said via being in an insulating material on said gate.

Amend claims 2~6 and 8~12 as follows:

Claim 2, line 1, delete "claim 1", and substitute therewith --claim 13--.

Claim 3, line 1, delete "claim 1", and substitute therewith --claim 13--.

Claim 4, line 1, delete "claim 1", and substitute therewith --claim 13--.

Claim 5, line 1, delete "claim 1", and substitute therewith --claim 13--.

Claim 6, line 1, delete "claim 1", and substitute therewith --claim 13--

Line 4, delete "and molybdenum", and substitute therewith --, molybdenum and tungsten--.

Claim 12, line 3, delete "and molybdenum" , and substitute therewith --, molybdenum and tungsten--.

Add new claims 15~17.

13

~~15.~~ A semiconductor structure according to claim ~~13~~ 1, wherein said conducting plug comprises an outer glue layer and a plug material therein.

14

~~16.~~ A semiconductor structure according to claim ~~13~~ 1, wherein said polysilicon gate and said diffusion region being exposed in said via in the absence of said conducting plug.

12

15

~~17.~~ A method according to claim ~~14~~ 7, wherein said gate is a polysilicon gate.

REMARKS

Claims 1 and 7 have been canceled. New claims 13~17 have been added. Thus claims 2~6 and 8~17 are now pending. No new matter is added by the present amendment.

Support for the amendment to claims 6 and 12 can be found in the specification at p. 10, lines 10-11; p. 11, step 24; p. 12, step 17 and p. 13, step 24.

Support for claim 15 can be found in the specification at p. 11, steps 23~24; p. 13, steps 23~24; p. 12, steps 16~17 and Figure 3B.

Rejection Under 35 USC §102(a)

The rejection of Claims 1~12 under 35 USC §102(a) as being anticipated by Kinoshita, U.S. Patent No. 5,453,640, is respectfully traversed.

Kinoshita teaches a contact hole formed in an insulating layer over a diffusion region, and a conducting tungsten plug fills the contact hole. Kinoshita further teaches a block of static memory cells using CMOS transistors, wherein metal interconnections, e.g.,ground lines for the CMOS transistors, are simplified by using buried layers in the substrate. Buried tungsten contacts in the memory cell form connections of the n-MOS and p-MOS transistor diffusion layers to underlying layers of opposite conductivities. Kinoshita further uses supply voltage or ground potential to each buried layer from the substrate surface by using additional buried contacts which are made at convenient locations outside the memory block. As shown in Kinoshita's Figure 5, the

diffusion region 46 and the polysilicon gate electrode 26 are adjacent but not in contact with each other. A tungsten contact plug fills the contact hole 32 for making electrical contact only with the diffusion region 46 (and not with the gate electrode 26).

The applicant's claims 1~12 are not anticipated by Kinoshita '640. To anticipate a claim of a patent, a single source must contain all its essential elements. See, e.g., *Tights, Inc. v. Acme-McCrary Corp.*, 191 USPQ 305 (4th Cir. 1976).

Kinoshita fails to teach a plug that contacts and provides electrical communication between a polysilicon gate and a diffusion region in a via opening exposing the gate and the diffusion region in the absence of the plug. Instead insulating layer 38 of silicon oxide or silicon nitride prevents polysilicon gate electrode 26 from being exposable or exposed in contact hole 32 (see Figure 5 of Kinoshita).

Therefore, Kinoshita does not anticipate the present invention. Withdrawal of the rejections of claims 1~12 under 35 USC §102(a) is respectfully requested.

Rejection under 35 USC §102(b)

The rejection of Claims 1~12 under 35 USC §102(b) as being anticipated by Nishigoori, U.S. Patent No. 5,245,210, is respectfully traversed.

Nishigoori '210 discloses a MOS type semiconductor device which has a contact hole

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