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United States Patent [19]

Kinoshita

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[54] **SEMICONDUCTOR INTEGRATED CIRCUIT HAVING MOS MEMORY AND BIPOLAR PERIPHERALS**

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[73] Assignee: **NEC Corporation**, Tokyo, Japan

[21] Appl. No.: **359,996**

[22] Filed: **Dec. 20, 1994**

[30] **Foreign Application Priority Data**

Dec. 22, 1993 [JP] Japan 5-322996

[51] **Int. Cl.**[6] **H01L 29/06**; H01L 27/11; H01L 27/04

[52] **U.S. Cl.** **257/520**; 257/903; 257/904; 257/377; 257/382; 257/384; 257/383; 257/515

[58] **Field of Search** 257/903, 904, 257/734, 301, 304, 349, 360, 361, 370, 371, 394, 377, 382, 383, 384, 396, 397, 510, 515, 520, 902

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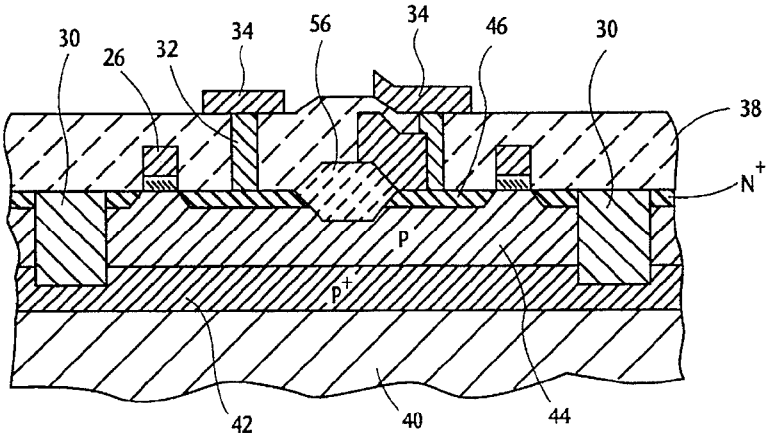
Primary Examiner—Mahshid D. Saadat
Assistant Examiner—Alexander Oscar Williams
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

In a semiconductor integrated circuit having a block of static memory cells using CMOS transistors and peripheral components using bipolar transistors, metal interconnections in a layer over the CMOS transistors on the substrate are simplified by using buried layers in the substrate as supply and ground lines for the CMOS transistors. This is accomplished by making buried contacts of a metal such as tungsten in each memory cell to make ohmic connection of the diffused layer of n-MOS transistors and the diffused layer of p-MOS transistors respectively to underlying buried layers of opposite conductivities and applying supply voltage or ground potential to each buried layer from the substrate surface by using additional buried contacts which are made at convenient locations outside the memory block. In the case of n-MOS memory cells using resistors or TFTs as load elements, ground potential is applied to the n-MOS transistors by the same method.

8 Claims, 7 Drawing Sheets



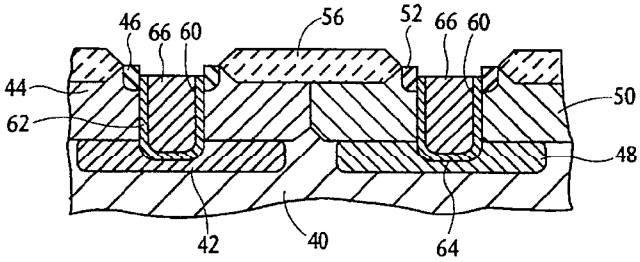


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FIG. 1 PRIOR ART

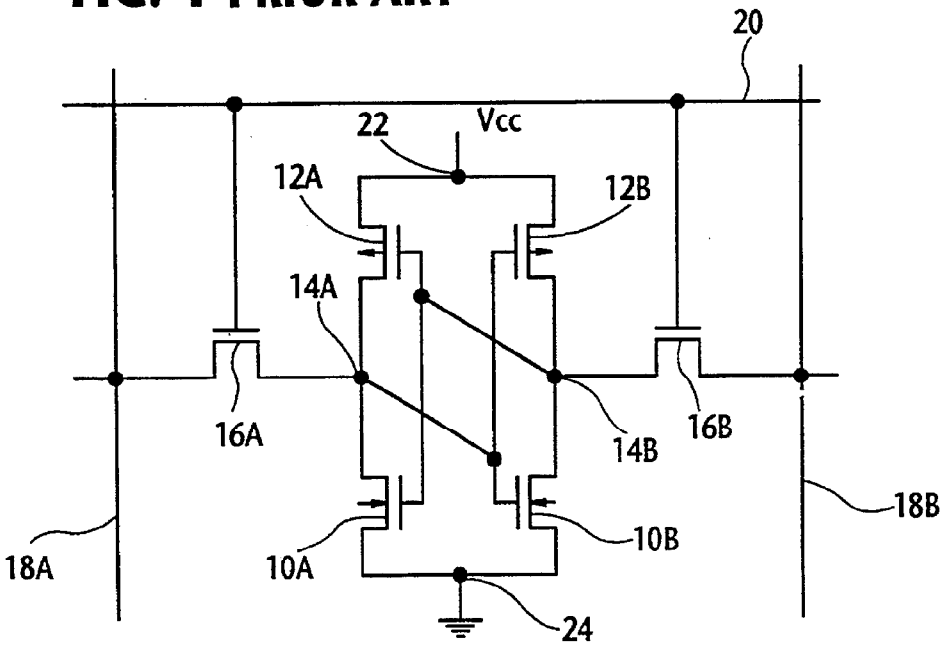


FIG. 2

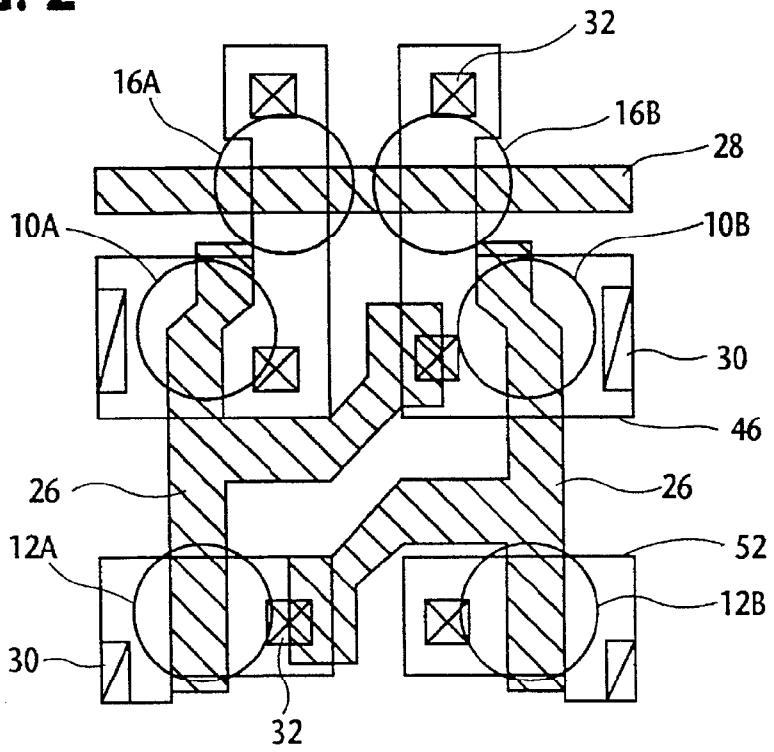


FIG. 3

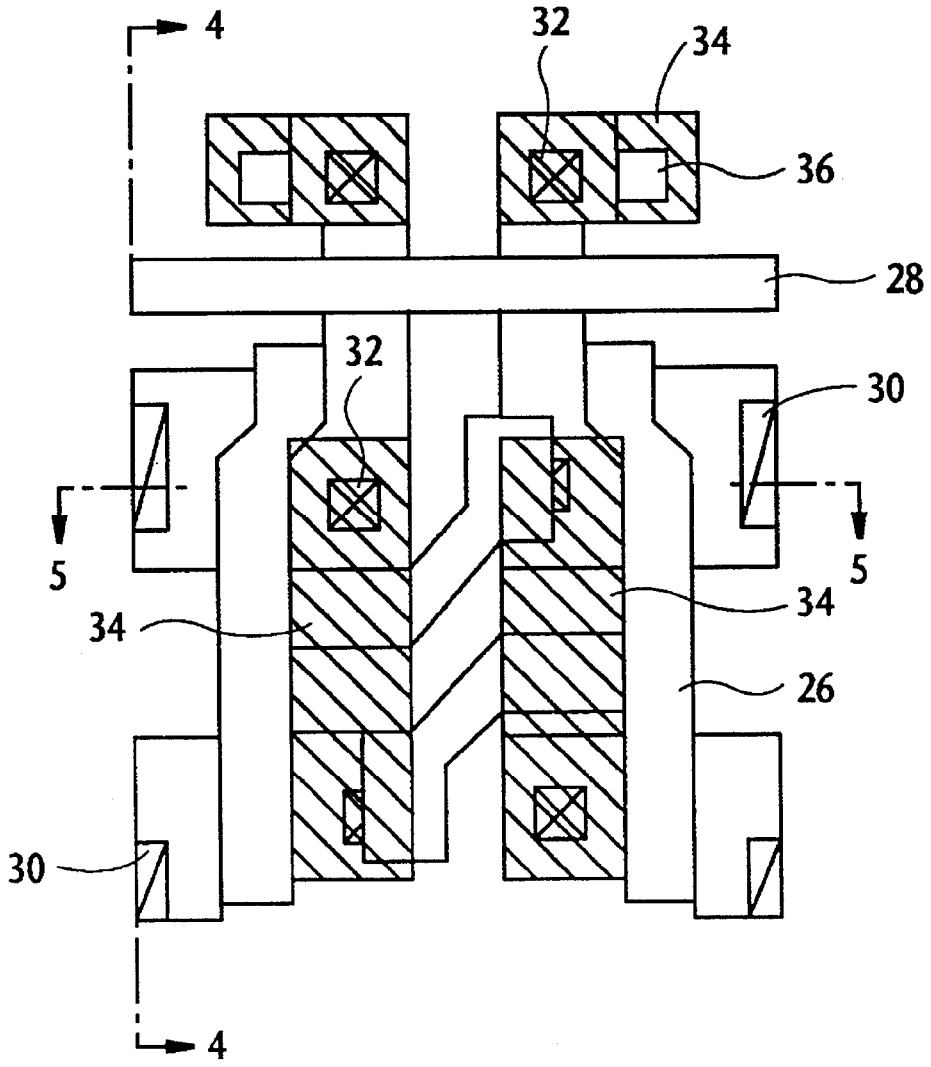


FIG. 4

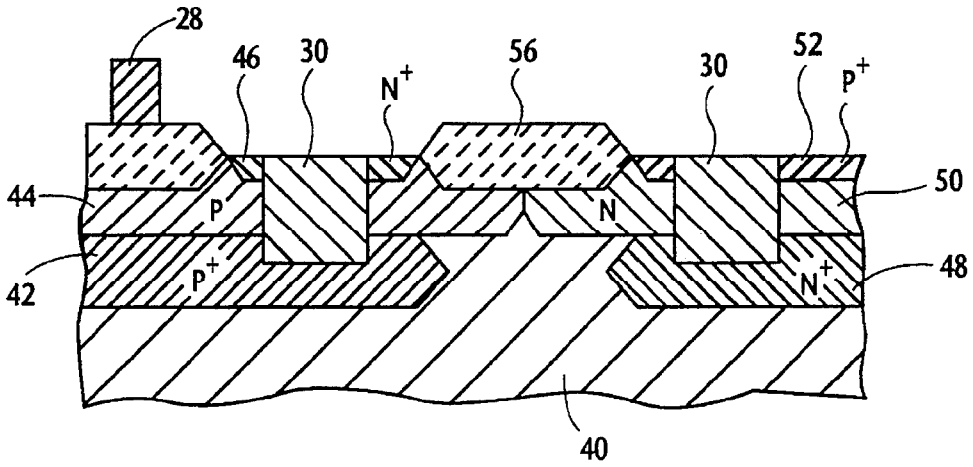


FIG. 5

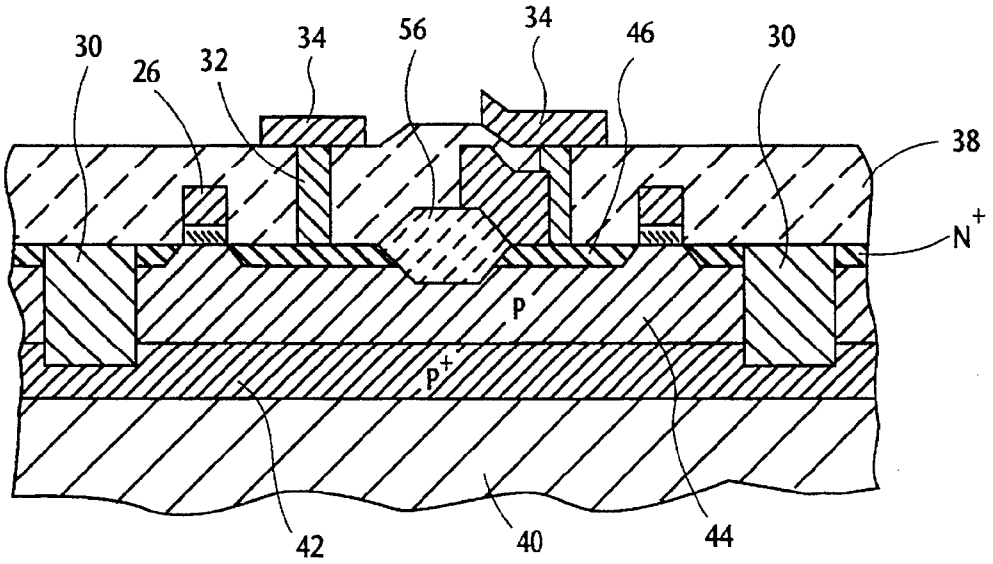


FIG. 6

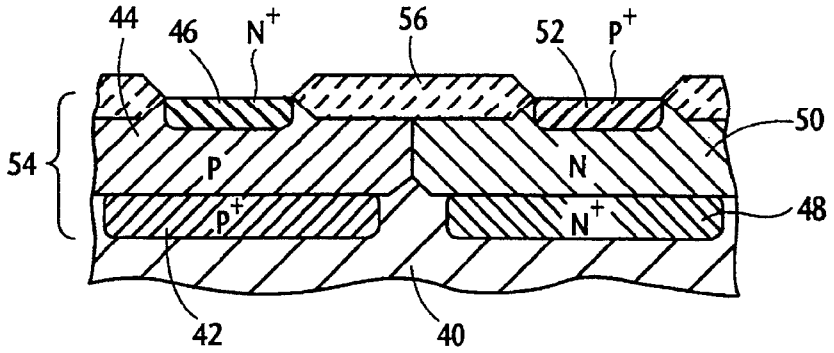


FIG. 7

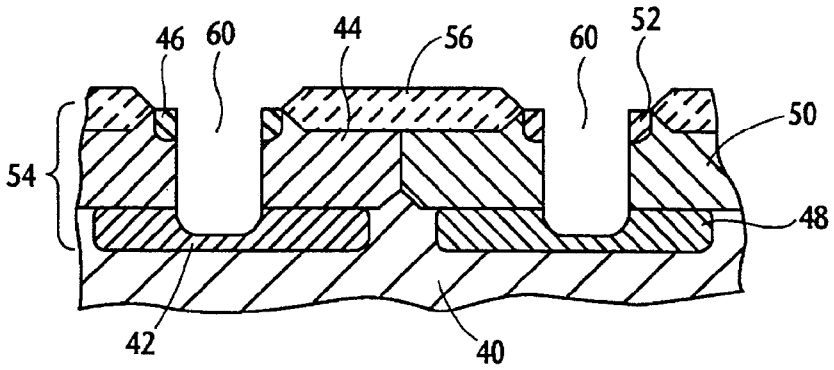


FIG. 8

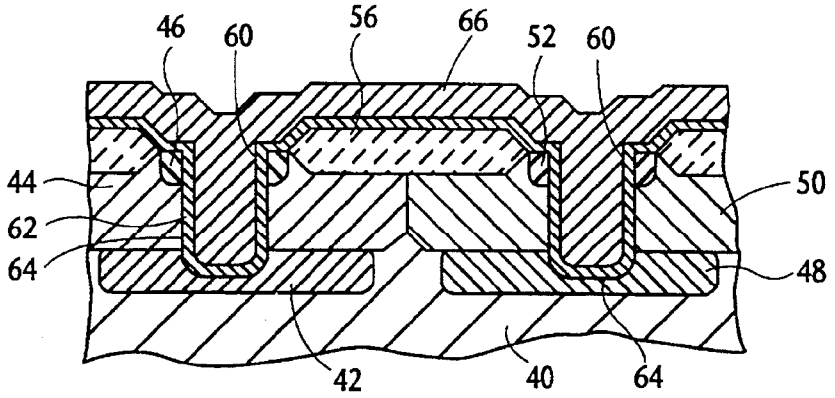
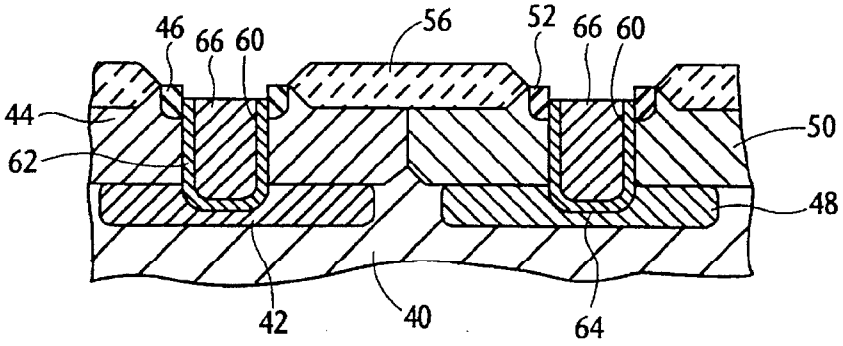


FIG. 9



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