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United States Patent [19]

Chappell et al.

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[54] SRAM CELL WITH CAPACITOR

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[21] Appl. No.: **162,588**

[22] Filed: **Dec. 3, 1993**

[51] **Int. Cl.**[6] **H01L 27/108**; H01L 27/11

[52] **U.S. Cl.** **257/306**; 257/374; 257/397; 257/513; 257/752; 257/903

[58] **Field of Search** 257/513, 752, 257/903, 374, 397, 904, 306

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[57] **ABSTRACT**

A storage latch comprising a gate insulating layer over the substrate, shallow trenches formed through the insulating layer and in the substrate to provide device insulation; and doped regions in the substrate between the shallow trenches. The doped regions define sources and drains. Gate stacks are formed over regions of oxide adjacent the doped regions. A planarized insulator is formed between the gate stacks. Openings are provided in the planarized insulator for contacts to the doped regions and the gate stacks. Conductive material fills the openings to form contacts for the doped regions and for the gate stacks. A patterned layer of conductive material on the planarized insulator connects selected ones of the contacts for wiring portions of the latch. A six device SRAM cell comprises a deep isolation trench formed in the substrate; a first latch including two transistors formed of p-type material on a first side of the trench; a second latch including two transistors formed of n-type material on a second side of the trench opposite the first side of the trench, and connection means for electrically cross wiring the transistors of the first latch to the transistors of the second latch. In forming the latch a self-aligned process for separately forming contacts to diffusion regions and gate stacks on the semiconductor substrate is used.

1 Claim, 8 Drawing Sheets

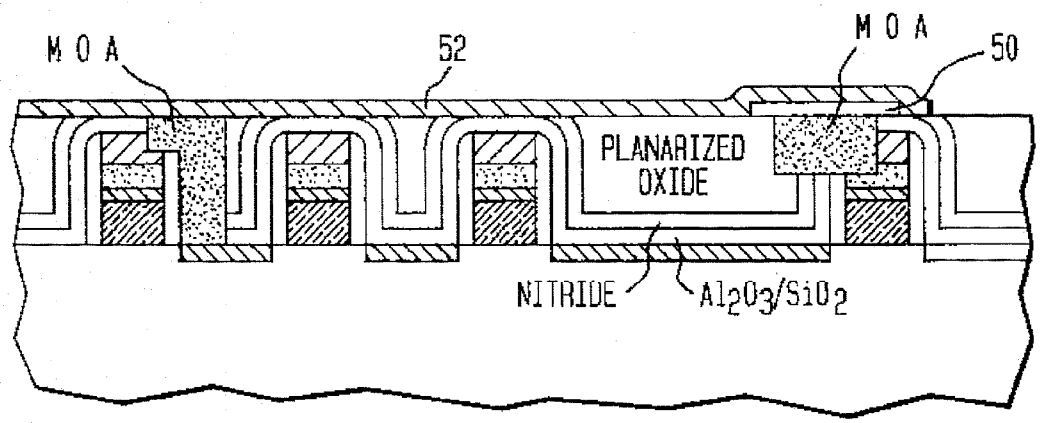

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FIG. 1

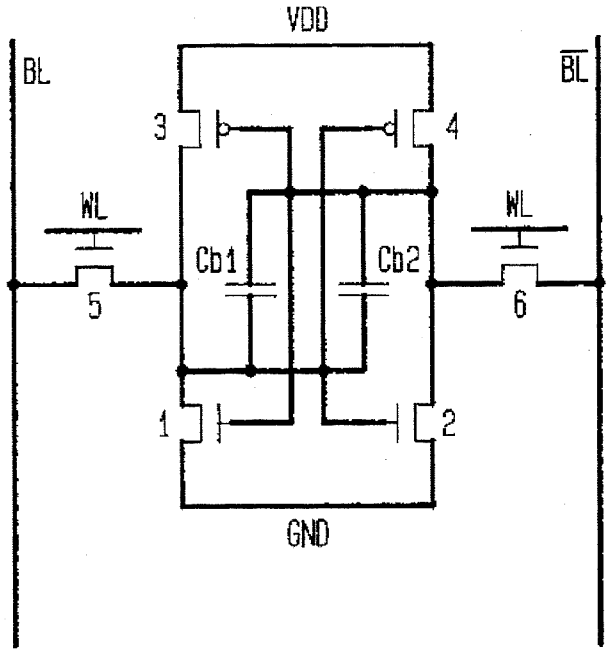


FIG. 2

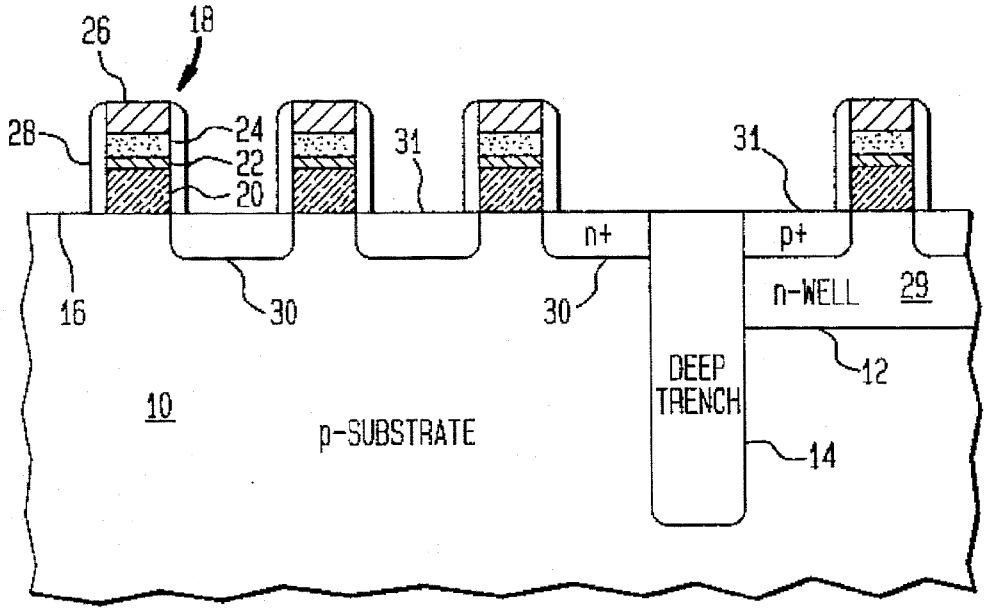


FIG. 3

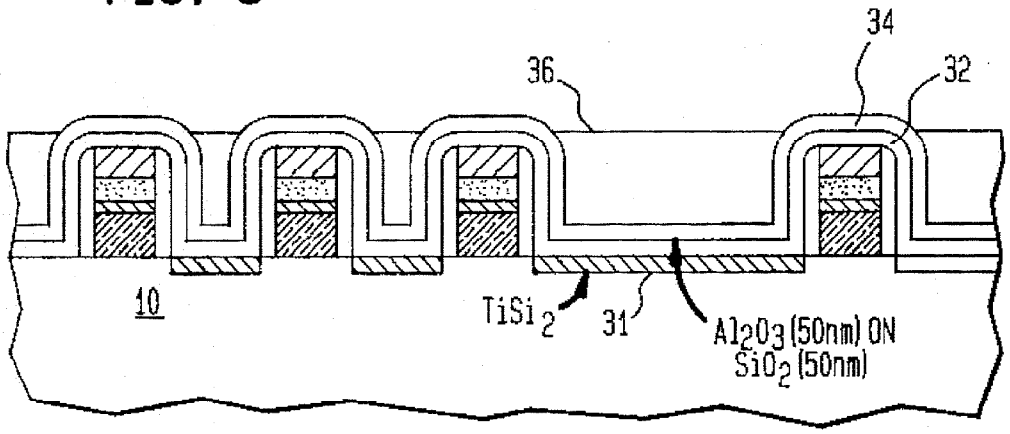


FIG. 4

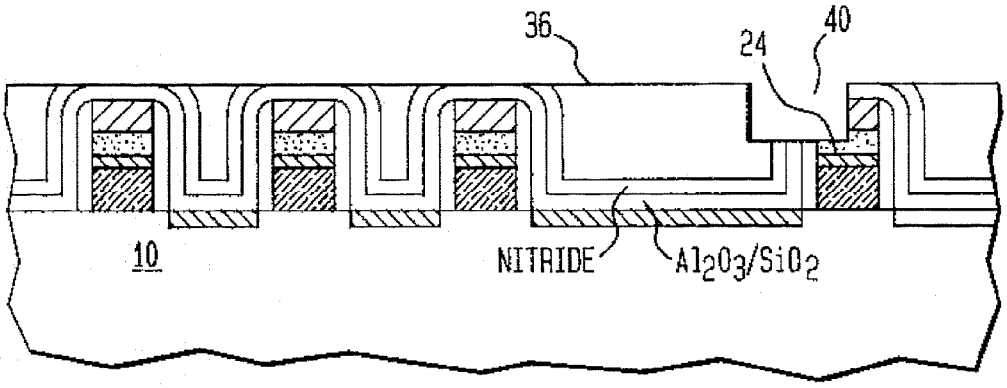


FIG. 5

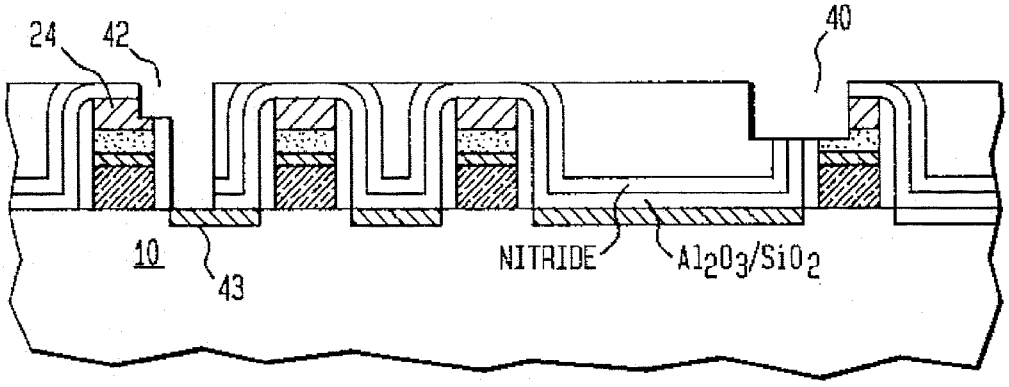


FIG. 6

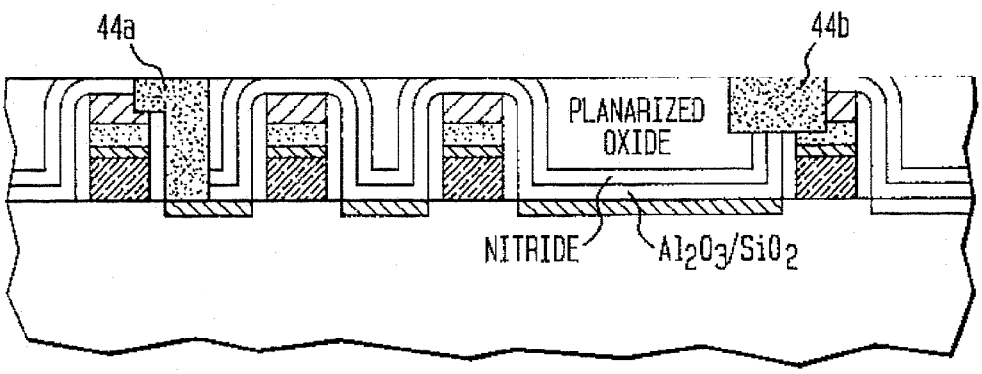


FIG. 7

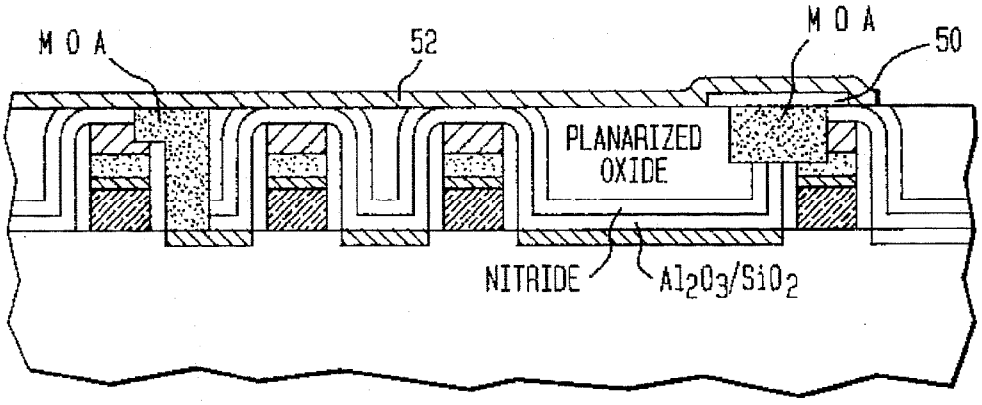
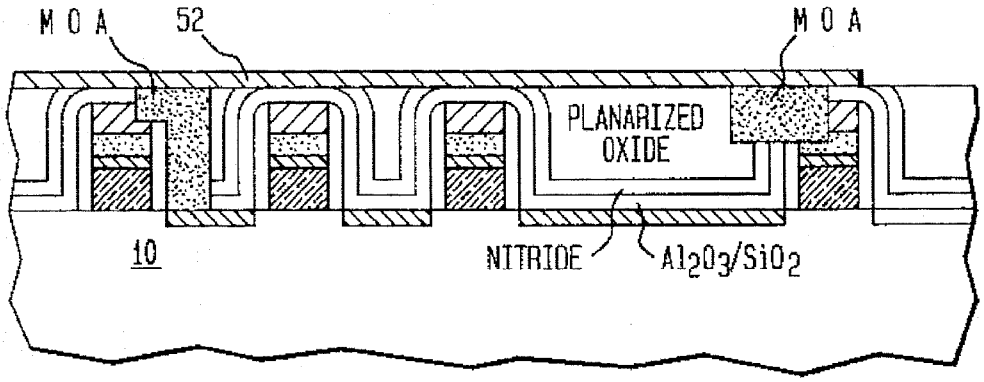


FIG. 8



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