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United States Patent [19]

Nicholls et al.

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[54] **SEMICONDUCTOR DEVICE
INCORPORATING A CONTACT FOR
ELECTRICALLY CONNECTING ADJACENT
PORTIONS WITHIN THE SEMICONDUCTOR
DEVICE**

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[73] Assignee: **Inmos Limited**, United Kingdom

[21] Appl. No.: **119,519**

[22] Filed: **Sep. 10, 1993**

[30] **Foreign Application Priority Data**

Sep. 11, 1992 [GB] United Kingdom 9219268

[51] Int. Cl.⁶ **H01L 29/76**

[52] U.S. Cl. **257/383; 257/641; 257/900**

[58] Field of Search 257/382, 383,
257/900, 393, 640, 641, 649, 903, 344,
408

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Primary Examiner—Sara W. Crane

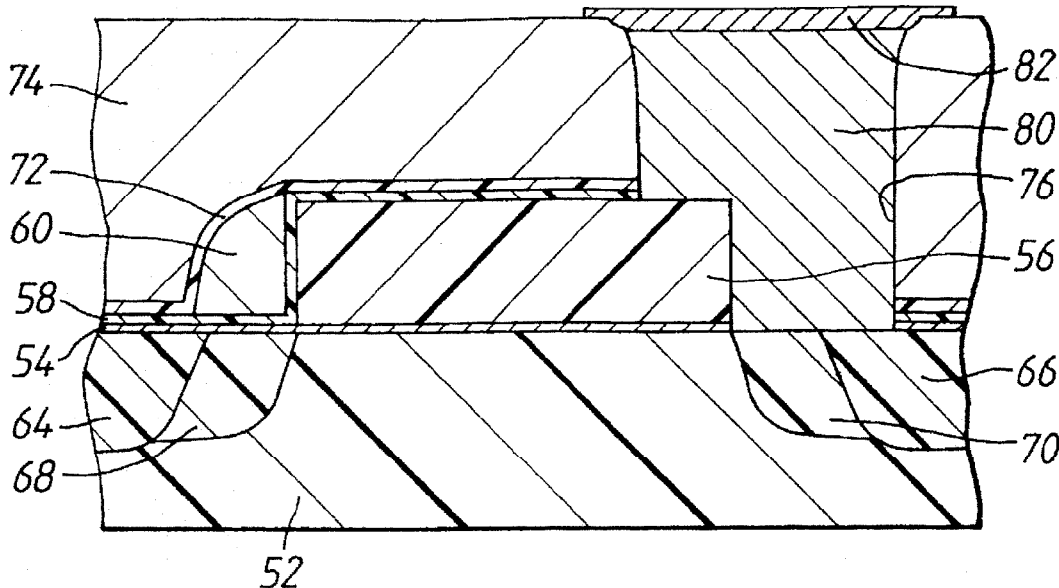
Assistant Examiner—Courtney A. Bowers

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[57] **ABSTRACT**

A semiconductor device comprising a silicon substrate, an oxide layer on the silicon substrate, a doped polysilicon region disposed on the oxide layer, a dielectric layer which has been deposited over the doped polysilicon region and the silicon substrate, a contact hole which is formed in the dielectric layer and extends over respective laterally adjacent portions of the doped polysilicon region and the silicon substrate and a contact which has been selectively deposited in the contact hole which electrically connects the said portions together. The invention also provides a method of fabricating a semiconductor device incorporating a refractory metal contact, the method comprising the steps of: a) providing a semiconductor substrate having an oxide layer thereon and a doped polysilicon region disposed on the oxide layer; (b) depositing a dielectric layer over the doped polysilicon region and over the silicon substrate; (c) forming a contact hole in the dielectric layer which exposes a portion of the doped polysilicon region and a laterally adjacent portion of the silicon substrate; and (d) selectively depositing a contact into the contact hole thereby electrically to connect together the doped polysilicon region and the silicon substrate.

10 Claims, 7 Drawing Sheets



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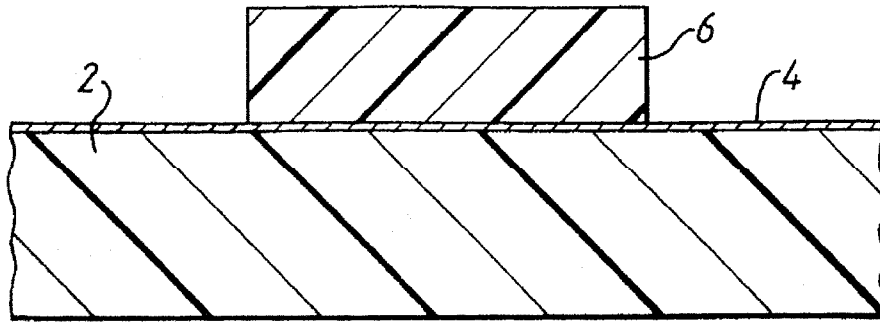


Fig. 1a

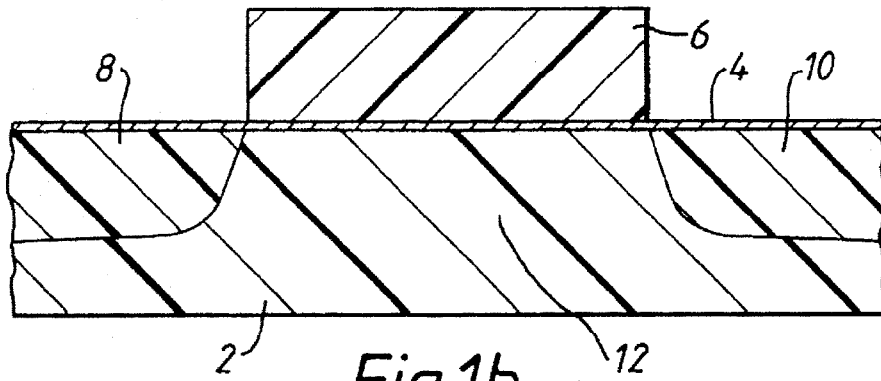


Fig. 1b

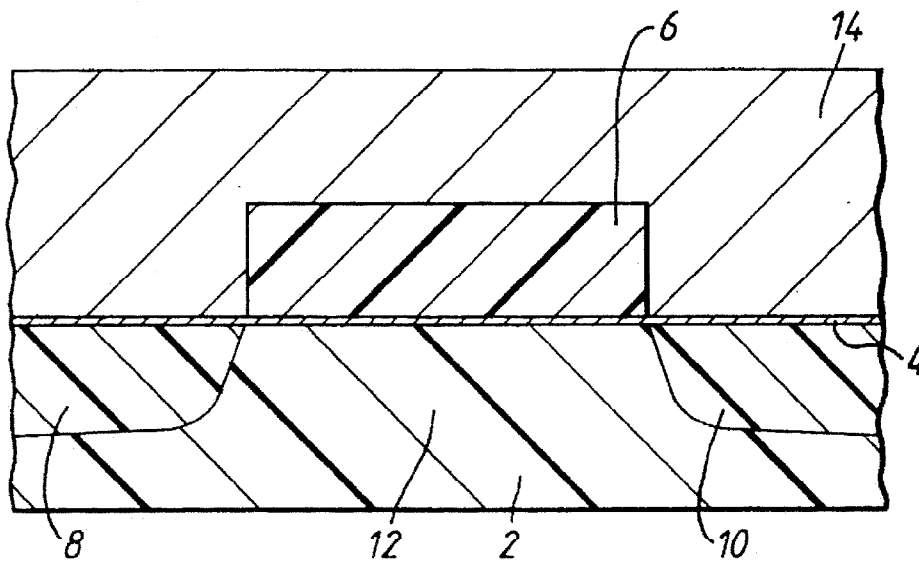


Fig. 1c

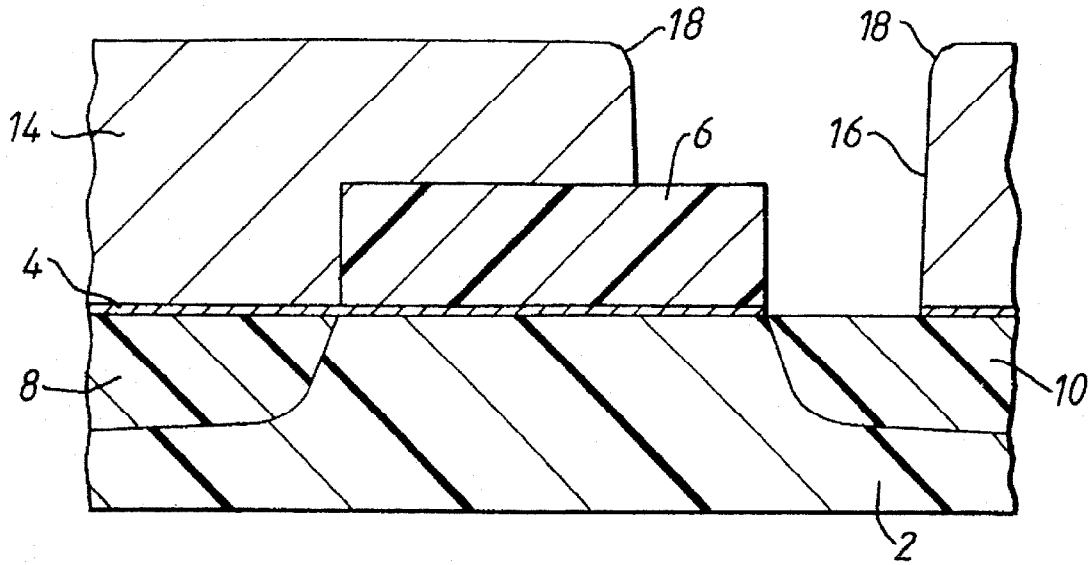


Fig. 1d

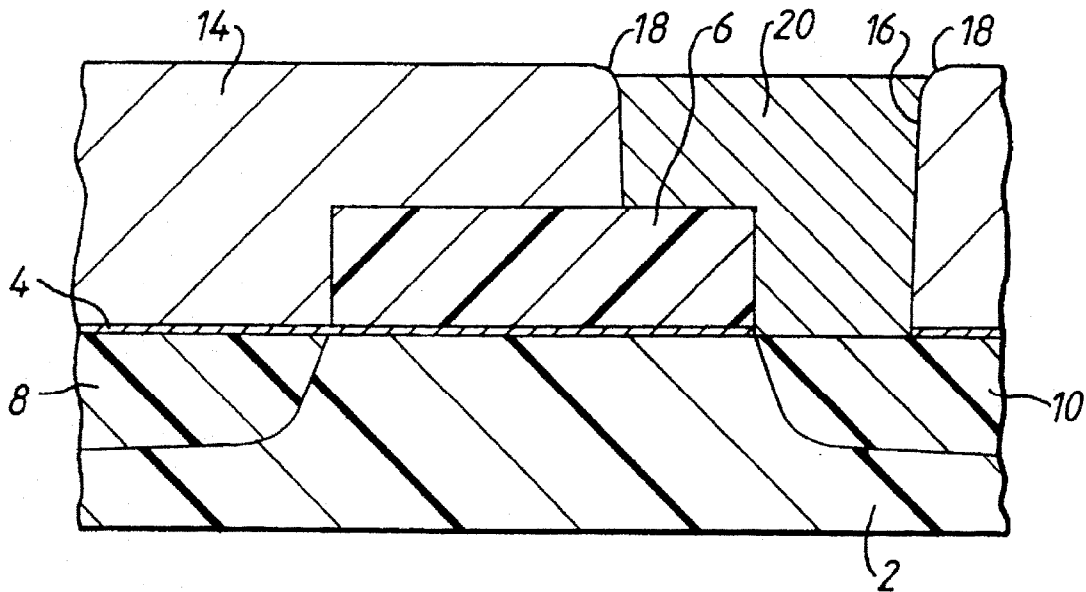


Fig. 1e

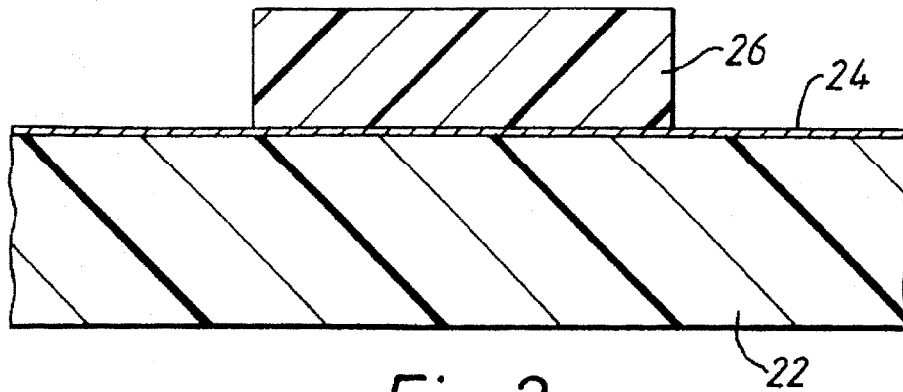


Fig. 2a

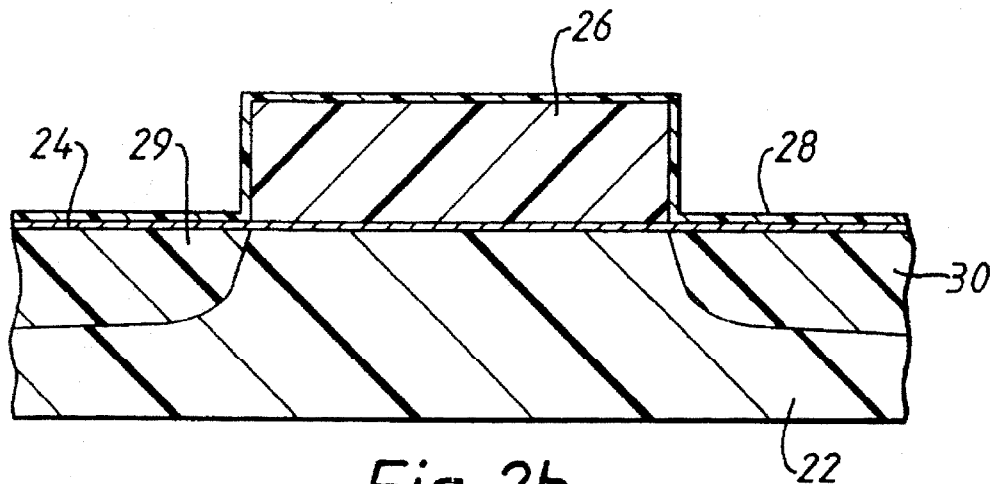


Fig. 2b

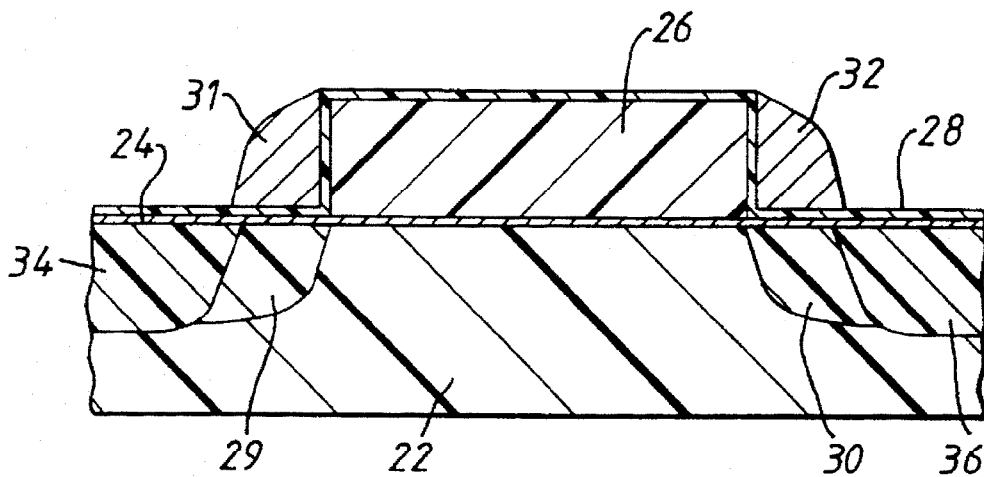
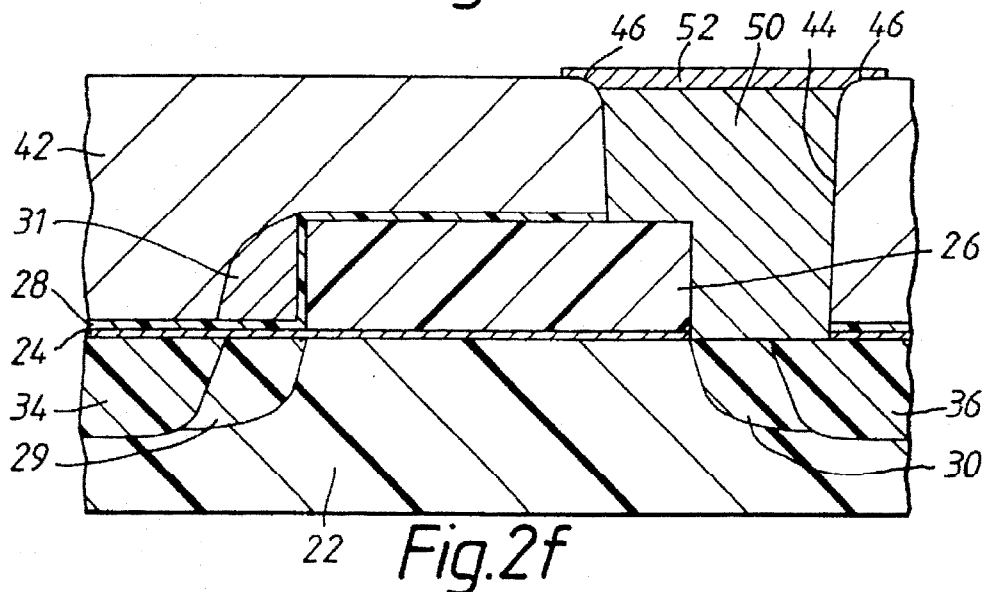
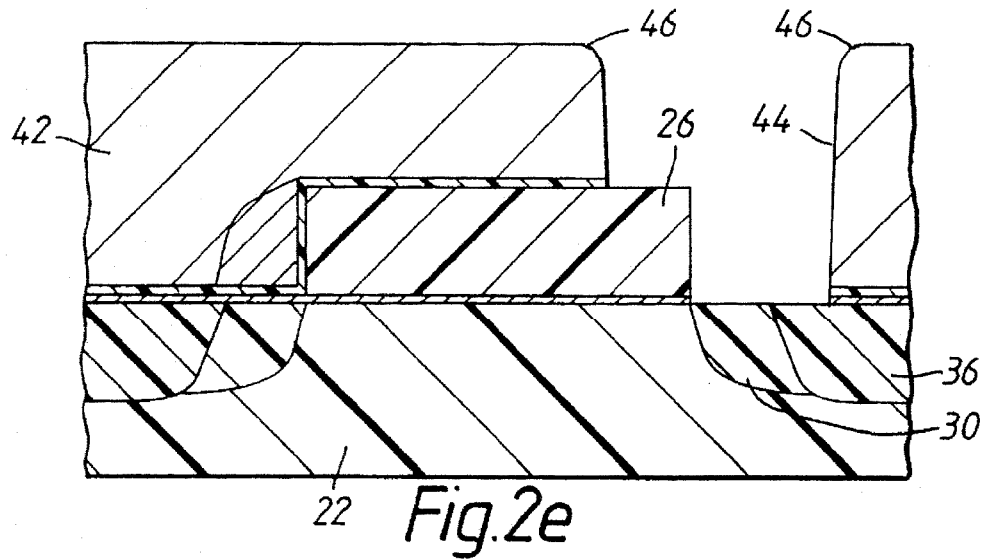
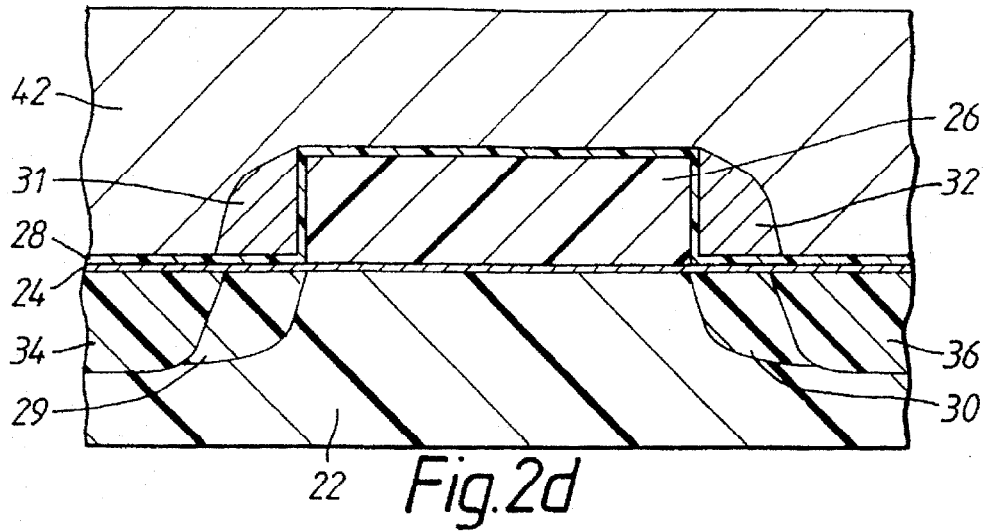


Fig. 2c



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