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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

Case IPR2016-00288

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,784,552 CHALLENGING CLAIMS 8-12 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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Intel Corporation ("Intel") respectfully requests *Inter Partes* Review of claims 8-12 of U.S. Patent No. 6,784,552 (the "'552 patent") (Ex. 1101) pursuant to 35 U.S.C. §§ 311-19 and 37 C.F.R. § 42.1 *et seq*.

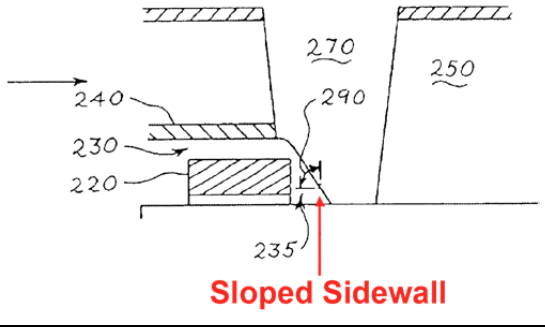
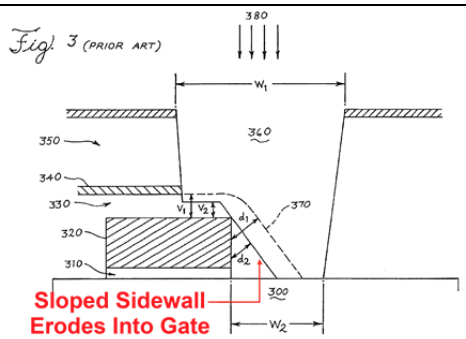
I. INTRODUCTION

The '552 patent purports to provide a novel approach to semiconductor manufacturing but instead merely duplicates a well-known technique patented by inventor Barbara Heath nearly a decade before the alleged invention.

The '552 patent is directed to the manufacture of transistors used in semiconductor products such as microprocessors and memory. Transistors are one of the basic building blocks of semiconductors—they are microscopic switches that turn on and off to allow semiconductors to process data. Transistors include various components and "contacts" that are used to connect a component of one transistor to a component of another transistor. The '552 patent is directed to a particular technique for the formation of "contact openings"—openings created through the layers of a semiconductor device so that a contact can be formed between components.

The patent asserts that prior art techniques for forming these contact openings resulted in an unacceptably high risk of creating unintentional connections (and thus a short-circuit) between the contacts and nearby components. Specifically, the patent explains that prior art techniques used non-conducting

"sidewall spacers" between contact openings and nearby components to prevent unintentional connections. But the patent notes that during the process of creating the openings, these sidewall spacers could become sloped. According to the patent, a sloped sidewall spacer is particularly susceptible to erosion in subsequent fabrication steps such that it can be worn down to the point that the contact opening and a nearby component can make an unintentional connection:

'552 patent, Fig. 2(B)	**'552 patent, Fig. 3**
	

In Fig. 2(B), described as "Prior Art," the patent shows a contact opening 270, a sidewall spacer 235 that has become sloped as a result of the creation of the contact opening, and a nearby component 220. In Fig. 3, also described as "Prior Art," the patent shows that in a subsequent step, the sloped sidewall spacer has become eroded from the dotted line (370) to the solid line, such that nearby component 320 (a "gate") is now exposed to the contact opening. According to the patent, this unintentional connection between the component and the contact opening would result in a short-circuit and thus a non-functioning transistor.

The patent purports to solve this problem by using a process that prevents

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