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Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

#16 Response Req for Recon Jmcunnille 3/11/03

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	

AMENDMENT AND REQUEST FOR RECONSIDERATION

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Responsive to the Official Action of September 11, 2002 Applicants respectfully request reconsideration in light of the following remarks.

REMARKS

Applicants would like to thank the Examiner for indicating withdrawal of the previous grounds of rejection.

The present invention relates to a semiconductor device with well defined contact openings. In the past, the practice with respect to forming contact openings during the fabrication of semiconductor devices, particularly self-aligned contact openings, was to

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use etchants with high selectivity to protect underlying regions. However, the properties of a highly selective etch of the overlying etch layer can transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer. Before the conductor materials are added to the contact opening, the opening was cleaned with a sputter etchant which can erode a portion of the sloped insulating spacer. Thus in conventional self-aligned contact structures, the diagonal thickness of the spacer, rather than the vertical thickness of the insulating layer, determined the minimum insulating layer thickness for the gate. Sloping spacers limit the number of structures that can be included on a device.

The present invention avoids this problem by retaining the substantially rectangular profile of the insulating spacers. The present invention includes at least one insulating spacer in the contact region and an etch-stop material over a first insulating layer and adjacent to the insulating spacer, the etch-stop material being a different material from the insulating spacer.

The rejection of the claims under 35 U.S.C. § 103 over Dennison, et al., in view of Figura, et al., and optionally further in view of Gonzalez, is respectfully traversed. Dennison, et al. includes spacers and caps which act as an etch-stop material with respect to the overlying BPSG layer and therefore must be made of silicon nitride in order to function. The thin overlying layer **20** is described by Dennison, et al. as a barrier layer which prevents diffusion from the BPSG layer. Figura, et al. describes oxide spacers, a silicon nitride etch-stop layer, and does not describe any barrier layers.

Dennison, et al. describes a method of forming a bit line over a capacitor array of memory cells. The semiconductor wafer of Dennison, et al. has an array of electrically isolated word lines **12, 14,** and **16** having insulating spacers and caps **18**; the spacers and caps preferably comprise an insulative nitride, such as Si_3N_4 (Figure 1; column 3, lines 25-36). A thin layer **20** of Si_3N_4 is provided atop the wafer to function as a diffusion barrier (column 3, lines 34-36). Dennison, et al. is clear about the function of all of these structures:

> The principal purpose of barrier layer **20** is to prevent diffusion of boron or phosphorous atoms from BPSG layer **28** into active areas **24** and **26**. Caps [and spacers] **18** are preferably comprised of nitride (Si_3N_4) where

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layer **28** is comprised of oxide, such that the contact etch to produce first contacts **32** will stop relative to word lines spacers and caps **18**.

Accordingly, Dennison, et al., indicates that the caps and spacers act as an etch-stop material with respect to the overlying BPSG layer, and therefore need to be formed of a material such as silicon nitride. Dennison, et al. also indicates that barrier layer **20** functions to prevent diffusion from the overlying BPSG layer **28**.

Figura et al. describes a method of forming contact areas between vertical conductors. A structure is described which includes transistor gate electrodes **22** which include gate insulating protective layer **28**, and an insulating spacers **30** formed on either side of the gate electrodes (column 4, lines 6-10; Figure 1). The gate insulating protective layer **28** and insulating spacers **30** are preferably made of silicon dioxide; the lower insulating layer **36** on top of these structures is made of BPSG (column 4, lines 10-14; Figure 2). It is also noted that silicon nitride may be used instead of silicon dioxide for insulating protective layer **28** and spacers **30** (column 4, lines 22-24). Shown in Figure 3a, an etch-stop layer **43**, made of silicon nitride or other suitable material, is deposited *over* lower insulating layer **36** (column 4, lines 50-53).

Gonzalez has only been cited for a description of silicon dioxide spacers.

The spacers and caps of Dennison, et al. are required to act as an etch-stop material (see Dennison, et al., column 4, lines 6-10); the only etch-stop material described in any of the references is silicon nitride. Layer **20** in Dennison, et al. is described as a barrier layer for preventing diffusion; of all the references only Dennison, et al. describes a barrier layer, and the only material described is silicon nitride. If one were to substitute silicon oxide for the caps and spacers in Dennison, et al., then they would not act as an etch-stop material with respect to the overlying BPSG layer, and therefore such a substitution would destroy their function. Accordingly, although Figura, et al. does describe a specific embodiment where an etch-stop layer is silicon nitride and caps and spacers are formed from silicon oxide, changing the composition of the caps and spacers in Dennison, et al. would defeat their function. Furthermore, there is no suggestion to replace the barrier layer **20** of Dennison, et al. with a different material--nothing else is suggested in any of the references which would provide a barrier function other than silicon nitride. Gonzalez does not provide any additional

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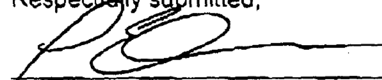
teaching to cure this deficiency. Accordingly, Applicants submit that combining the references defeats the purpose of Dennison, et al., and therefore the claimed invention is not obvious over the applied references. Withdrawal of this ground of rejection is respectfully requested.

Applicants respectfully request that the Examiner contact the undersigned upon the indication of any allowable subject matter. Applicants submit the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



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