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United States Patent [19]

Dennison et al.

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[54] **METHOD OF FORMING A BIT LINE OVER CAPACITOR ARRAY OF MEMORY CELLS**

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[73] Assignee: **Micron Semiconductor, Inc.**, Boise, Id.

[21] Appl. No.: **47,668**

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[51] **Int. Cl.**[5] **H01L 21/72**

[52] **U.S. Cl.** **437/60**; 437/233; 437/919

[58] **Field of Search** 437/47, 52, 60, 233, 437/919; 148/DIG. 14; 257/306

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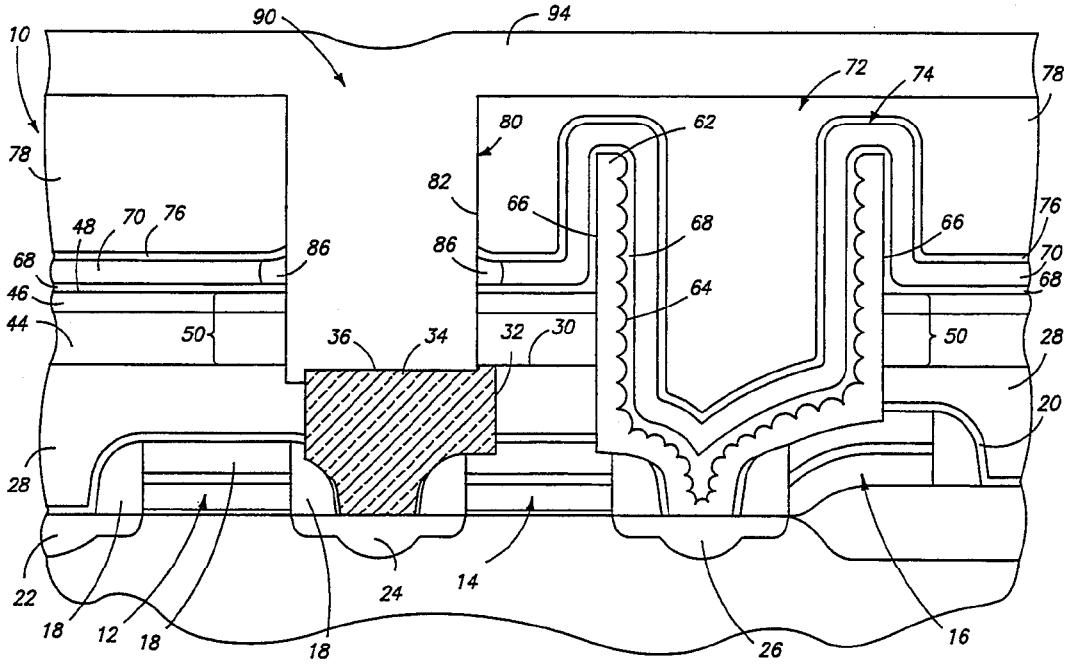
Assistant Examiner—Chandra Chaudhari
Attorney, Agent, or Firm—Wells, St. John, Roberts, Gregory & Matkin

[57] **ABSTRACT**

A method of forming a bit line over capacitor array of memory cells includes providing first conductive material pillars within first contact openings downwardly to active (source/drain) areas for ultimate connection with bit lines. A covering layer of insulating material is provided over the first pillars, and contact openings provided therethrough to electrically connect with other active (source/drain) areas for formation of capacitors. Capacitors are then provided within the capacitor contact openings. An overlying layer of insulating material is then provided over the covering layer of insulating material and over the capacitors. Bit line contact openings are then provided through the overlying layer and the covering layer to the first pillar upper surfaces. Then, a digit line layer of conductive material is provided atop the wafer and within the bit line contact openings, the digit line layer electrically connecting with the first pillar upper surfaces.

33 Claims, 20 Drawing Sheets



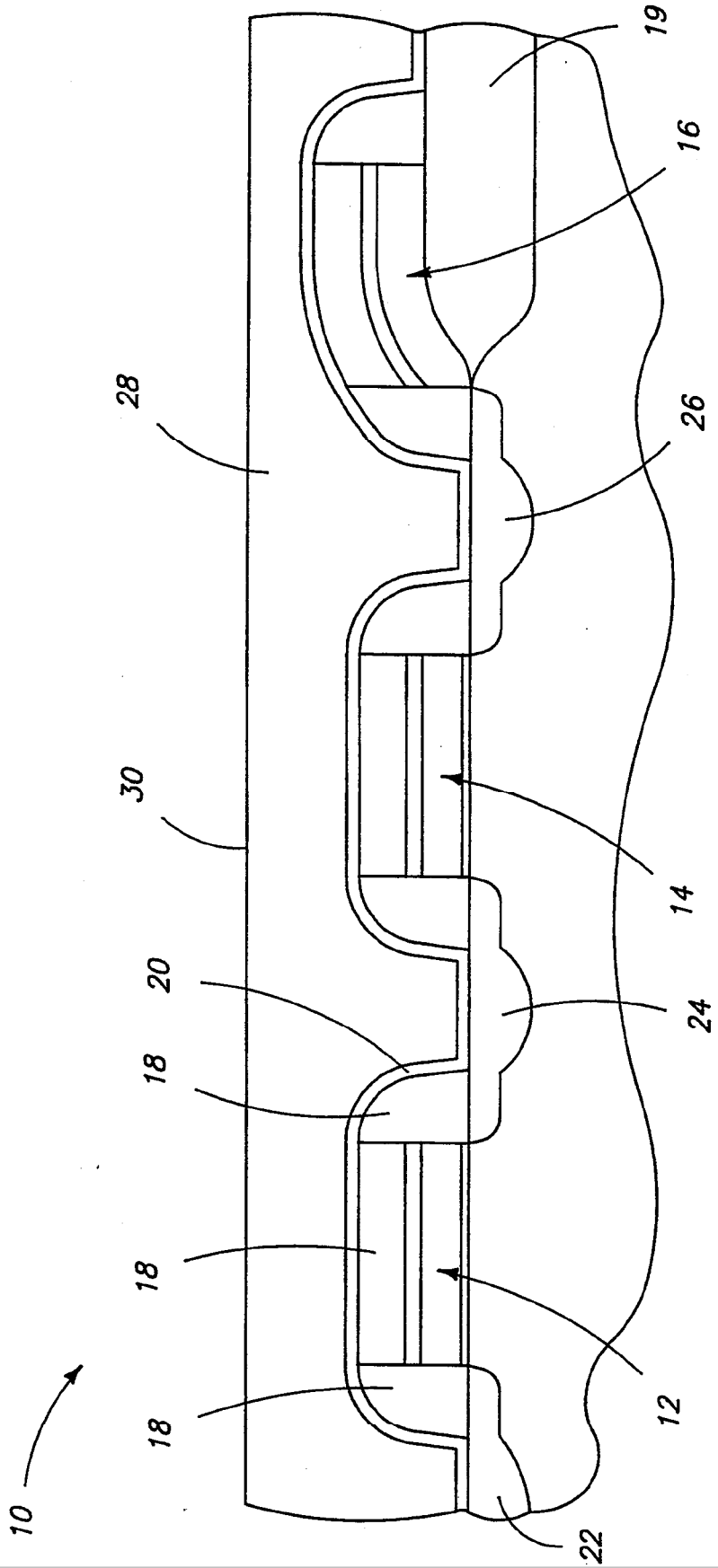


FIG. 1

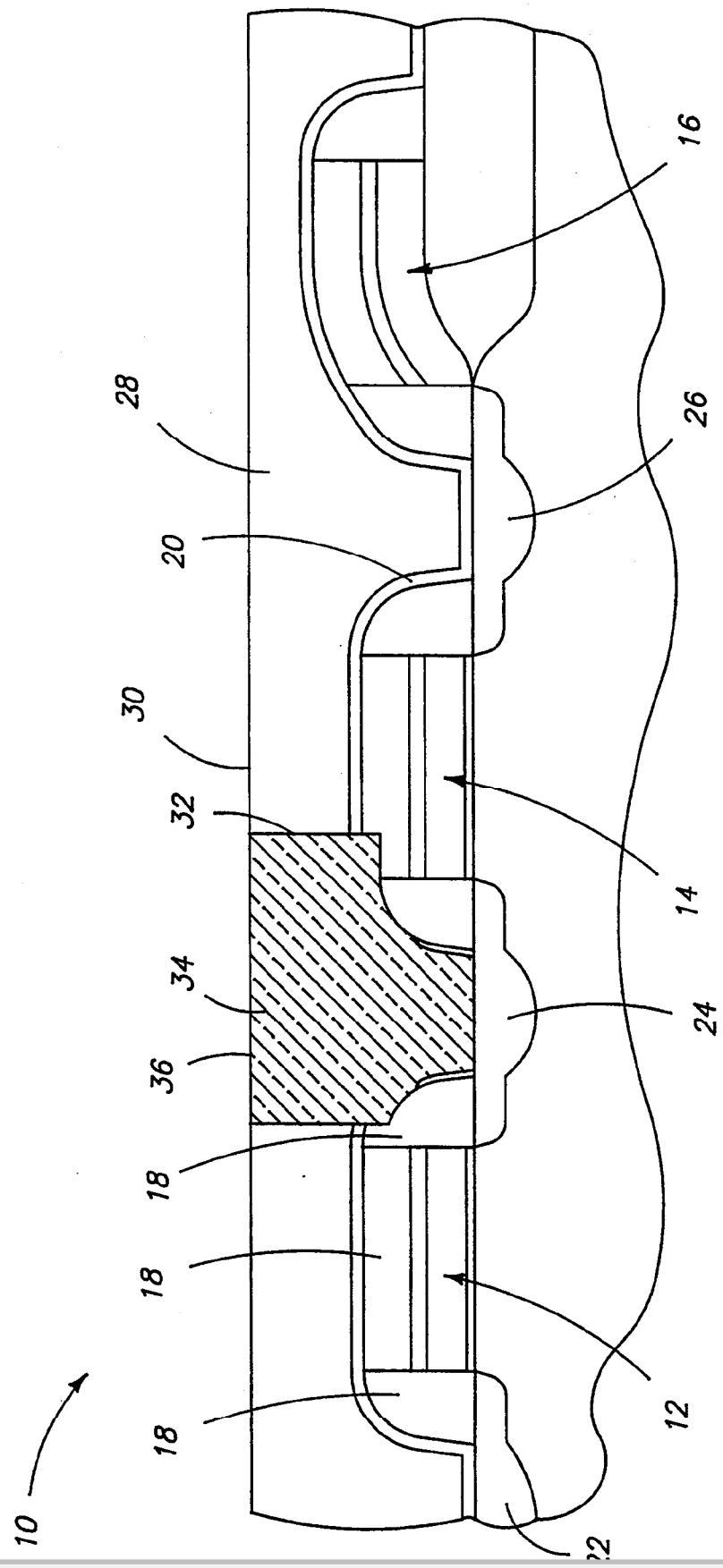


FIG 2

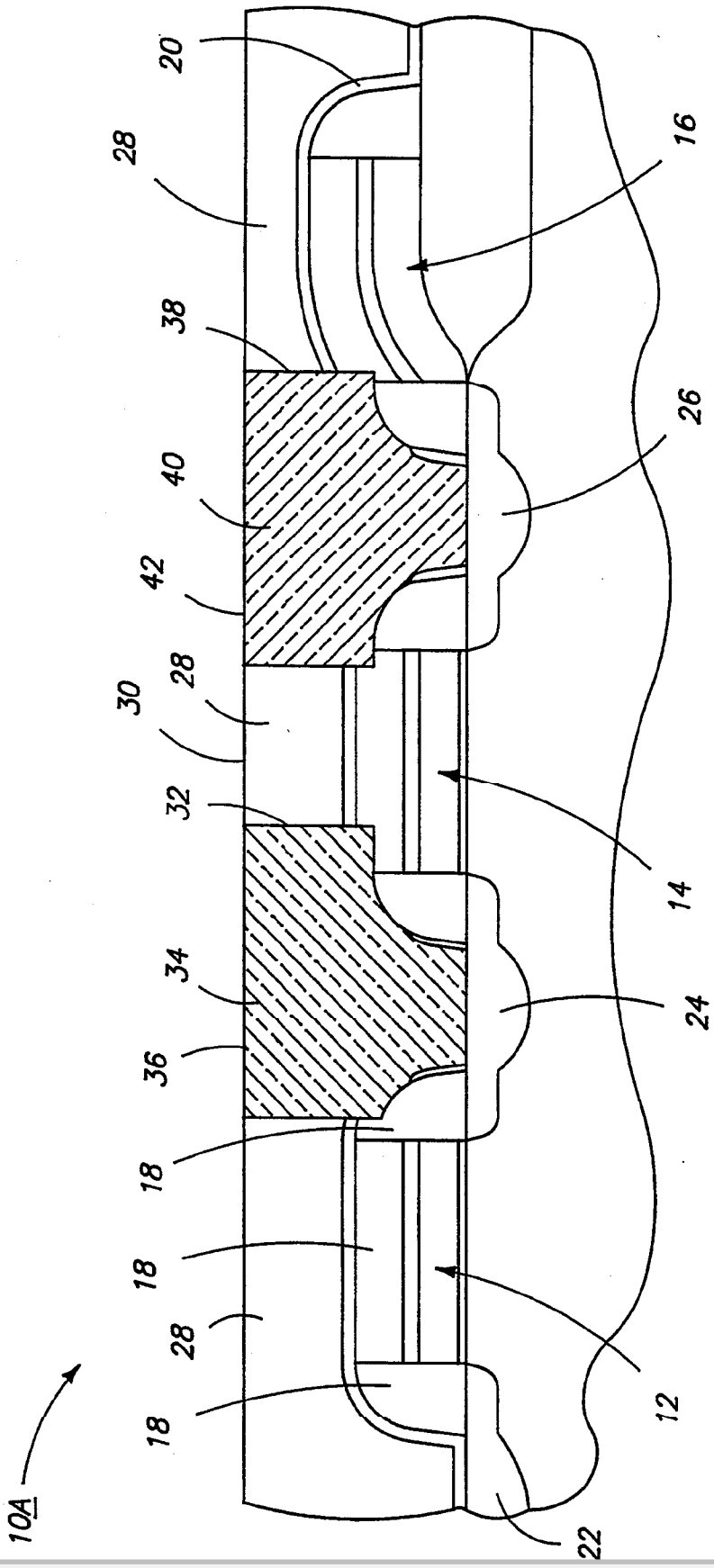


FIG 2 (A)

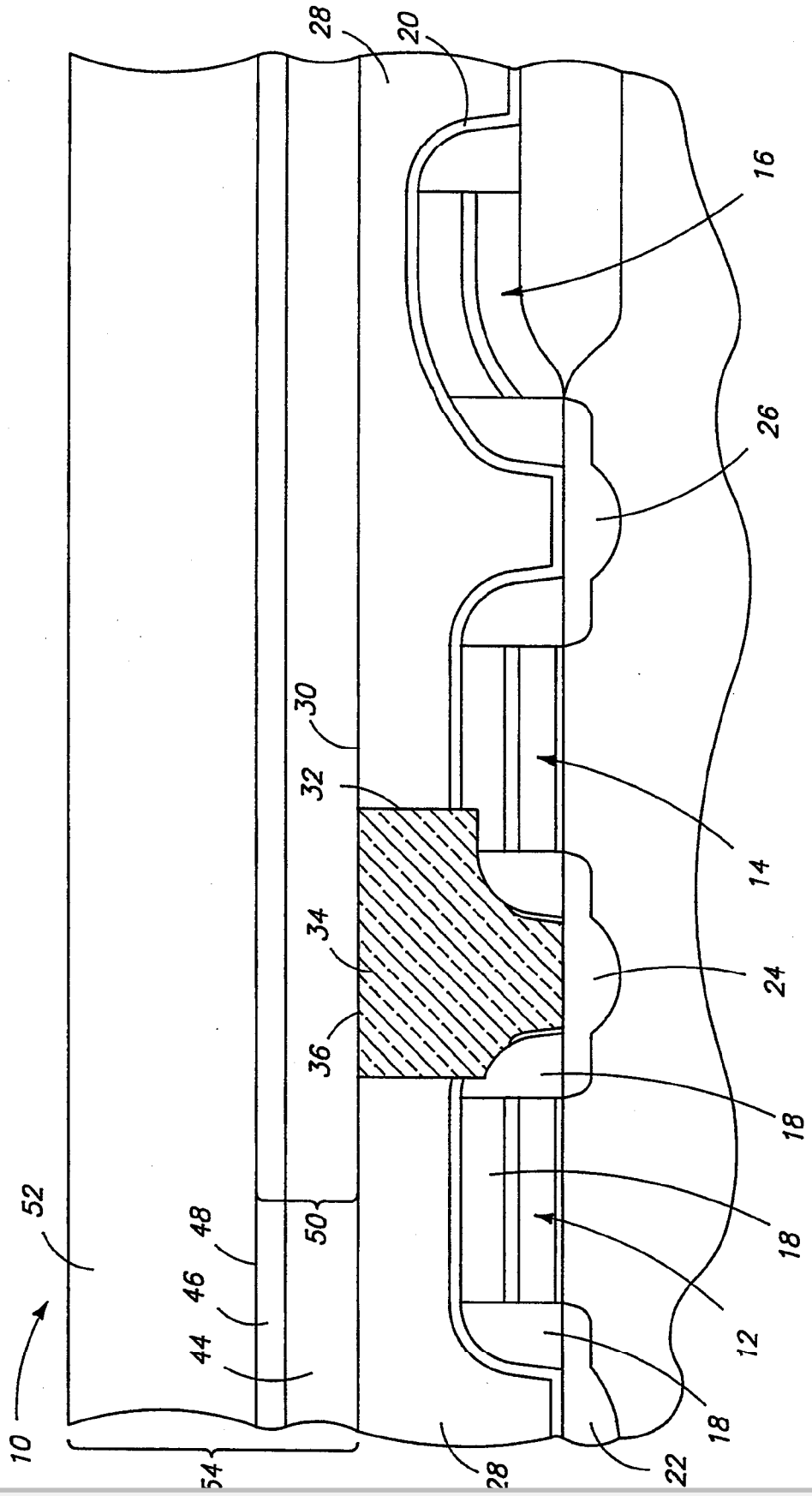


FIG. 3

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