

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner

v.

DSS Technology Management, Inc.
Patent Owner

U.S. Patent No. 6,784,552
Claims 8-12

Case IPR2016-00288

**DECLARATION OF JOHN C. BRAVMAN, PH.D.
ON BEHALF OF PETITIONER**

INTEL 1102

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 2. Claim 9: “The structure of claim 8, wherein the electrically insulative spacer has a surface portion without overlying etch stop material”48
 3. Claim 10: “The structure of claim 9, wherein the electrically insulative spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate”49

4. Claim 11: “The structure of claim 8, further comprising a second insulating layer on the etch stop layer and over the conductive layer”	50
5. Claim 12: “The structure of claim 11, further comprising a second conductive material in the contact region”	51
B. Ground 2: Claims 8-12 Would Have Been Obvious Over Heath in View of Dennison.....	52
1. Heath, in combination with Dennison, renders the claims obvious under an overly narrow construction of the “angle” limitation— <i>e.g.</i> , limiting it to a particular portion of the “side” of the insulative spacer—recited in claim 8 (element 8(g))	52
2. Even if Heath is found to not disclose an etch stop material over the insulating spacer, Heath, in combination with Dennison, renders the claims obvious.	64
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I, John C. Bravman, declare as follows:

1. My name is John C. Bravman.
2. My academic training was at Stanford University, where I received my Bachelor of Science degree in Materials Science and Engineering in 1979, and a Master of Science degree in 1981, also in Materials Science and Engineering. I completed my Doctor of Philosophy degree in 1984, with a dissertation that focused on the nature of silicon – silicon dioxide interfaces as found in integrated circuit devices.
3. From 1979 to 1984, while a graduate student at Stanford, I was employed part-time by Fairchild Semiconductor in their Palo Alto Advanced Research Laboratory. I worked in the Materials Characterization group. In 1985, upon completion of my doctorate, I joined the faculty at Stanford as Assistant Professor of Materials Science and Engineering. I was promoted to Associate Professor with tenure in 1991, and achieved the rank of Professor in 1995. In 1997 I was named to the Bing Professorship.
4. At Stanford I was Chairman of the Department of Materials Science and Engineering from 1996 to 1999, and Director of the Center for Materials Research from 1998 to 1999. I served as Senior Associate Dean of the School of Engineering from 1992 to 2001 and the Vice Provost for Undergraduate Education from 1999 to 2010. On July 1, 2010, I retired from Stanford University and

assumed the Presidency of Bucknell University, where I also became a Professor of Electrical Engineering.

5. I have worked for more than 25 years in the areas of thin film materials processing and analysis. Much of my work has involved materials for use in microelectronic interconnects and packaging, and in superconducting structures and systems. With regard to integrated circuits, I led investigations involving aluminum, copper and tungsten metallizations, polycrystalline silicon, metal silicides, a variety of oxide and nitride dielectrics, and barrier layers such as titanium and tantalum-based nitrides. Further, my groups blended fundamental aspects of the behavior of microelectromechanical systems—specifically, compliant multilayer cantilever beams—for possible test probe and package implementations. In this work my group investigated the mechanical behavior of package underfill systems, focusing on the relationship between microstructures, processing, and adhesion. I have also led multiple development efforts of specialized equipment and methods for determining the microstructural and mechanical properties of materials and structures. My groups designed and built the first high voltage SEM for in-situ studies of electromigration, the first high temperature wafer curvature system, and the first microtensile tester for micron-scale structures, amongst many others. As a graduate student I developed one of

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