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Our Case No. 10200/12
Client Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Nulty et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For STRUCTURE HAVING REDUCED LATERAL SPACER EROSION	

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Responsive to the Office Action mailed June 1, 2001, Applicants respectfully request reconsideration in light of the following amendments and remarks.

IN THE SPECIFICATION

Please insert the following statement in the application on page 1, before line 1:

+This application is a divisional of application Ser. No. 08/577,751, now U.S. Pat. No. 6,066,555, filed December 22, 1995.+ Issued on May 23, 2022

Please replace the following paragraphs:

pg. 1, ln. 19-pg. 2, ln. 9

At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and a first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

pg. 4, ln. 23-pg. 5, ln. 3

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semi-conductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discrete devices on a semiconductor substrate becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

pg. 6, ln. 4-8

Figure 1 illustrates a self-aligned contact 130 between two gate structures. Figure 1(A) is a planar top view of the contact 130. Figure 1(B) is a planar cross-sectional view of the self-aligned contact 130 between a pair of gates taken through line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of the self-aligned contact 130 between a pair of gates taken through line 1(C) of Figure 1(A).

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pg. 6, ln. 9-17

The self-aligned contact 130 is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to a well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide (designated by FOX in Fig. (1C). In this illustration, the self-aligned contact 130 is not directly over the diffusion region 140 but extends over (i.e., overlaps) a well portion 170. The self-aligned contact 130 does not short to the well portion 170 because the self-aligned contact 130 is separated from the well 170 by the field oxide.

pg. 6, ln.18-23

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon layer 110.

pg. 6, ln. 24-pg. 7, ln. 8

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate without risk of exposing the device structures and layers because the device structuring and layers

are protected from excessive etching by the etch stop layer 125. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

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pg. 7, ln. 11-22

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures is to utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 illustrates a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer 220 is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240, overlies the TEOS layer 230 and the contact region 270. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

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pg. 7, ln. 23-pg. 8, ln. 5

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact opening 270 was formed through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence, the description of the

B5 silicon nitride layer 240 is described as an etch stop layer. The silicon nitride etch stop layer 240 protected the underlying TEOS layer 230 and spacer portion 235 so that the polysilicon layer 220 completely encapsulated.

pg. 8, ln. 6-13

Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch 260 illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch B6 the silicon nitride layer 240 and to protect the underlying TEOS layer 230 from the etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

pg. 8, ln. 14-ln. 23

Figure 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride layer 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion 235 is sloping or tapered toward the contact opening 270. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective etch of the overlying etch stop layer 240 will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

pg. 8, ln. 24-pg. 9, ln. 10

In addition to providing stopping points or selectivity between materials, the use of high selectivity etches to form sloped spacer portions is the preferred practice because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not

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