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BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a
5 semiconductor device with well defined contact openings.

Background of the Invention

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In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric.
10 Examples of dielectrics include silicon dioxide, SiO₂, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si_xN_y, silicon oxynitrides, SiO_xN_y(H₂), and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")).
15 Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

Pub P2
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At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes

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typically different for different materials. The difference is used to create a selective etch, by using a gas mixture that puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For example, an etchant that has an etch rate ratio
5 or a selectivity ratio of two to one for silicon nitride compared to silicon dioxide is an effective stripper of silicon nitride from the semiconductor substrate, because it will selectively strip silicon nitride over silicon dioxide on a substrate surface. An etchant that has an etch rate ratio or a selectivity ratio of 0.85 to one for silicon
10 nitride compared to silicon dioxide is not considered an effective stripper of silicon nitride from the semiconductor substrate because the etchant will not effectively strip silicon nitride to the exclusion of silicon dioxide.

The selectivity of the etch process is a useful parameter for monitoring the process based on the etch rate characteristic of the particular etchant. As noted above, particular etchants or etchant chemistries attack different materials at
15 different etch rates. With respect to dielectrics, for example, particular etchants attack silicon dioxide, BPTEOS, TEOS, and silicon nitride dielectrics at different rates. To make openings in a substrate comprising a contact region surrounded by different dielectric layers, e.g., a dielectric layer of TEOS surrounded by a dielectric layer of silicon nitride, a process will utilize different etchants to make openings
20 through the different dielectrics. Thus, the different etch rates of particular dielectric layers for an etchant may be used to monitor the creation of an opening through a dielectric layer.

Further, by adjusting the feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied. If a low sidewall angle is desired, the
25 chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to

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prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

note B3

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discreet devices on a semiconductor substrate

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