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**BACKGROUND OF THE INVENTION**

**Field of the Invention:**

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a  
5 semiconductor device with well defined contact openings.

**Background of the Invention**

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In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric. Examples of dielectrics include silicon dioxide, SiO<sub>2</sub>, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si<sub>x</sub>N<sub>y</sub>, silicon oxynitrides, SiO<sub>x</sub>N<sub>y</sub>(H<sub>2</sub>), and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")). Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

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At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes





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prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

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The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discreet devices on a semiconductor substrate

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