

[54] METHOD OF MAKING STACKED E-CELL CAPACITOR DRAM CELL

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[52] U.S. Cl. 437/52; 437/47; 437/48; 437/60; 437/233; 437/919; 357/23.6

[58] Field of Search 437/47, 48, 51, 52, 437/60, 191, 193, 195, 228, 233, 235, 919; 357/23.6, 51

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Primary Examiner—Brian E. Hearn

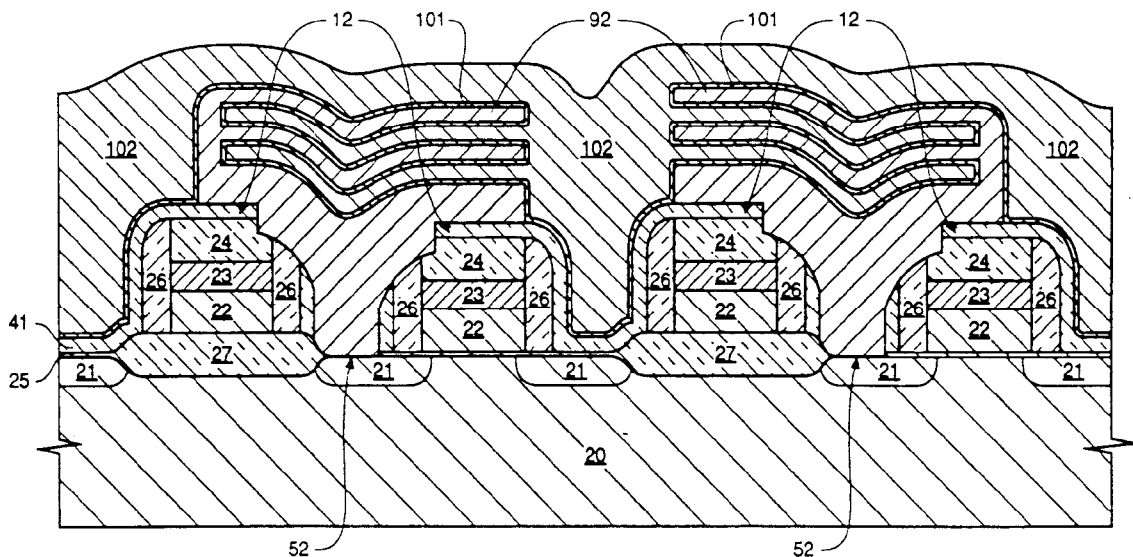
Assistant Examiner—Tom Thomas

Attorney, Agent, or Firm—David J. Paul

[57] ABSTRACT

An existing stacked capacitor fabrication process is modified to construct a three-dimensional stacked capacitor, referred to hereinafter as a stacked E cell or SEC. The SEC design defines a capacitor storage cell that in the present invention is used in a DRAM process. The SEC is made up of a polysilicon storage node structure having an E-shaped cross-sectional upper portion and a lower portion making contact to an active area via a buried contact. The polysilicon storage node structure is overlaid by polysilicon with a dielectric sandwiched in between to form a completed SEC capacitor. With the 3-dimensional shape and a textured surface of a polysilicon storage node plate, substantial capacitor plate surface area of 3 to 5X is gained at the storage node.

18 Claims, 11 Drawing Sheets



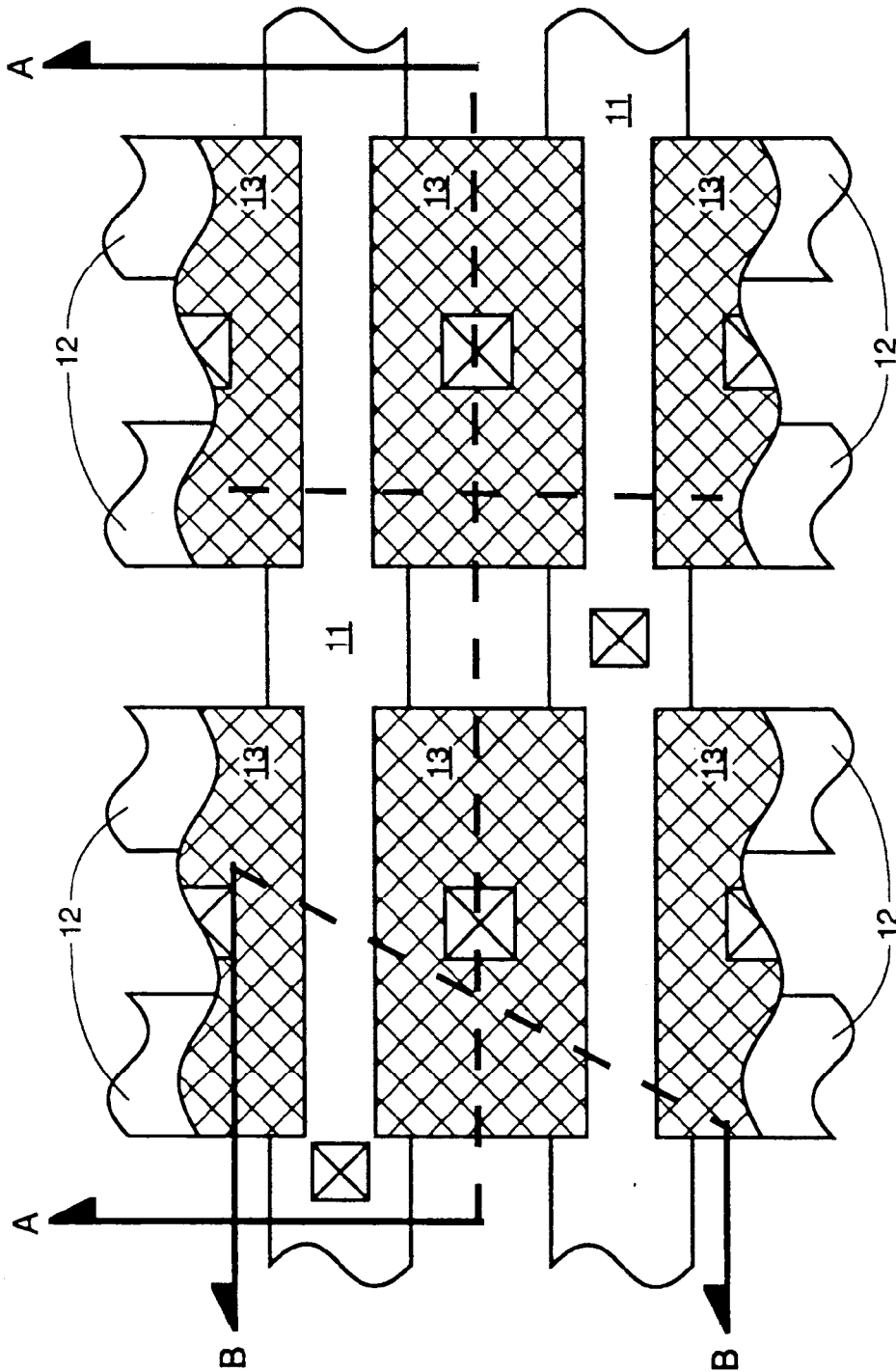


FIG. 1

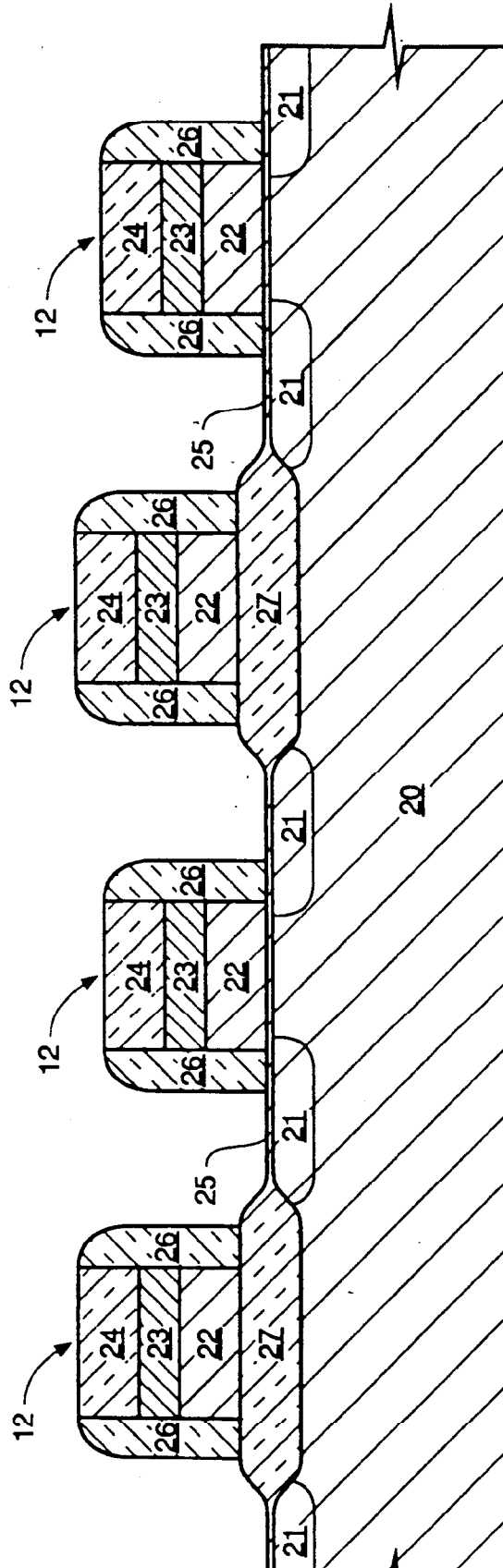


FIG. 2

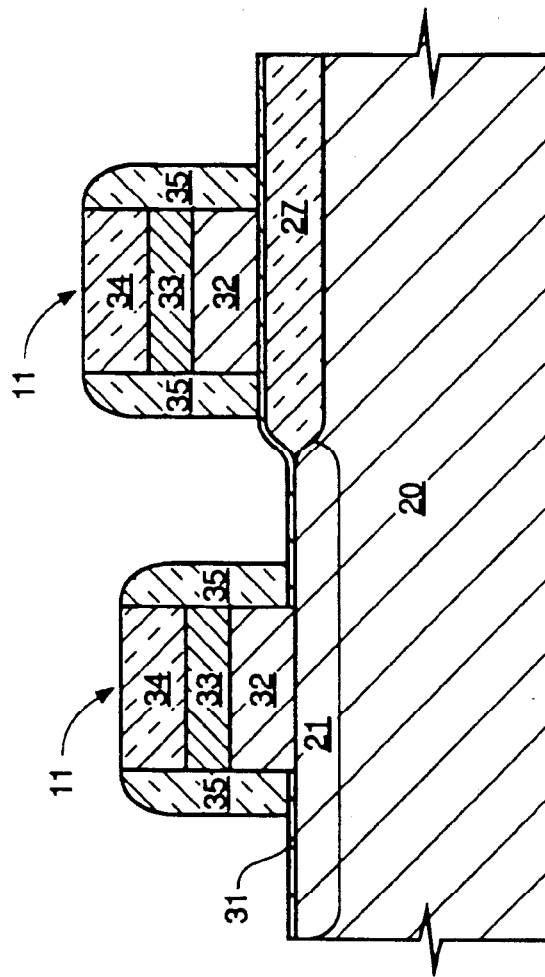


FIG. 3

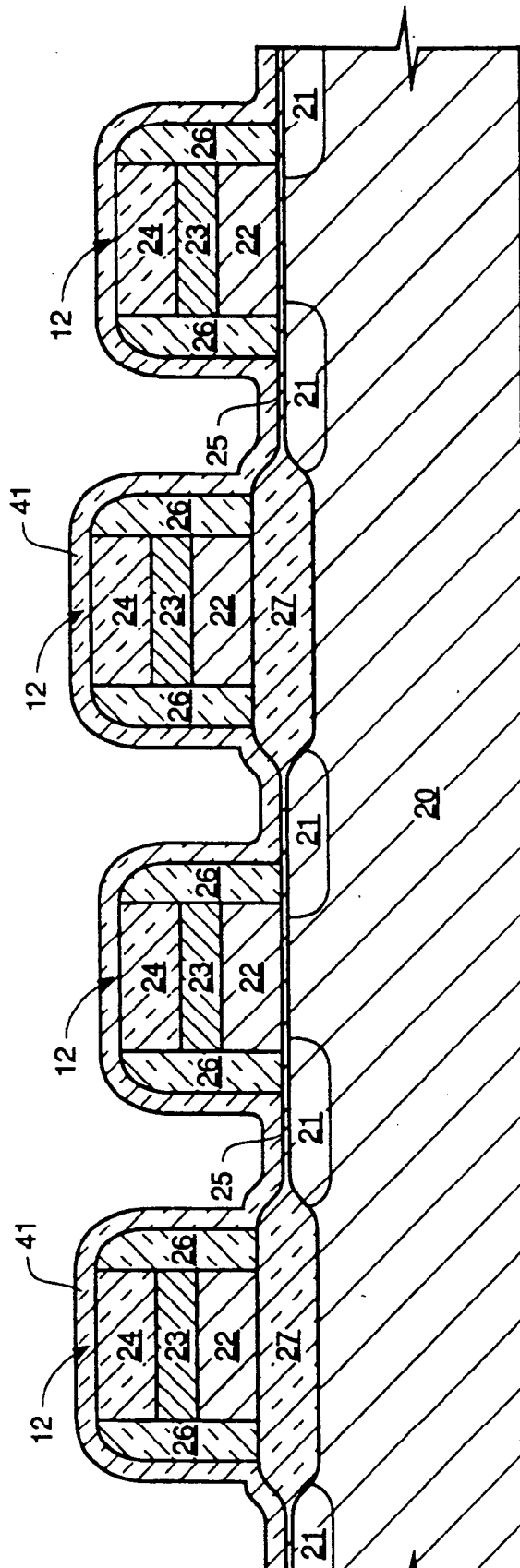


FIG. 4

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