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(54)	Title of the Invention:	Multi-Layer Semiconductor Device and Method of Manufacturing the Same
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SPECIFICATION

1. Title of the Invention

Multi-Layer Semiconductor Device and Method of Manufacturing the Same

2. Claims

(1) A multi-layer type semiconductor device comprising:

a substrate having a main surface;

a first semiconductor element layer having semiconductor elements formed on the main surface of the substrate;

an insulating film layer formed on the semiconductor element layer; and

a second semiconductor element layer having semiconductor elements formed in the vertically opposite direction to the semiconductor elements of the first semiconductor element layer, on the insulating layer.

(2) A multi-layer type semiconductor device comprising:

a transparent substrate;

a photosensor layer, formed on the transparent substrate, and having photosensor elements for receiving light passing through the transparent substrate and converting it into an electric signal;

a circuit layer, formed on the photosensor layer, and having a processing circuit, connected to the photosensor layer via through holes, for processing the electric signal received from the photosensor layer;

an insulating film layer formed on the circuit layer; and

a display element layer having display elements formed in the vertically opposite direction to the photosensor elements of the photosensor layer, formed on the insulating film layer, and through-hole-connected to the circuit layer, for displaying the results of the processing of the circuit layer.

(3) A multi-layer type semiconductor device comprising:

a transparent substrate;

a display element layer having display elements formed on the transparent substrate such that the display matter is visible through the transparent substrate;

a circuit layer, formed on the display element layer, and having a processing circuit, which is through-hole-connected to the display element layer, for processing display matter to be displayed by the display elements;

an insulating film layer formed on the circuit layer; and

a sensor layer having a face that contacts the insulating film layer and another face that is exposed to the exterior, and having sensor elements, through-hole-connected to the circuit layer, for converting an information variable from the exterior to an electrical signal.

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(4) A multi-layer type semiconductor device comprising:

a substrate having through holes wherein conductors are formed in the through holes;

a first circuit layer formed on the substrate and having an electrical circuit electrically connected to the conductors;

an insulating film layer formed on the first circuit layer;

a second circuit layer having an electrical circuit formed on the insulating film layer in the vertically opposite direction to the electrical circuit of the first circuit layer, and through-hole-connected to the electrical circuit of the first circuit layer; and

pads, formed on the insulating film layer, and electrically connected to the electrical circuit of the second circuit layer.

(5) A method of manufacturing a multi-layer type semiconductor device comprising:

a step of bonding a first substrate, having a first semiconductor layer on a surface thereof, and a second substrate, having an insulating layer on a surface thereof and a second semiconductor layer below the insulating layer, with the insulating layer and the first semiconductor layer facing each other;

a step of thinning the first substrate to expose the first semiconductor layer;

a step of forming a first semiconductor element with the first semiconductor layer as a base, with the first semiconductor layer directed upward;

a step of forming an insulating film on the first semiconductor element;

a step of bonding a third substrate on the insulating film;

a step of thinning the second substrate to expose the second semiconductor layer; and

a step of forming a second semiconductor element, with the second semiconductor layer as a base, with the second semiconductor layer directed upward.

(6) A method of manufacturing a multi-layer type semiconductor device comprising:

a step of forming through holes through a first substrate;

a step of filling the through holes in the first substrate with conductors;

a step of forming a first semiconductor layer on a main surface of a second substrate having a main surface, forming an insulating layer on the first semiconductor layer, and forming and a second semiconductor layer on the insulating layer ;

a step of forming a first electrical circuit with the second semiconductor layer on the insulating layer of the second substrate as a base, and forming first pads electrically connected to the first electrical circuit;

a step of bonding the first substrate and the second substrate so as to electrically connect the conductors of the first substrate and the first pads of the second substrate;

a step of thinning the second substrate to expose the first semiconductor layer;

a step of forming a second electrical circuit with the first semiconductor layer on the insulating layer of the second substrate as a base, and forming second pads electrically connected to the second electrical circuit.

3. Detailed Description of the Invention

[Field of Use in Industry]

This invention relates to multi-layer type semiconductor devices and to a manufacturing method for the same, and more particularly to multi-layer type semiconductor devices having semiconductor element layers stacked in mutually vertically opposite directions.

[Prior[1] Art]

An ordinary integrated circuit is formed on a surface of a wafer and has, so to speak, a two-dimensional structure. As opposed to this, an integrated circuit in which semiconductor layers, on which semiconductor elements are formed, are stacked in multiple layers is called a three-dimensional integrated circuit. Because of the multi-layer structure, the three-dimensional integrated circuit has the advantage of realizing greatly improved integration and functions.

Generally, in three-dimensional integrated circuits, semiconductor layers and insulating layers are stacked alternately, with each semiconductor layer having active elements formed therein. With the integrated circuit having elements formed in the semiconductor layers formed on the insulating layers in this manner, the elements have little excess electrical capacity, and hence there is a further advantage of the elements operating at high speeds.

The technique of forming semiconductor layers, particularly silicon layers, on insulating layers will be described next.

The technique of forming silicon layers on insulating layers, or the technique of producing a structure in which silicon layers have been formed on insulating layers is known as the SOI (Silicon On Insulator)

[1] *"Background" has been crossed out and replaced by "Prior"*

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technique. A silicon layer formed on an insulating layer is called an SOI layer, and a structure having silicon layers formed on insulating layers an SOI structure.

Methods are known which utilize epitaxial growth as SOI techniques. In these methods, liquid phase epitaxy methods, such as the melting/recrystallization method, in which a polycrystalline or amorphous semiconductor layer formed on an insulating layer is exposed to and melted by energetic light such as a laser beam, an electron beam or the like, and is thereafter allowed to solidify, the solid phase epitaxy method, in which an amorphous semiconductor layer is caused to grow in a solid phase, and vapor phase epitaxy methods such as graphoepitaxy, bridging epitaxy or the like are used. However, since these methods cause silicon crystals to grow on an insulating layer, there were problems in terms of it being more difficult to obtain a single-crystal layer over a large area, and problems in terms of it being more difficult to control film thickness, than in the case of causing silicon crystals to grow epitaxially on a single-crystal layer.

Furthermore, SIMOX (Separation by Implanted Oxygen) is known as a technique for producing the SOI structure. SIMOX is a method of injecting ions such as oxygen ions, in high concentrations, into a semiconductor layer to form a buried insulating layer so as to obtain a structure having mutually separated semiconductor layers. With this method, however, it is difficult to obtain a multi-layer structure, and therefore this method is difficult to apply to three-dimensional integrated circuits.

Further, a wafer bonding method is known as technique for producing a SOI structure. In the wafer bonding method, a single-crystal wafer or a wafer having a single-crystal layer is overlaid on a wafer having an insulating layer formed on the surface, and the two wafers are heat treated (annealed) in an atmosphere of 600°C to 1000°C, whereby an interatomic junction is produced at the joined faces, bonding the wafers together, and the upper wafer is thinned, whereby the semiconductor layer is formed on the insulating layer. The semiconductor layer produced on the insulating layer in this manner is originally formed by epitaxial growth on a single-crystal silicon substrate, and thus has crystalline properties and a uniform film thickness, and is therefore suitable for manufacture of a three-dimensional integrated circuit.

A multi-layer type semiconductor device manufactured using such a wafer bonding method, which serves as background for this invention will be described next.

FIGS. 24A through 24K are sectional views describing a process of manufacturing the multi-layer type semiconductor device serving as background for this invention.

Referring to FIG. 24A, a first silicon wafer 101a having a thickness of 500 to 600 μm is such that an insulating layer 102 is formed 1000 to 10,000 Å thick on a surface region thereof. Meanwhile, a second silicon wafer 101b having approximately the same thickness as the first silicon wafer 101a is such that, formed on a surface region thereof, there is a boron-injected layer 103a with boron injected at a high concentration, on the order of 1 x $10^{20}/cm^3$, and a low concentration epitaxial layer 104a having a thickness of about 5,000 Å. The epitaxial layer 104a is produced by causing silicon crystals to grow epitaxially on the single-crystal substrate 101b.

Referring to FIG. 24B, the two wafers 101a and 101b are overlaid with the insulating layer 102 and epitaxial layer 104a facing each other, and are heat-treated in an atmosphere of approximately 800°C. This heat treatment is called annealing. The annealing induces an interatomic junction at the joined faces, which bonds the two wafers 101a and 101b. Next, an upper surface of one of the wafers 101b is abraded until the thickness reaches 100 μm, and next the wafer 101b is etched until the thickness reaches 10 um.

Next, the wafer 101b is etched with an aqueous solution of ethylenediamine and pyrocatechol. The etching rate with this aqueous solution is 1 μm/minute for semiconductor regions having a low concentration of boron, but 20 Å/minute for the regions of high boron concentration, and thus the etching action stops at the high concentration boron-injected layer 103a. Thus, as shown in FIG. 24C, the wafer 101b is removed, leaving the high concentration boron-injected layer 103a and epitaxial layer 104a. Next, to form semiconductor elements, the boron-injected layer 103a

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is etched away, next the exposed surface is oxidized, and next the oxide film is etched away. Consequently, a thin SOI layer 104a having a thickness on the order of approximately 1000 Å is produced.

Next, referring to FIG. 24D, field oxide layers 105a are formed by LOCOS (Local Oxidation of Silicon) in regions of the SOI layer 104a which are to serve as element isolation regions.

Next, referring to FIG. 24E, a gate insulator film 107a is formed by oxidation of the SOI layer 104, and a polysilicon layer is formed on the gate insulator film 107a. This polysilicon layer is patterned into a shape of a gate electrode 106a. Next, impurities are ion implanted, with the gate electrode 106a as a mask, to form source and drain regions 108a.

Next, referring to FIG. 24F, an interlayer insulating film 109a is formed over the entire surface, and contact holes 110 are formed in the interlayer insulating film 109a.

Next, referring to FIG. 24G, a refractory metal wiring layer 111 is formed electrically connected to the source and drain regions 108a and extending on the interlayer insulating film 109a. The gate electrode 106a, the gate insulator film 107a and the source and drain regions 108a constitute a transistor. Next, an insulating layer 112 is formed over the interlayer insulating film 109a and the refractory metal wiring layer 111.

Next, referring to FIG. 24H, the insulating layer 112 is flattened for the purpose of lamination. Thereafter the flattened insulating layer 112 is overlaid by a third silicon wafer 101c having a high concentration boron-injected layer 103b and an epitaxial layer 104b, in the same manner as the second silicon wafer 101b. The two wafers are annealed in an atmosphere of approximately 800°C, whereby the wafers are bonded, with the surfaces of the insulating layer 112 and the epitaxial layer 104b as the joined faces, as shown in FIG. 24I.

Next, as described above, the wafer 101c is thinned by abrasion and etching with a mixed solution of hydrofluoric acid and nitric acid, and further etched with an aqueous solution of ethylenediamine and pyrocatechol, so as to leave the high concentration boron-injected layer 103b and epitaxial layer 104b on the wafer 101c, as shown in FIG. 24J. The epitaxial layer 104b of the third silicon wafer 101c is used as a second SOI layer. Next, to form semiconductor elements, the high concentration boron-injected layer 103b is etched away.

Next, referring to FIG. 24K, field oxide layers 105b, a gate insulator film 107b, a gate electrode 106b, source and drain regions 108b, an interlayer insulating film 109b, and a wiring layer 113 made from aluminum or an aluminum alloy are formed with the second SOI layer 104b as a base, in the same manner as described for FIGS. 24D and 24E. The gate electrode 106b, gate insulator film 107b and source and drain regions 108b constitute a transistor. In this way, a first active layer L1 is formed on the semiconductor substrate 101a with the insulating layer 102 therebetween, and a second active layer L2 is formed on the first active layer L1 with the insulating layer 112 therebetween. The transistor of the first active layer L1 and the transistor of the second active layer L2 are electrically connected by conductors provided in through holes 114, as necessary.

The multi-layer type semiconductor device manufactured by way of the steps described above employs a refractory metal wiring layer, instead of aluminum, for the metal wiring layer of the first active layer. This is because the wiring layer is subjected to high temperatures when the two wafers are bonded by annealing as shown in FIG. 24I. Thus, if a third active layer is formed on the second active layer, rather than an aluminum wiring layer, a refractory metal wiring layer is used.

In the multi-layer type semiconductor device described above, the active layers are stacked in one direction[2]. Thus, if a large number of layers are stacked, in conjunction with this stacking direction being a fixed direction, distortion becomes pronounced, giving rise to the problems of fluctuating threshold voltages and increasing leakage currents.

Furthermore, since the active layers are stacked on only one surface of the substrate, the active layers close to the substrate are heated more times than the active layers or layers farther away from the substrate and, therefore,

[2] *See Amendment (1) in the Amendment to Proceedings of*

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requires higher heat-resistance.

Next, an image processing system employing the multi-layer type semiconductor device manufactured by way of the steps discussed above will be described. This image processing system includes a light-receiving unit for receiving light from a photographic subject, and a display unit for displaying a received optical signal as an image.

In such an image processing system, generally, the light-receiving unit and display unit are formed separately. This is for the following reason. That is to say, it is necessary for light-receiving elements to receive light from outside, and it is necessary for display elements to be visible from outside. Both elements must face outward or be formed close to this. Meanwhile, with the multi-layer semiconductor device 10 that serves as background for this invention, since this is formed only on one face of the substrate, if the display elements and light-receiving elements are formed on the substrate, the display elements are formed closest to the substrate and the light-receiving elements are formed furthest from the substrate, or conversely, the light-receiving elements are formed closest to the substrate and the display elements are formed furthest from the substrate. However, since the active layers are stacked on one surface of the substrate, the elements formed closer to the substrate will be heated more times than the elements formed farther away from the substrate, and thus, a material having poor thermal resistance[3] cannot be used for the layer close to the substrate.

If, for example, a sensor made from an amorphous material were formed in the layer close to the substrate, this sensor would become inoperable since the amorphous material would become crystallized as a result of the long heat treatment. Furthermore, if a sensor comprising a pn junction were formed in the layer close to the substrate, the position of junction in the pn junction would shift or the junction would be buried in[4] semiconductor layer as a result of the long heat treatment, thereby lowering the light absorption efficiency of the sensor. Further, for example, if a liquid crystal display was formed near the substrate, the characteristics would be inferior due to the heat[5].

In order to avoid the problems described above, a method is conceivable wherein, for example, on the opposite face of the substrate on which an active layer including display elements is stacked, again for example, an active layer including sensor elements is formed. However, through holes have to be provided in the thick substrate in order to electrically connect this active layer and an active layer on the opposite side of the substrate. Since it is difficult to form many through holes in the substrate, this method cannot be applied to the above system which requires a high degree of integration. Thus, it is very difficult to apply a multi-layer type semiconductor device having SOI layers stacked only on one surface of the substrate to an image processing system having a light-receiving unit and a display unit formed on one chip. Generally, therefore, as shown in FIG. 25, a light-receiving unit 20 and a display unit 30 are fabricated separately and are electrically interconnected through leads 15.

In FIG. 25, the light-receiving unit 20 includes a substrate 201, an insulating layer 202 formed on the substrate 201 for forming an SOI layer, a three-dimensional integrated circuit 215 formed on the insulating layer 202 and including a processing circuit for processing an electric signal based on the light received by the light-receiving unit 20, a memory circuit for storing data for comparison with the electric signal and the like, a photoelectric sensor 216 wherein photodiodes are arranged in matrix, and an output circuit 217 having output pads. The three-dimensional integrated circuit 215 includes active layers L1, L2 . . . Ln in which are formed, in individual layers or in units of multiple layers, circuits having independent functions, wherein signal transfer between the layers is performed via through holes. The display unit 30 includes a substrate 301, a circuit 318 including electrodes for driving a liquid crystal display, an input circuit 317 having input pads, a liquid crystal 319, a resin member 320 for sealing the liquid crystal, and a window 321 for the display unit 30.

In the image processing system shown in FIG. 25, the photoelectric sensor 216 of the light-receiving unit 20 receives light in the direction of arrow A from a photographic subject, and converts it into an electric signal. This electric signal is electrically processed by the three-dimensional integrated circuit 215 and, for example, contour extraction, enhancement, pattern recognition and the like are performed. This electric signal is transferred from the output pads 217 of an output circuit such as a shift register, via the leads 15, to the input pads 317 of the display unit 30. In the display unit 30,

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[3] *See Amendment (2) in the Amendment to Proceedings of December 12, 1990. -- trans.*

[4] *See Amendment (3) in the Amendment to Proceedings of December 12, 1990. -- trans.*

[5] *See Amendment (4) in the Amendment to Proceedings of*

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