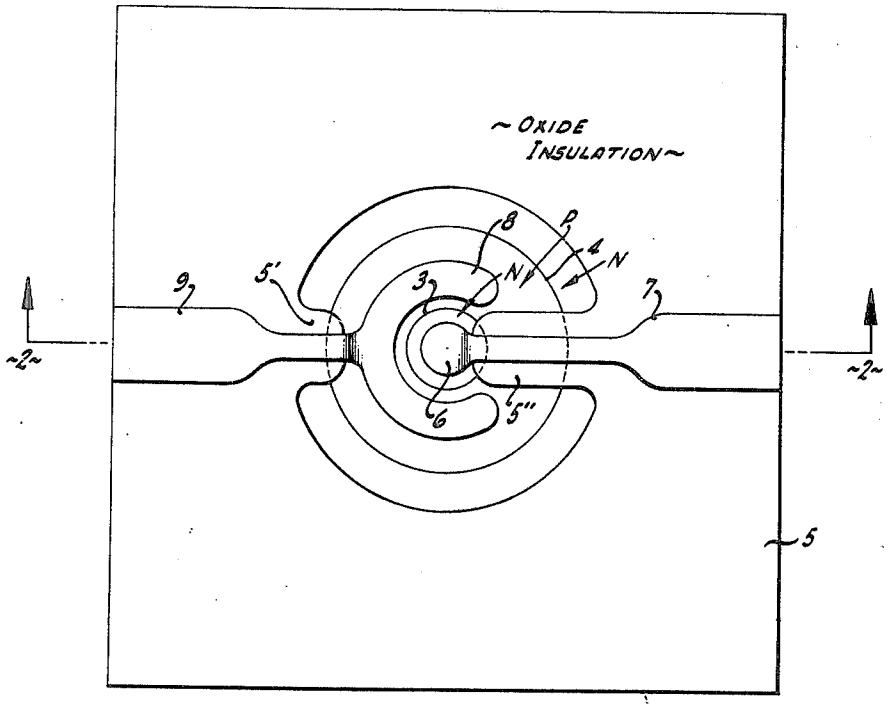
April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 1

FIG-1



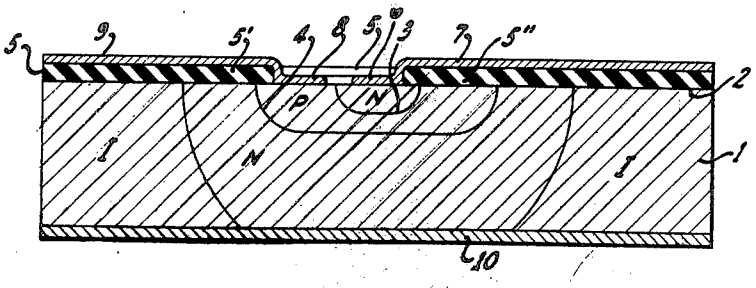


FIG-2

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SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

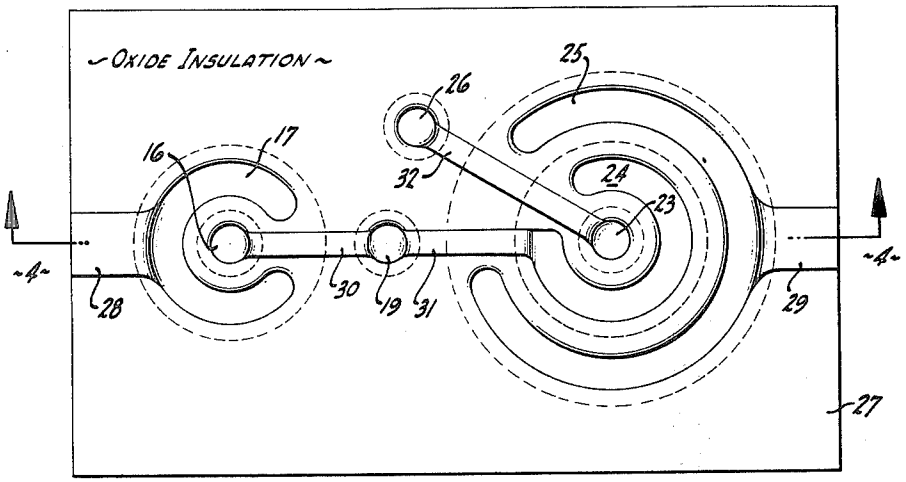

FIG-3

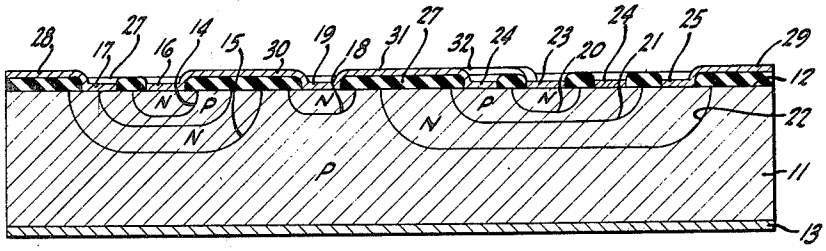

FIG-4

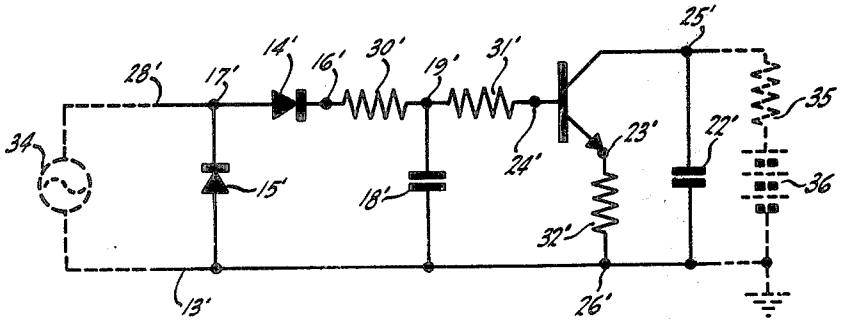

FIG-5

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April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 3

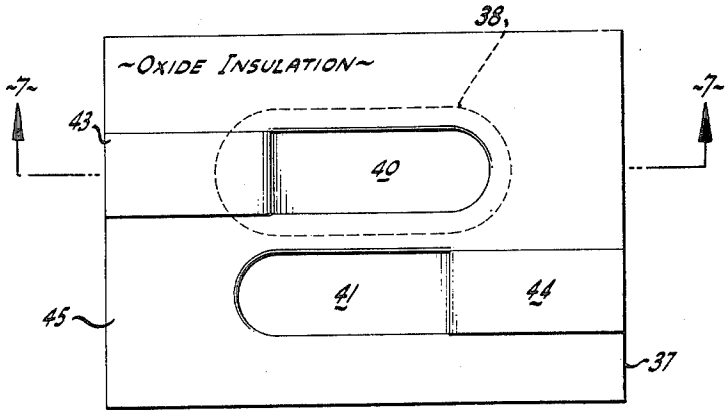

FIG-6

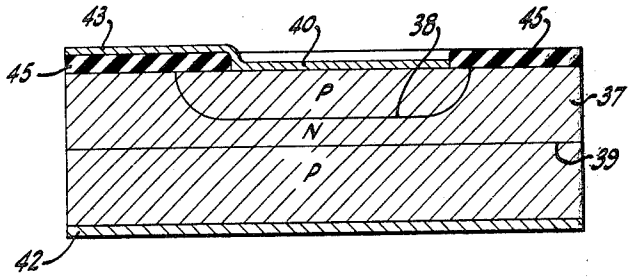

FIG-7

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United States Patent Office

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Patented Apr. 25, 1961

2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

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Filed July 30, 1959, Ser. No. 830,507

10 Claims. (Cl. 317—235)

This invention relates to electrical circuit structures incorporating semiconductor devices. Its principal objects are these: to provide improved device-and-lead structures for making electrical connections to the various semiconductor regions; to make unitary circuit structures more compact and more easily fabricated in small sizes than has heretofore been feasible; and to facilitate the inclusion of numerous semiconductor devices within a single body of material.

In brief, the present invention utilizes dished junctions extending to the surface of a body of extrinsic semiconductor, an insulating surface layer consisting essentially of oxide of the same semiconductor extending across the junctions, and leads in the form of vacuum-deposited or otherwise formed metal strips extending over and adherent to the insulating oxide layer for making electrical connections to and between various regions of the semiconductor body without shorting the junctions.

The invention may be better understood from the following illustrative description and the accompanying drawings.

Fig. 1 of the drawings is a greatly enlarged plan view of a transistor-and-lead structure embodying principles of this invention;

Fig. 2 is a section taken along the line 2—2 of Fig. 1;

Fig. 3 is a greatly enlarged plan view of a multi-device semiconductor-and-lead structure embodying principles of this invention;

Fig. 4 is a section taken along the line 4—4 of Fig. 3;

Fig. 5 is a simplified equivalent circuit of the structure shown in Figs. 3 and 4, with additional circuit elements external to said structure represented by broken lines;

Fig. 6 is a greatly enlarged plan view of another transistor-and-lead structure embodying principles of the invention;

Fig. 7 is a section taken along the line 7—7 of Fig. 6.

Figs. 1 and 2 illustrate one example of a structure according to this invention. A single-crystal body of semiconductor-grade silicon, represented at 1, has a high-quality surface 2, prepared in accordance with known transistor technology. Within the body 1 there are high-resistivity regions, designated I in the drawing, composed either of high-purity silicon having so few donor and acceptor impurities that it is a good insulator at ordinary temperatures and an intrinsic semiconductor at elevated temperatures, or of somewhat less-pure silicon containing a trace of a material such as gold that diminishes the effect of donor and acceptor impurities by greatly reducing the carrier concentrations.

Elsewhere within body 1, there are extrinsic N-type and extrinsic P-type regions, designated N and P respectively, formed in the well-known manner by diffusing N-type and P-type dopants through surface 2 into the crystal, with appropriate masking to limit the dopant to the desired areas. The smallest and uppermost N-type region constitutes an emitter layer of the transistor. This emitter layer overlies a somewhat larger P-type region which

layer, in turn, overlies a still larger N-type region which constitutes the collector layer of the transistor. Between the emitter and base layers there is a dished, P–N junction 3, having a circular edge which extends to surface 2 and there completely surrounds the emitter. Between the base and collector layers there is a dished, P–N junction 4, having a circular edge that extends to surface 2 and there completely surrounds the base. The thickness of the emitter and base layers has been exaggerated in the drawings: in actual practice each of these layers is but a few microns thick. The collector layer generally is considerably thicker, and in the example illustrated extends completely through the body 1 so that contact thereto may be made from the back side. Thus, the three extrinsic semiconductor layers described form a transistor equivalent to previously known types of double-diffused junction transistors.

During diffusion of the donor and acceptor impurities into the semiconductor, at elevated temperature in an oxidizing atmosphere, the surface of the silicon oxidizes and forms an oxide layer 5, often one micron or more in thickness, congenitally united with and covering surface 2. This layer may consist chiefly of silicon dioxide, or of disproportionated silicon suboxide, depending upon the temperature and conditions of formation. In any event, the oxide surface layer is durable and firmly adherent to the semiconductor body, and furthermore it is a good electrical insulator.

According to common prior practice in manufacturing diffused-junction transistors, the semiconductor body was deoxidized by chemical etching prior to deposition of metal contacts on the semiconductor surface. According to the present invention, only selected portions of the oxide layer are removed, as illustrated in Figs. 1 and 2, for example, while other portions of the oxide layer are left in place to serve as insulation for electrical leads used in making connections to and between the several semiconductor regions.

In particular, portions of the remaining oxide film extend across the edges of the P–N junctions at the surface of the semiconductor body, to facilitate the making of electrical connections from one side of a junction to another without shorting the junction. Thus, as illustrated in Figs. 1 and 2, the remaining oxide film comprises a tongue 5′ that crosses the edge of junction 4, and another tongue 5″ that crosses the edges of both junctions 3 and 4. On the other hand, at least a portion of the surface over each of the emitter and base layers must be cleared to permit the formation of base and emitter contacts.

A convenient and highly accurate way to remove only selected portions of the oxide film is to use photoengraving techniques. The photoengraving resist is placed over the oxide-coated surface, and this is then exposed through a master photographic plate having opaque areas corresponding to the areas from which the oxide is to be removed. In the usual photographic developing, the unexposed resist is removed; and chemical etching can then be employed to remove the oxide layer from the unexposed areas, while the exposed and developed resist serves as a mask to prevent chemical etching of the oxide areas that are to be left on the semiconductor surface.

A discoid, metal, emitter contact 6 is adherent to surface 2, wholly within the edge of junction 3, centered upon and in electrical connection with the emitter region of the transistor. Electrical connections to this emitter contact are made through a metal strip 7 extending over and adherent to oxide layer 5. The strip 7 extends over the tongue 5″ of the insulating oxide layer across the junctions 3 and 4, and thus provides

composite structure inward to the central emitter contact, without shorting any of the transistor junctions.

The base contact is a C-shaped, metal strip 8, adherent to surface 2 wholly between the edges of junctions 3 and 4, substantially concentric with the emitter contact 6 and substantially encircling the junction 3. It will be noted that tongue 5'' and lead 7 extend between the two ends of the C-shaped contact 8, so that lead 7 and the emitter contact are effectively insulated from the base contact even though the base contact substantially surrounds the emitter junction. Electrical connection to contact 8 is made through a metal strip 9 extending over and adherent to the insulating oxide layer 5. Strip 9 extends over tongue 5' across the collector junction 4, and thus provides an electrical connection from one side of the composite structure into the base layer, which in this embodiment is completely surrounded by the collector layer at the surface 2, without shorting the collector junction 4.

Various methods may be employed for forming the base and emitter contacts and leads. By way of example, the contacts and leads can be deposited in the configuration shown by direct vacuum evaporation of aluminum, or other suitable contact metal, through a mask of suitable size and shape. Alternatively, a metal coating may be deposited over the entire upper surface of the composite structure, and the unwanted metal then removed by known photoengraving techniques to leave only the contact-and-lead configuration shown. After the contacts have been deposited upon surface 2 of the semiconductor, the structure is usually heated to form an alloy at the metal-silicon interface so that good, ohmic contact between the metal and the silicon is obtained.

It will be noted that regions of high-resistivity silicon are made to underlie portions of the leads 7 and 9. The principal purpose in this is to reduce the shunt capacitance between the leads and the semiconductor body. Otherwise, an undesirably high shunt capacitance may exist in some cases since the extrinsic semiconductor regions are fairly good conductors, and the insulating layer 5 has a thickness of only one to two microns. The high-resistivity regions act essentially as insulators rather than as conductors, and thus reduce the area of closely spaced conductors that lead to high shunt capacitances. Of course, in cases where the shunt capacitance is not excessive for the purposes desired, use of high-resistivity regions as disclosed is not required.

The transistor structure is completed by an electrical contact to the collector layer, which may take the form of a metal coating 10 plated over the entire back side of the silicon body.

Even in a single transistor, as illustrated in Figs. 1 and 2, the composite semiconductor-and-lead structure provided by this invention has significant advantages. According to prior practice, electrical connection to the base and emitter contacts had to be made by fastening wires directly to the contact areas. This led to certain manufacturing difficulties, particularly in the case of small devices wherein, for example, the emitter region might be only a few mils in diameter and a few microns in thickness. Merely to position the emitter lead on the emitter contact in such small structures required the use of microscopes and micro-manipulators; and the use of any considerable pressure or considerable heat in making the joint permanent could cause sufficient damage to destroy the transistor.

By means of the present invention, the leads 7 and 9 can be deposited at the same time and in the same manner as the contacts themselves. Furthermore, leads 7 and 9 can be made as large as may be desired at the point where wires or other external circuit elements are to be attached; and such attachments can be made at a distance from the active elements of the transistor proper, so that the chances of damage to the transistor are significantly reduced.

Further advantages accrue when it is desired to incorporate more than one circuit device into a single body of semiconductor. In this way exceptionally compact and rugged circuits can be constructed. One example of such a multi-device structure is illustrated in Figs. 3 and 4.

A single-crystal body 11 of silicon, largely P-type, has a high-quality surface 12 prepared in accordance with well known transistor technology. The other side of body 11 is plated with a metal coating 13, which serves as an electrical contact to the largest P-type region and as a ground plane for the electrical circuit. Various circuit elements may be formed within and on this body of silicon. N-type and P-type dopants, restricted to specific areas by known masking techniques, are diffused through surface 12 to form a plurality of N-type and P-type extrinsic semiconductor regions, separated from the underlying P-type region and from each other by a plurality of dished, P–N junctions of various diameters and depths, all having, in this particular example, circular edges extending to surface 12 and there surrounding the overlying semiconductor regions.

Toward the left end of the structure illustrated in Figs. 3 and 4, there will be found an N-type region overlying a small P-type region and separated therefrom by a dished junction 14. The small P-type region overlies another N-type region; and the underlying N-type region in turn overlies the large, grounded P-type region and is separated therefrom by a dished junction 15. The junction between the two intermediate layers is shorted by contact 17. Consequently, this structure provides two rectifying junctions connected in series, each equivalent to a crystal diode.

Electrical connection to the upper N-type region is made through a discoid, metal contact 16, adherent to surface 12, wholly within junction 14 and substantially centered upon the N-type region. Electrical contact to the two regions between junctions 14 and 15 is made through a C-shaped metal contact 17, adherent to surface 12, wholly between the edges of junctions 14 and 15, concentric with contact 16 and substantially encircling the edge of junction 14, which extends to the surface 12.

Proceeding toward the right in the drawings, there will be found another N-type region, separated from the underlying, grounded, P-type region by a dished junction 18. Electrical connection to the N-type region in this case is made through a discoid, metal contact 19, adherent to surface 12 and substantially centered inside the edge of junction 18, which extends to the surface of the semiconductor.

Toward the right end of the structure illustrated, there will be found a small N-type region overlying a P-type region and separated therefrom by a dished junction 20. The last-mentioned P-type region in turn overlies a larger N-type region and is separated therefrom by a dished junction 21. The N-type region below junction 21 in turn overlies the grounded P-type region and is separated therefrom by a dished junction 22. In this case, the width of the P-type region between junctions 20 and 21 is less than a diffusion length, so that a substantial proportion of the electrons that cross junction 20 are collected by junction 21. The result is an N-P-N junction transistor, in which the small N-type region overlying junction 20 acts as the emitter, the P-type region between junctions 20 and 21 acts as the base, and the N-type region between junctions 21 and 22 acts as the collector. The width of the last-menttioned N-type region is greater than a diffusion length, and consequently there is little interaction between junctions 21 and 22. As will be explained hereinafter, junction 22 is normally reverse-biased and acts much as a capacitor in the overall circuit. It serves the important function of isolating the collector of the transistor from the grounded, underlying, P-type region.

Electrical connections to the three active regions of the

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