Advanced staring Si PIN visible sensor chip assembly for Bepi-Colombo mission to Mercury

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ABSTRACT

The planet Mercury, by its near proximity to the sun, has always posed a formidable challenge to spacecraft. The Bepi-Colombo mission, coordinated by the European Space Agency, will be a pioneering effort in the investigation of this planet. Raytheon Vision Systems (RVS) has been given the opportunity to develop the radiation hardened, high operability, high SNR, advanced staring focal plane array (FPA) for the spacecraft destined (Fig. 1) to explore the planet Mercury. This mission will launch in 2013 on a journey lasting approximately 6 years. When it arrives at Mercury in August 2019, it will endure temperatures as high as 350°C as well as relatively high radiation environments during its 1 year data collection period from September 2019 until September 2020. To support this challenging goal, RVS has designed and produced a custom visible sensor based on a 2048 × 2048 ($2k^2$) format with a 10 µm unit cell. This sensor will support both the High Resolution Imaging Camera (HRIC) and the Stereo Camera (STC) instruments. This dual purpose sensor was designed to achieve high sensitivity as well as low input noise (<100 e-) for space-based, low light conditions. It also must maintain performance parameters in a total ionizing dose environment up to 70 kRad (Si) as well as immunity to latch-up and singe event upset. This paper will show full sensor chip assembly data highlighting the performance parameters prior to irradiation. Radiation testing performance will be reported by an independent source in a subsequent paper.

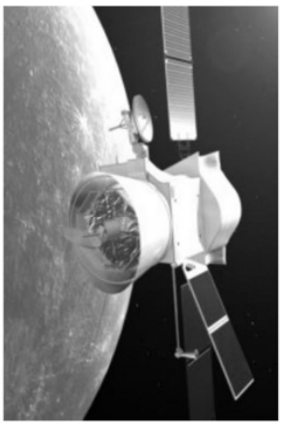

Fig. 1. Artist rendition of the Bepi-Colombo spacecraft

Keywords: Si PIN, Sensor Chip Assembly, Visible, Focal Plane Array, Bepi-Colombo

1 INTRODUCTION

RVS has been an industry leader in the development of visible and infrared sensors critical to space applications for over four decades. Building upon these prior successes, RVS is a key partner with the Selex-Galileo science team working to advance the state of the art in visible and infrared sensors for the next generation of planetary missions. Scheduled to launch in 2013, ESA's Bepi Colombo mission to Mercury will provide the best understanding of the least explored planet in the solar system. It will gather scientific data on the composition, geophysics, atmosphere, magnetosphere and history of Mercury. Bepi-Colombo has two separate spacecraft with two separate objectives: the Mercury Planetary Orbiter (MPO) will map the planet; the Mercury Magnetospheric Orbiter (MMO) will study the magnetosphere. The MPO carries a suite of instrument payloads to meet the principle science objectives. One of the main platforms is the SIMBIO-SYS: Spectrometers and Imagers for MPO Bepi-Colombo Integrated Observatory System. That platform in turn hosts the Stereo Camera (STC), the High Resolution Imaging Camera (HRIC), and Visible Infrared Hyperspectral Imager (VIHI). The focal plane assembly (FPA) for the STC/HRIC is the chief focus for this paper. RVS is also supplying the FPA for the VIHI instrument.

The challenges of designing a dual purpose camera to support a mission to Mercury are many: vibration and shock encountered during the launch, the proximity to the sun causes extreme thermal gradients, the sensors must operate over very wide dynamic ranges, and the entire sensor assembly must be able to withstand the radiation environment. After a

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thorough trade space analysis, the inherent advantages of Si PIN staring FPA technologies for this application led RVS to our present design.

Hybrid FPAs using Silicon PIN (Si PIN) diodes are an excellent choice for high sensitivity space applications. Being backside illuminated, Si PIN detectors have 100% fill factor and very high quantum efficiency clear through the near IR wavelengths. Between 450 nm and 850 nm, Si PIN detectors combined with Raytheon's anti-reflective coating, produces detectors with 8% spectral flatness and peak quantum efficiencies above 92% in the spectral range of interest. Excellent signal performance, coupled with Si PIN's inherent radiation tolerance, makes them an excellent choice for space-based applications requiring high sensitivity. Another advantage of using a hybrid technology is the ability to utilize a modern CMOS foundry for the readout integrated circuit (ROIC), enabling great flexibility, high density, and low power. The detector is then fabricated in a dedicated detector foundry where the processes can be optimized for best performance without regard for the needs of the separate CMOS circuit. In the case of this FPA, this approach enables an architecture which combines the ability to readout multiple windows at a relatively high frame rate thru a single analog output while retaining a simple electrical interface and 120 mW power budget.

RVS responded to these challenges by designing a radiation tolerant, four mega-pixel, mixed-signal FPA for this high sensitivity visible imaging application. Each pixel is composed of a Si PIN detector connected to a snap-shot source follower unit cell in the readout electronics. Relatively small 10 µm pixels are used to collect the incoming photon signal. The readout architecture contains one full-speed voltage mode analog output operating at 5 MPPS as well as one reference output. Details of this sensor performance as well as an update for Raytheon's Si PIN visible sensor efforts will be given in this paper.

2 READOUT INTEGRATED CIRCUIT DESIGN

The readout electronics were designed to support both STC and HRIC using a 2048 × 2048 active pixel array with a 10 µm × 10 µm unit cell. The basic design incorporates both snapshot as well as integrate-then-read operation at the output rate of 5 MPPS readout speed. As shown in the Fig. 2 block diagram of the readout, the active sensing array is situated in the upper right-hand portion allowing the possibility of one or two sided butting. All the control and output pads are located at the bottom of the layout. The full array is read out on one analog output and one optional reference output is provided for calibration and noise mitigation. The 5.5 V CMOS process provides a full well capacity greater than 120,000 e- with a charge conversion gain of approximately 20 µV/e-. Very low noise, less than 100 e- RMS with a goal of 60 e- RMS, is obtained with this source-follower unit cell design. A 72 bit serial command register allows programmable mode controls and adjustments of reference biases, integration time, and other critical performance parameters. Programmable windowing on a frame by frame basis is also controlled through the same command word. Windowed frames can overlap and window sizes can vary from 1 to 2048 in the row direction with one row resolution and from 128 to 2048 with 64 column resolution. Using extensive experience working with the ROIC foundry, RVS incorporated designs that have been proven to be total dose radiation, Single Event Upset (SEU) and Single Event Latchup (SEL) tolerant. The ROIC is designed to provide full specification operation from -5 to 25° C and non-specification performance over the temperature range of -60 to 40° C,

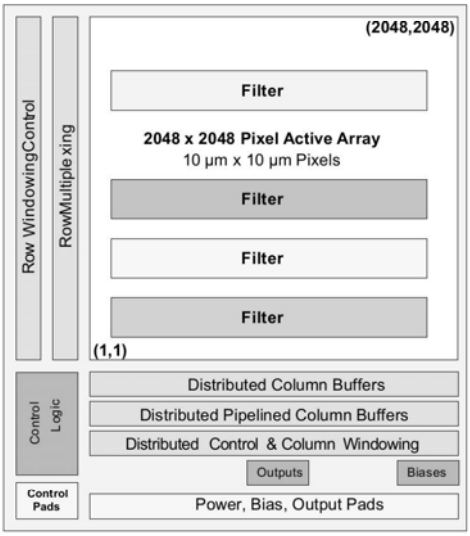

Fig 2. Block diagram of the readout integrated electronics.

3 DETECTOR DESIGN AND WAFER PERFORMANCE

The fabrication of high-performance visible sensors starts with the ability to process low-defect, highly uniform PIN detectors on high resistivity six inch silicon substrates. The device structure for the visible PIN detectors consists of a p-type junction implanted in the detector side and a very thin n- type junction implanted into the light collection side. As

shown in Fig. 3, these layers are implanted into a nearly intrinsic silicon wafer, creating the P Intrinsic N structure (PIN). The interconnection to the ROIC is also shown. The detector was designed to be fully depleted at low voltages, but can be biased from 5 to 100 V to enhance performance and lower crosstalk. The final detector is thinned to approximately 40 microns to ensure less degradation from proton and neutron damage. This thickness combined with the excellent uniformity results in reduced red fringing, and enhanced red and near infrared response. Fig. 4 shows that the absolute quantum efficiency of typical thinned Si PIN detectors provides excellent QE over the entire 400 to 950 nm spectral range, and QE > 80% from 450 to 900 nm. The detector was also designed to provide excellent modulation transfer function (MTF) at all detected wavelengths, but this performance parameter has not been measured at this time.

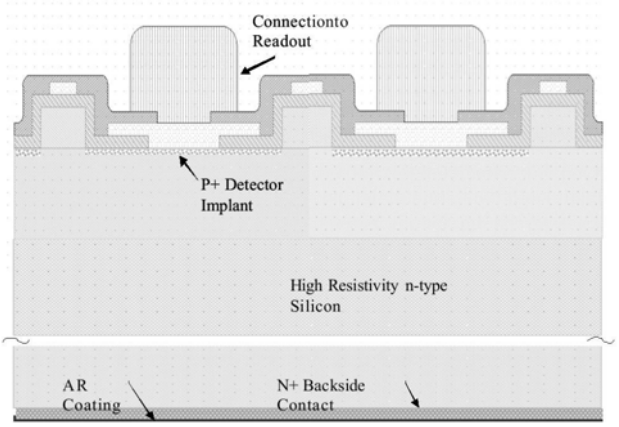

Fig 3. Physical layout of the SiPIN detector.

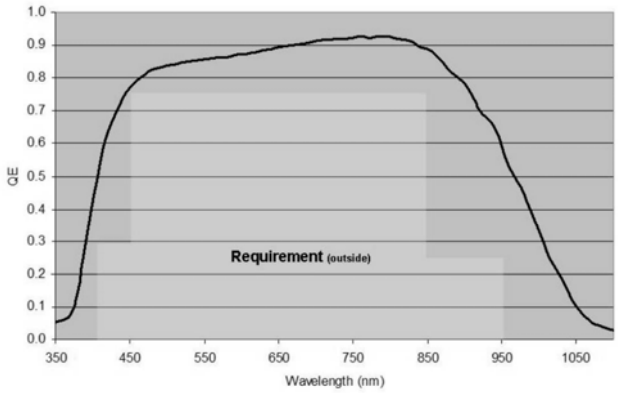

Fig 4. Typical 293K detector spectral response characteristics for a thinned SiPIN detector meet program requirements.

As will be shown from the FPA performance, the detectors demonstrated high quantum efficiency (>80% for antireflection coated devices) with excellent spectral response.

4 SENSOR CHIP ASSEMBLY DESIGN AND PERFORMANCE

As shown in Fig. 5, the detector and ROIC are fabricated separately, then bonded together to form a single hybrid structure. The traditional approach has been to deposit bumps on both the detector and the ROIC, and then hybridize the two sections together. This technique has been used for many years, but presents challenges when the pixel size is less than about 15 µm. Fig. 6 shows an array of high density indium bumps that can be used for sensors with less than 15 µm unit cells. However, this qualified approach still presents the challenges of interconnect yield and leaves a gap that would require epoxy wicking for mechanical stability during the detector thinning operation. For this application, RVS has developed a novel oxide bond interconnect solution to eliminate the need for indium bumps altogether. This technique has previously demonstrated extremely high interconnect yield and also has the advantage that it leaves no air gap between the detector and the ROIC. Fig. 7 shows a SEM picture of a detector direct bond interconnected to a ROIC. The five layers of metal in the ROIC can be seen in the lower 80% of the picture and the upper portion is the thinned silicon detector that has been oxide bonded to the ROIC and interconnected with metal vias.

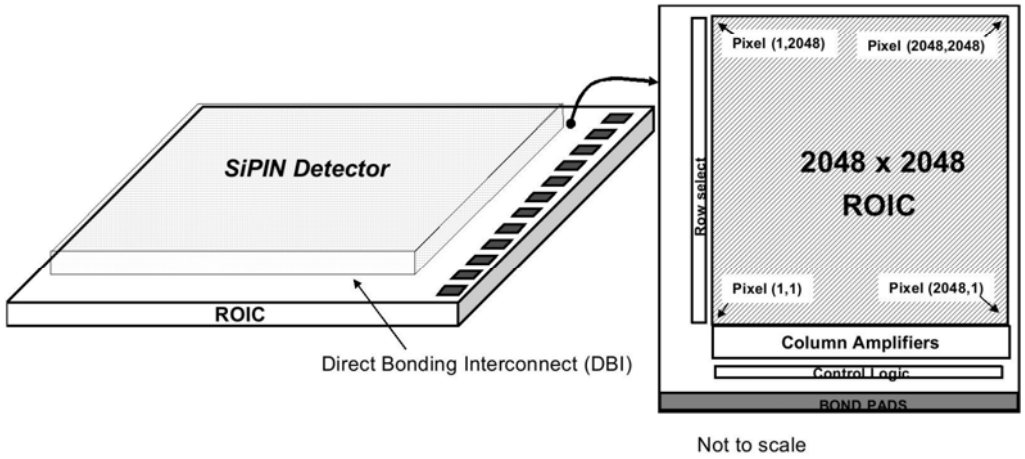

Fig 5. Block diagram of the ROIC interfaced with the detector using direct bond interconnect.

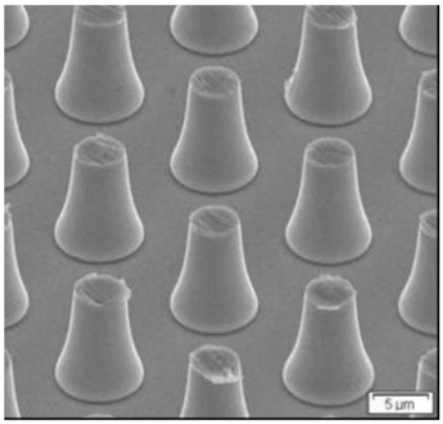

Fig 6. Traditional indium bump solution.

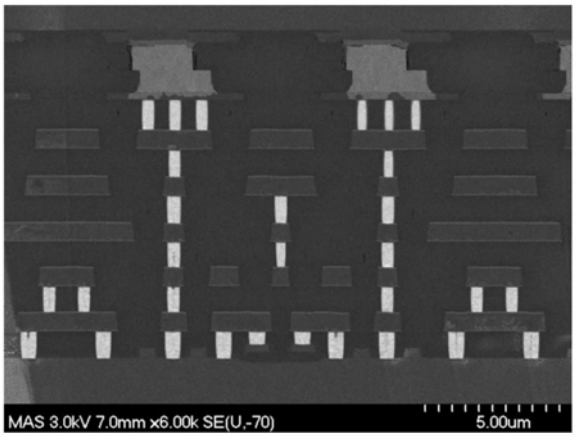

Fig 7. SEM of high density Direct Bond Interconnect showing no air gap between detector in upper portion and ROIC in lower.

For this work, sensor chip assembly (SCA) performance was evaluated using bare ROICs and the first two pathfinder engineering SCAs. The science grade sensors were not yet available in time for this paper; however, a subsequent paper presenting final performance and radiation data sets is intended to be submitted at the completion of the program.

Initial testing was performed on bare readout integrated circuits (ROIC) without detectors, four of which are depicted in Fig. 8 bonded in 124 pin leadless chip carriers. The design validation testing was performed on three separate ROICs to verify the functionality. Power was designed to be less than 120 mW and was measured to be an average of 97 mW for ten devices. In Fig. 9, a graph of the unit cell reset voltage versus the output voltage of a bare ROIC at room temperature shows that the dynamic range is > 2V and excellent linearity of ± 1% has been achieved. Other parameters validated at this stage of testing include performance of the command word operation, internal and output amplifier range, normal response to variations in integration time, as well as the windowing functions. All of these performance parameters were verified operational at both room and operating temperatures.

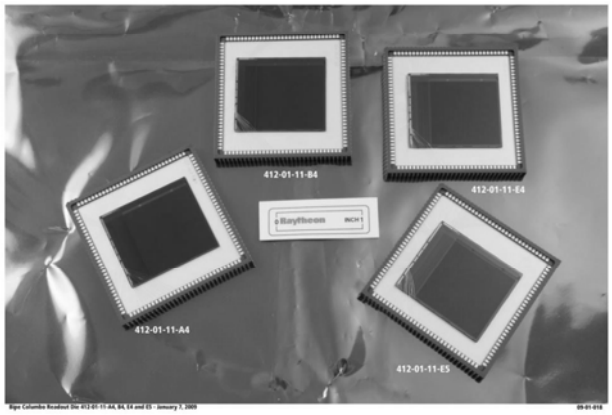

Fig. 8. Bare ROICs mounted on leadless chip carriers for test

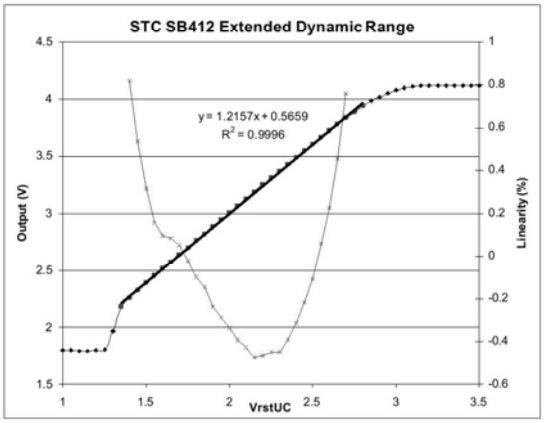

Fig. 9. Excellent linearity and dynamic range was verified at 293K on a bare ROIC

Typically, the SCAs are tested at 273K, although they are capable of operating from 200-300K. The SCAs were tested under several different flux conditions and spectral ranges to simulate the variety of expected modes of operation. For this application, the sensor was designed to operate with detector currents ranging from a minimum of 1×10^6 ph/s/pixel to a maximum of 2×10^9 ph/s/pixel. This photon flux range results in detector currents ranging from 160 fA to 320 pA. For the quantum efficiency (QE) measurements, the test conditions used F/17 optics, pass band filters ranging from 450 to 900 nm, and an integrating sphere source. These test conditions resulted in a flux level hitting the detector ranging from 6×10^{11} ph/cm^2-s to 2×10^{14} ph/cm^2-s.

To begin to analyze the sensor chip assembly test data, the first concern is the number of pixels that are interconnected and respond to visible light. For basic signal response, a pixel was considered operable if the measured response was 0.5 to 1.5 times the mean response of the array. Applying this operability criteria, the functional operability for the two pathfinder engineering arrays was found to be 99.96% and 99.99%, respectively. The histogram and grey-scale data is shown in Figs. 10 and 11 for SCA ENG-01 and SCA ENG-02. These plots demonstrate very high pixel interconnect yield with only 278 and 1835 of more than 4.23 million pixels unresponsive.

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