

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

SONY CORPORATION,  
Petitioner,

v.

RAYTHEON COMPANY,  
Patent Owner.

---

Case IPR2016-00209  
Patent 5,591,678

---

Before JO-ANNE M. KOKOSKI, JENNIFER MEYER CHAGNON, and  
JEFFREY W. ABRAHAM *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

I. INTRODUCTION

Sony Corporation (“Petitioner”) filed a Petition for *inter partes* review of claims 1–18 (“the challenged claims”) of U.S. Patent No. 5,591,678 (Ex. 1001, “the ’678 patent”). Paper 2 (“Pet.”). Raytheon Company (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 10 (“Prelim. Resp.”).

We have authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and for the reasons explained below, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail with respect to all of the challenged claims. *See* 35 U.S.C. § 314(a). Accordingly, we institute trial as to claims 1–18 of the ’678 patent.

*A. Related Proceedings*

The ’678 patent has been asserted in *Raytheon Co. v. Samsung Electronics Co.*, No. 2:15-cv-00341 (E.D. Tex.), and *Raytheon Co. v. Sony Kabushiki Kaisha*, No. 2:15-cv-00342 (E.D. Tex.). Pet. 1; Paper 5, 2. Petitioner also has challenged the ’678 patent in *Sony Corp. v. Raytheon Co.*, Case IPR2015-01201 (“the 1201 IPR”). Pet. 1–2; Paper 5, 2.

*B. The ’678 Patent*

The ’678 patent, titled “Process of Manufacturing a Microelectric Device Using a Removable Support Substrate and Etch-Stop,” relates to a method of fabricating a microelectronic device, in which the microelectronic device is moved from one support to another during fabrication. Ex. 1001, 1:12–13. According to the ’678 patent, “[t]he invention permits microelectronic devices to be prepared using well-established, inexpensive thin-film deposition, etching, and patterning techniques, and then to be further processed singly or in combination with other such devices, into more complex devices.” *Id.* at 2:9–14.

Figure 1 of the '678 patent is reproduced below.

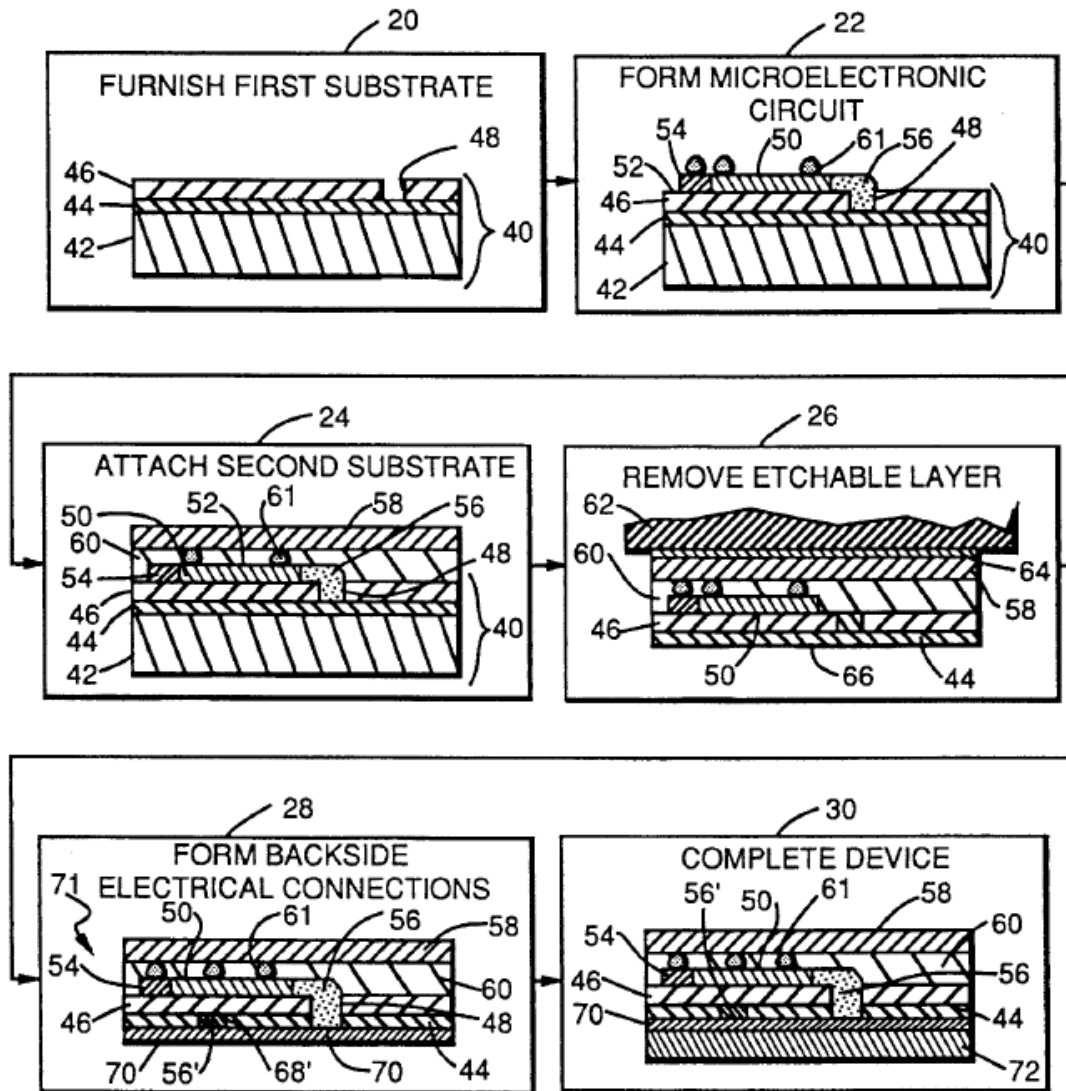


FIG. 1.

Figure 1 is a process flow diagram of the method of the '678 patent, schematically illustrating each stage of fabrication of a microelectronic device formed in accordance with the method. *Id.* at 3:48–50. As shown in box 20, first substrate 40 is provided, the first substrate including etchable layer 42, etch-stop layer 44, and wafer layer 46. *Id.* at 3:65–4:2. As noted in the '678 patent, “[s]uch substrates can be purchased commercially,” or

“prepared by applying well-known microelectronic techniques.” *Id.* at 4:2, 4:22–23. In a preferred embodiment, etchable layer 42 is a layer of bulk silicon, etch-stop layer 44 is a layer of silicon dioxide, and wafer layer 46 is a layer of single crystal silicon. *Id.* at 4:3–15.

Microelectronic circuit element 50 is formed in wafer layer 46, as shown in box 22. *Id.* at 4:37–52. The ’678 patent notes that “the present invention is not limited to any particular circuit element 50,” and, for example, “can include many active devices such as transistors,” or “may be simply a patterned electrical conductor layer that is used as an interconnect between other layers of structure in a stacked three-dimensional device.” *Id.* at 4:55–56, 4:47–52.

Second substrate 58 is attached to the structure, as shown in box 24. *Id.* at 5:14–44. Second substrate 58 may comprise, for example, silicon or aluminum oxide, and optionally may include a microelectronic device deposited therein. *Id.* at 5:18–25. Etchable layer 42 is removed by etching, as shown in box 26. *Id.* at 5:45–6:9. The entire structure may be attached temporarily to base 62, which may be a piece of aluminum oxide (particularly, sapphire), to protect the structure against etch attack. *Id.* at 5:47–49. As described in the ’678 patent, the “etchant is chosen so that it attacks the etchable layer 42 relatively rapidly, but the etch-stop layer 44 relatively slowly or not at all.” *Id.* at 5:52–54.

“Back-side electrical connections are formed through the [exposed] etch-stop layer 44 (for direct back-side interconnects 56’) and through the etch stop layer 44 and the wafer layer [46] to the microelectronic circuit element 50 (for indirect front-side interconnects [56]),” as shown in box 28. *Id.* at 6:10–14. The connections are formed by patterning etch-stop layer 44

using well-known patterning techniques. *Id.* at 6:14–17. Electrical conductor layer 70 may be deposited over etch-stop layer 44 and back side electrical connections 56, 56'. *Id.* at 6:44–49.

As shown in box 30 of Figure 1, final structure 71 may be joined with another microelectronic device 72, to form a three-dimensional structure comprising structures 71, 72. *Id.* at 6:50–58, Fig. 2.

*C. Illustrative Claim*

Of the challenged claims, claims 1, 11, and 13 are independent. Claims 2–10 depend, directly or indirectly, from claim 1; claim 12 depends from claim 11; and claims 14–18 depend, directly or indirectly, from claim 13. Claim 1 of the '678 patent, reproduced below, is illustrative of the challenged claims:

1. A method of fabricating a microelectronic device, comprising the steps of:

furnishing a first substrate having an etchable layer, an etch-stop layer overlying the etchable layer, and a wafer overlying the etch-stop layer;

forming a microelectronic circuit element in the exposed side of the wafer of the first substrate opposite to the side overlying the etch-stop layer;

attaching the wafer of the first substrate to a second substrate; and

etching away the etchable layer of the first substrate down to the etch-stop layer.

Ex. 1001, 8:5–16.

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.