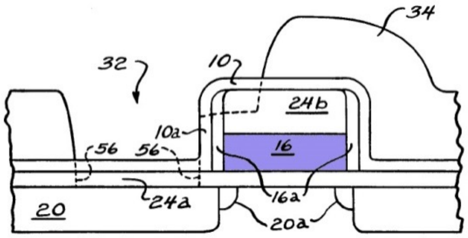
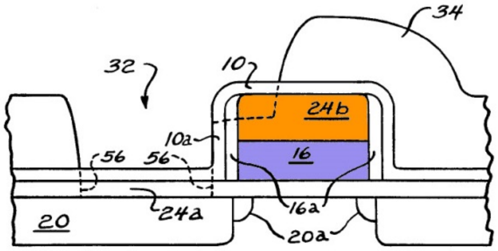
Heath anticipates claims 1, 2, and 4-10 of U.S. Patent No. 6,784,552, Nulty et al. (“the ’552 Patent”) under 35 U.S.C. § 102

Prior Art Cited in this Chart:
U.S. Patent No. 4,686,000, Heath (“Heath”)

Claim Language	Heath
Claim 1	
A structure, comprising:	“Another object of the invention is to provide a technique for self-aligning contacts in a semiconductor structure despite the use of interlevel dielectric, which ordinarily is relatively thick.” **Col. 5, lines 16-19.**
a conductive layer disposed over a substrate;	“FIGS. 8A and 8B show a gate electrode 16 and an active area 20 in the substrate to the left of gate electrode 16.” **Col. 9, lines 50-52.** **Figure 8C**  FIG. 8C
a first insulating layer on the conductive layer:	“Oxide layer 24 covers the active area 20 and the top of gate electrode 16.” **Col. 9, lines 52-53.** **Figure 8C**  FIG. 8C
a contact region in said first insulating layer;	“A contact window is to be opened to the active area 20.” **Col. 9, lines 56-57.** “The etching in any event will etch the part of layer 10 in FIG. 7 generally between lines 42 for opening a contact window to the source/drain region 20.” **Col. 9, lines 21-23.** **Figure 7**

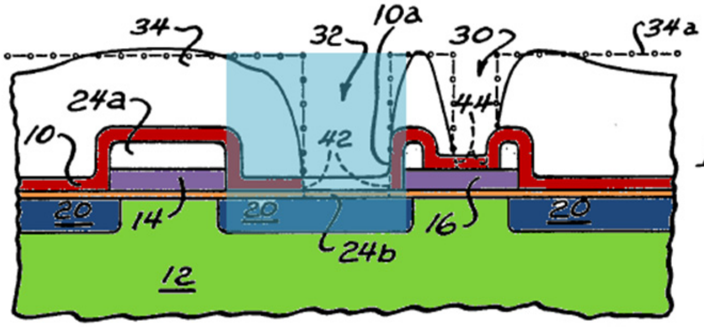
<table>
<tr><th>Claim Language</th><th>Heath</th></tr>
<tr><td></td><td>


FIG. 7

Figure 8C

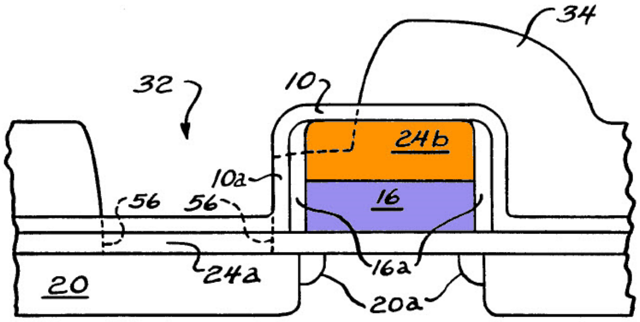


FIG. 8C
</td></tr>
<tr><td>at least one insulating spacer in the contact region adjacent to the first insulating layer; and</td><td>
"This structure results from implantation techniques combin[ed] with the addition of a sidewall spacer 16a. The spacer is formed after the source/drain implant 20a, a 'light' doese implant (generally between 5x10^{12} and 5x10^{13} ions/cm^2), but before the heavy source/drain implant 20 (illustratively 6x10^{15} ions/cm^2). In this case, spacer 16a formed illustratively of oxide, is 0.1-0.3μm thick and remains in the structure after completion of the circuit."

Col. 10, lines 17-25.

Figure 8C

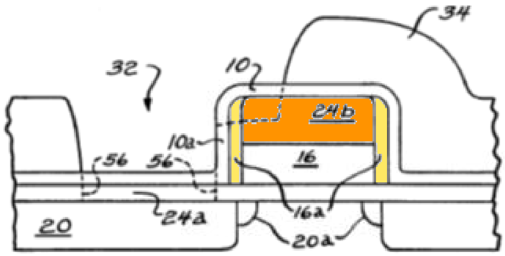
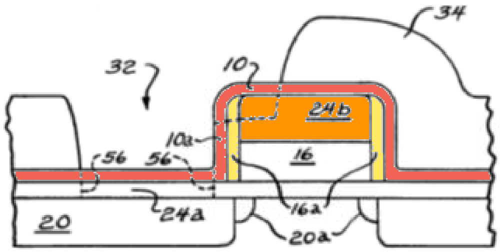
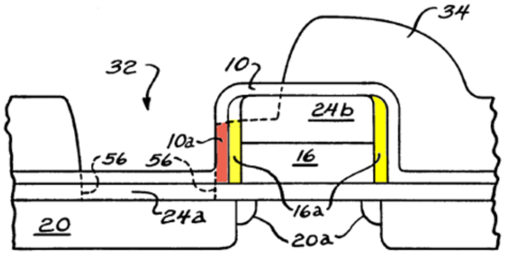
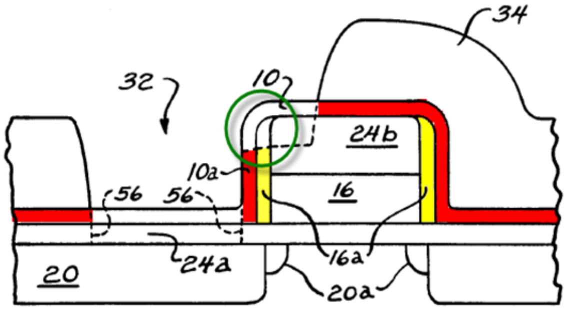
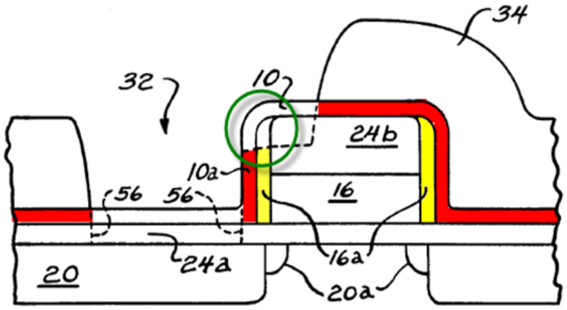
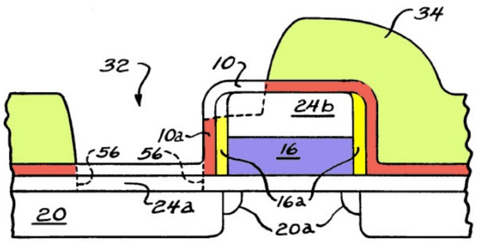


FIG. 8C
</td></tr>
<tr><td>an etch stop material over said first insulating layer and adjacent to the</td><td>
"Turning to FIG. 5, etch stop layer 10 is added to this intermediate, partially complete structure. Preferably, this is a layer of silicon nitride (Si_3N_4) which is put on by a chemical vapor deposition using Silane (SiH_4) or dichlorosilane (SiH_2Cl_2) with ammonia (NH_3)."
</td></tr>
</table>

Claim Language	Heath
insulating spacer, the etch stop material being a different material from the insulating spacer,	**Col. 8, lines 18-21.** "Consequently, etching will occur first along dotted lines 54, and the part of interlevel dielectric layer 34 between lines 54 will be etched away using the etchant described supra. Such etching will stop when its reaches nitride layer 10." **Col. 9, lines 63-66.** "In this case, spacer 16a formed illustratively of oxide is 0.1-0.3μm thick and remains in the structure after completion of the circuit." **Col. 10, lines 23-25.** **Figure 8C**  FIG. 8C
wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.	"Some oxide 24b will remain on the top of gate electrode 16 even after the etch exposes the source/drain region 20 within the contact window, and because the nitride removal is anisotropic, the 'stick' 10a will remain on the side, so no short to electrode 16 can occur." **Col. 10, lines 7-11.** **Figure 8C**  FIG. 8C
Claim 2	
The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride.	"Turning to FIG. 5, etch stop layer 10 is added to this intermediate, partially complete structure. Preferably, this is a layer of silicon nitride (Si_3N_4) which is put on by a chemical vapor deposition using Silane (SiH_4) or dichlorosilane (SiH_2Cl_2) with ammonia (NH_3)." **Col. 8, lines 18-21.**
Claim 4	

Claim Language	Heath
The structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.	“Next, the etchant is changed as described supra, and the part of layer 10 between dashed lines 56 is removed, leaving the vertical ‘stick’ 10a of layer 10.” **Col. 10, lines 1-3.** **Figure 8C**  FIG. 8C
Claim 5	
The structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.	“Next, the etchant is changed as described supra, and the part of layer 10 between dashed lines 56 is removed, leaving the vertical ‘stick’ 10a of layer 10.” **Col. 10, lines 1-3.** **Figure 8C**  FIG. 8C
Claim 6	
The structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer.	“Consequently, etching will occur first along dotted lines 54, and the part of interlevel dielectric layer 34 between lines 54 will be etched away using the etchant described supra.” **Col. 9, lines 63-65.** **Figure 8C**

Claim Language	**Heath**
	 FIG. 8C
Claim 7	
The structure of claim 6, further comprising a second conductive material in the contact region.	"As shown below, the requirement that the field oxide edge be vertical can be relaxed somewhat depending on the extent of the diffusion of the source/drain implant underneath that edge. Thus metallization can be added, and contact can be made to the source/drain region without shorting to the top or edge of a polysilicon element or the substrate under the edge of a field oxide." **Col. 6, lines 8-15.** "Briefly, one way in which the invented process can be applied to a single poly system using silicide in a CMS system is as follows: 1. grow thin oxide on silicon substrate; 2. deposit and dope polysilicon; 3. deposit silicide and oxide, mask, etch and anneal oxide/silicide/poly layer, leaving some gate oxide in the active area regions; 4. mask for N channel source/drain implants; 5. implant arsenic or phosphorous for N channel source/drain and heat drive if desired; 6. mask for and implant P channel source/drain implants; 7. mask and etch contact windows to silicide/poly layer but not source/drain regions; 8. deposit nitride layer; 9. deposit BPS (densify, reflow, and activate implants); 10. mask contact windows to silicide/poly electrode and source/drain regions; 11. etch through BPSG to nitride layer; 12. (densify and reflow BPSG and activate implants); 13. etch through nitride layer and underlying oxide to source/drain and silicide, leaving a "stick of etch stop; 14. add metal or other conductive material for interconnects." **Col. 11, line 52 – Col. 12, line 10.**
Claim 8	
A structure, comprising:	***See* claim 1, *supra*.**
a first electrically conductive material formed in and/or on a surface of a substrate;	"This structure results from implantation techniques combin[ed] with the addition of a sidewall spacer 16a. The spacer is formed after the source/drain implant 20a, a 'light' doese implant (generally between $5x10^{12}$ and $5x10^{13}$ ions/cm^{2}), but before the heavy source/drain implant 20 (illustratively $6x10^{15}$ ions/cm^{2}). In this case, spacer 16a formed illustratively of oxide, is 0.1-0.3µm thick and remains in the structure after completion of the circuit." **Col. 10, lines 17-25.**

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