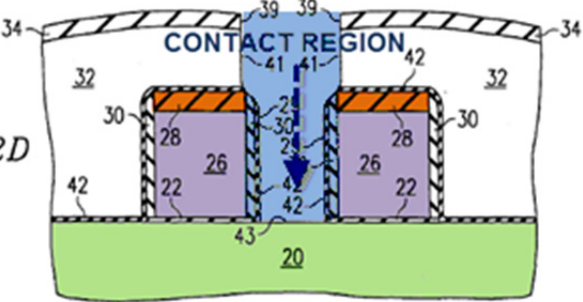


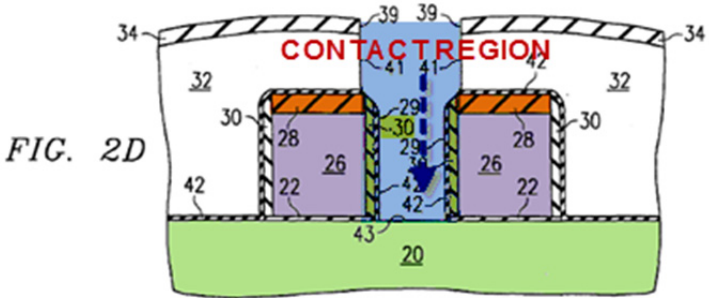
**Havemann anticipates claims 1-12 of U.S. Patent No. 6,784,552, Nulty et al.  
 (“the ’552 Patent”) under 35 U.S.C. § 102**

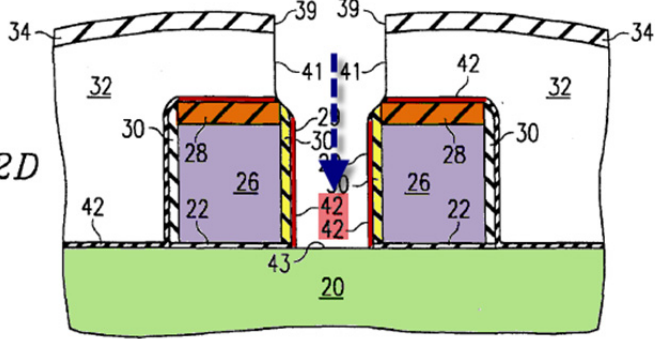
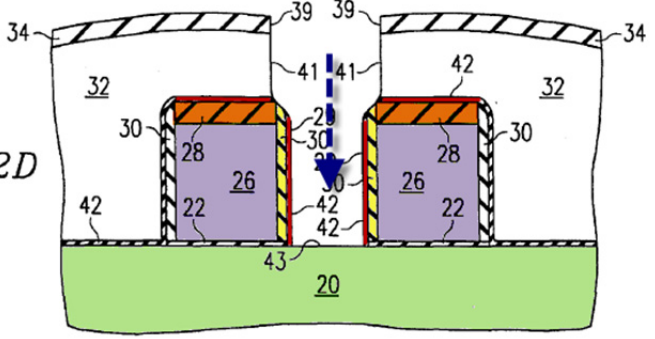
Prior Art Cited in this Chart:

U.S. Patent No. 5,482,894, Havemann (“Havemann”)

Claim Language	Havemann
<b>Claim 1</b>	
A structure, comprising:	<p>“The present invention relates to a method of producing and a structure for self-aligned contacts on semiconductor devices.”  <b>Col. 2, lines 10-11.</b></p>
a conductive layer disposed over a substrate;	<p>“Conformal dielectric 30 deposited on the sidewalls of conductors 26 may also be thinned at this point (e.g., if layer 30 is used in a known manner to align ion implantation to substrate 20, layer 30 may require thinning after implantation to reduce the aspect ratio of insulated gap 29).  <b>Col. 5, lines 10-14.</b></p> <p><b>Figure 2D</b></p>
a first insulating layer on the conductive layer;	<p>“FIG. 1B shows the structure after patterning and etching by known methods to form two conductors 26, including insulating conductor caps 28, separated by a gap 24 with a relatively high aspect ratio (1.4:1 aspect ratio shown).”  <b>Col. 3, lines 62-65.</b></p> <p><b>Figure 2D</b></p>
a contact region in said	<p>“Preferably, a short anisotropic etch of the conformal layer follows</p>

Claim Language	Havemann
<p>first insulating layer;</p>	<p>these steps if contact is to be made to the substrate in the gap (which may then be followed by a deposition of conducting material in the gap to form an electrical contact to the substrate.”  <b>Col. 2, lines 62-66.</b></p> <p>“Finally, as illustrated in FIG. 11, contact plug 40, formed of a conducting material (e.g. a composite comprised of a refractory metal underlayer with a tungsten overlayer) may be deposited in cap window 39 and contact window 41 (which includes the portion of insulated gap 29 underlying window 39) to form a contact to the substrate at gap bottom 43.”  <b>Col. 4, line 63 – Col. 5, line 1.</b></p> <p><b>Figure 2D</b></p>  <p><i>FIG. 2D</i></p>

Claim Language	Havemann																																															
<p>at least one insulating spacer in the contact region adjacent to the first insulating layer; and</p>	<table border="1" data-bbox="586 296 1365 1146"> <thead> <tr> <th data-bbox="586 296 695 359">Drawing Element</th> <th data-bbox="695 296 927 359">Preferred or Specific Examples</th> <th data-bbox="927 296 1122 359">Generic Term</th> <th data-bbox="1122 296 1365 359">Other Alternate Examples</th> </tr> </thead> <tbody> <tr> <td data-bbox="586 359 695 422">20</td> <td data-bbox="695 359 927 422">Single-crystal silicon</td> <td data-bbox="927 359 1122 422">Substrate</td> <td data-bbox="1122 359 1365 422"></td> </tr> <tr> <td data-bbox="586 422 695 464">22</td> <td data-bbox="695 422 927 464">Thermally-grown oxide (SiO<sub>2</sub>)</td> <td data-bbox="927 422 1122 464">Gate oxide</td> <td data-bbox="1122 422 1365 464">Silicon nitride</td> </tr> <tr> <td data-bbox="586 464 695 558">26</td> <td data-bbox="695 464 927 558">Polysilicon w/ refractory metal silicide overlayer</td> <td data-bbox="927 464 1122 558">Conductors</td> <td data-bbox="1122 464 1365 558">Aluminum, copper, tungsten, platinum, titanium</td> </tr> <tr> <td data-bbox="586 558 695 621">28</td> <td data-bbox="695 558 927 621">Thermally-grown oxide</td> <td data-bbox="927 558 1122 621">Insulating conductor cap</td> <td data-bbox="1122 558 1365 621">CVD oxide, silicon nitride, doped oxides, silicon oxynitride</td> </tr> <tr> <td data-bbox="586 621 695 716">30</td> <td data-bbox="695 621 927 716">Thermally-grown oxide</td> <td data-bbox="927 621 1122 716">Conformal dielectric layer</td> <td data-bbox="1122 621 1365 716">CVD oxide, silicon nitride, silicon oxynitride</td> </tr> <tr> <td data-bbox="586 716 695 789">32</td> <td data-bbox="695 716 927 789">Allied Signal 515 Series SOG</td> <td data-bbox="927 716 1122 789">Organic-containing dielectric layer</td> <td data-bbox="1122 716 1365 789">Amorphous Teflon, parylene, polyimide</td> </tr> <tr> <td data-bbox="586 789 695 884">34</td> <td data-bbox="695 789 927 884">CVD silicon dioxide</td> <td data-bbox="927 789 1122 884">Inorganic cap layer</td> <td data-bbox="1122 789 1365 884">Inorganic SOG, silicon nitride, doped oxides, silicon oxynitride</td> </tr> <tr> <td data-bbox="586 884 695 915">36</td> <td data-bbox="695 884 927 915"></td> <td data-bbox="927 884 1122 915">Photoresist</td> <td data-bbox="1122 884 1365 915"></td> </tr> <tr> <td data-bbox="586 915 695 1052">40</td> <td data-bbox="695 915 927 1052">Tungsten w/ refractory metal underlayer</td> <td data-bbox="927 915 1122 1052">Contact plug</td> <td data-bbox="1122 915 1365 1052">Aluminum, polysilicon, copper, titanium, tantalum, titanium nitride, refractory metal silicides</td> </tr> <tr> <td data-bbox="586 1052 695 1146">42</td> <td data-bbox="695 1052 927 1146">Silicon nitride</td> <td data-bbox="927 1052 1122 1146">Conformal dielectric overlayer</td> <td data-bbox="1122 1052 1365 1146">Thermal oxide, CVD oxide</td> </tr> </tbody> </table>				Drawing Element	Preferred or Specific Examples	Generic Term	Other Alternate Examples	20	Single-crystal silicon	Substrate		22	Thermally-grown oxide (SiO <sub>2</sub> )	Gate oxide	Silicon nitride	26	Polysilicon w/ refractory metal silicide overlayer	Conductors	Aluminum, copper, tungsten, platinum, titanium	28	Thermally-grown oxide	Insulating conductor cap	CVD oxide, silicon nitride, doped oxides, silicon oxynitride	30	Thermally-grown oxide	Conformal dielectric layer	CVD oxide, silicon nitride, silicon oxynitride	32	Allied Signal 515 Series SOG	Organic-containing dielectric layer	Amorphous Teflon, parylene, polyimide	34	CVD silicon dioxide	Inorganic cap layer	Inorganic SOG, silicon nitride, doped oxides, silicon oxynitride	36		Photoresist		40	Tungsten w/ refractory metal underlayer	Contact plug	Aluminum, polysilicon, copper, titanium, tantalum, titanium nitride, refractory metal silicides	42	Silicon nitride	Conformal dielectric overlayer	Thermal oxide, CVD oxide
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<p>an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a</p>	<p>Col. 6, line 6.</p> <p>Figure 2D</p>  <p>“Additional material may subsequently be deposited as a conformal dielectric overlayer 42, e.g., using thermal oxide or silicon nitride (see FIG. 2C).”</p> <p>Col. 5, lines 16-18.</p>																																															

Claim Language	Havemann
<p>different material from the insulating spacer,</p>	<p>“If conformal layer 30 and overlayer 42 differ in materials (e.g. thermal oxide and nitride), relatively selectively between the two materials may also be exploited to design a structure wherein conductor caps 28 are extremely thin.”  <b>Col. 5, lines 27-31.</b></p> <p><b>Figure 2D</b></p> 
<p>wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.</p>	<p>“Cap window 39 supplies a pattern for etching a contact window 32 by a suitable anisotropic (substantially in one direction, usually vertical) etch.”  <b>Col. 4, lines 37-40.</b></p> <p>“At some geometry, this method becomes ineffective for reliably forming such self-aligned contacts; the limited selectivity between dielectric layers and limited etch anisotropy (ability to etch in one direction only, e.g. vertically) make such a process difficult for high aspect ratio gaps.”  <b>Col. 2, lines 1-6.</b></p> <p><b>Figure 2D</b></p> 
<p><b>Claim 2</b></p>	

Claim Language	Havemann
<p>The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride.</p>	<p>“The selective etch process is designed to remove material from the second dielectric layer faster than it removes material from the first dielectric layer. Silicon nitride and silicon dioxide (of different varieties) are used for the dielectric layers; relative etch selectivity for the best of such dielectric combinations is on the order of 10:1.”  <b>Col. 1, 55-60.</b></p>
<p><b>Claim 3</b></p>	
<p>The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide.</p>	<p>“The selective etch process is designed to remove material from the second dielectric layer faster than it removes material from the first dielectric layer. Silicon nitride and silicon dioxide (of different varieties) are used for the dielectric layers; relative etch selectivity for the best of such dielectric combinations is on the order of 10:1.”  <b>Col. 1, 55-60.</b></p> <p>“Additional material may subsequently be deposited as a conformal dielectric overlayer 42, e.g., using thermal oxide or silicon nitride (see FIG. 2C). This layer provides a minimal protection for substrate 20 during the O<sub>2</sub> plasma etch to remove organic-containing material from insulated gap 29.”  <b>Col. 5, lines 15-20.</b></p>

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