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Multilevel Metal Interconnection Utilizing CVD Tungsten and Liftoff Processing

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Interconnections between semiconductor devices in integrated circuits continue to present difficult problems in the tradeoffs between RC time constants, production worthiness, reliability, structural complexity, and compactibility for any single technology. A process and structure has been demonstrated for integrated circuit interconnections which uses a conformal tungsten layer deposited by chemical vapor deposition to provide step coverage into via holes of variable height. The film is then patterned with a via interconnect pattern designed for liftoff processing, layers of chromium copper and chromium are then deposited *insitu* on the wafers by way of evaporation. The undesired material is lifted off in a solvent process and the resulting metal pattern is used as the mask for the reactive ion etching of CVD tungsten. This combination of materials and process allows for high conductivity reliable interconnections with negligable step coverage problems. Processing and test information will be presented in the paper.

Key words: Tungsten, interconnect, liftoff, CVD, chemical vapor deposition

INTRODUCTION

The use of liftoff processing to define metal patterns on integrated circuits has been known for sometime[1,2] and has been improved for process simplicity and control in recent years.[3,4] The primary advantage of liftoff processing is that it allows almost any material which may be evaporated without decomposition under high vacuum conditions ($>10^{-6}$ Torr) and reasonable temperatures to be structured into thin film ULSI patterns without the requirement of anisotropic etches for processing. Some materials of interest for ULSI interconnects such as copper and complex layered films can be difficult to etch using currently available processes and equipment giving liftoff processing a distinctive advantage. The primary weakness in liftoff processing is the inherent poor step coverage over steep topography such as vertical via openings. This is because liftoff processing makes use of incomplete step coverage on resist films to allow dissolution of the resist and removal of undesired material during the resist strip process. The desire for low RC time constants and improved cross talk immunity tends to make thick insulating layers with low dielectric constants desirable, this in turn further aggravates the step coverage of conductor lines through via contacts.

The use of chemically vapor deposited tungsten on integrated circuits can provide conformal coatings of a good conductor (6–10 μm-cm).[5,6,7] This material can be etched anisotropically[8] but it is not sufficiently conductive to provide chip long interconnections on ULSI circuits without the use of very thick films which would exhibit greater cross talk and RC penalties[9,10] for many circuit designs.

The combination of the two technologies, liftoff and CVD metal, has been demonstrated to synergistically provide the individual benefits of both technologies. Agglutination of the patterned liftoff metallurgy onto the CVD tungsten allows the use of many high conductivity materials and layered films to act as the primary horizontal conductors while relying on the tungsten to provide step coverage into vias. The upper layer conductors which were used in this paper include a three layered film of chromium (600Å), copper (4500Å), and chromium (700Å) on 4500Å CVD tungsten. The second metallurgy studied using this technology was an 4% copper alloy (8KÅ) of aluminum on top of 4500Å of chemically deposited tungsten. Figure 1 provides a diagram of one interconnect level using this method of circuit interconnection.

PROCESSING OF TEST STRUCTURES

The test structures consisted of oxidized silicon substrates. Liftoff patterning was performed using the MCNC/Genesis[3,11] liftoff process which utilizes Shipley 1400-31 photoresist[12] exposed on a GCA 6300 series reduction step and repeat lithography system.[13] The stepper has an exposure wavelength of 405 nm and 0.35 numerical aperature. Following image reversal and development, the first metal conductors were deposited between the liftoff resist lines. Cr-Cu-Cr layers and aluminum +4% copper films were deposited onto the substrates. Following liftoff of the undesired metal in acetone baths, subsequent rinsing, the substrates were prepared for the new interconnect process.

Silicon nitride was first deposited by plasma assisted CVD to help protect the substrate and metal

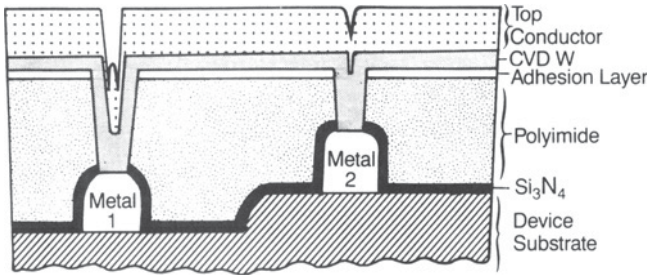


Fig. 1 — Cross section diagram of combined CVD tungsten and liftoff metal structure.

polymide[14] was spin coated on the wafer. The film was cured using oven cycles recommended by Dupont to obtain a nominal 1.2 micrometer thick film. Good surface smoothing was observed with 80% or better planarization. While thicker films may be desired for some applications, this thickness was adequate for our tests.

An etch stop layer of silicon dioxide deposited in a PECVD system was applied. This film was used to insure a good etch step was obtained during SF_6 etching, however, subsequent tungsten RIE process development reduced the need for this layer. A film of titanium (600Å) and then silicon (400Å) were sequentially evaporated to provide an anti-reflective coating and etch stop for via photolithography and via etch respectively as well as an adhesion layer for the yet to be deposited CVD tungsten.

Vias were patterned using routine photolithography. 1.5 μm Shipley 1400-31 positive photoresist was exposed on a GCA-6300 h line step and repeat system. Thinner resist films have been used successfully as a result of the effectiveness of the silicon/titanium etch step, however the samples being reported on were processed using the thicker 1.5 μm resist. The resist was developed on GCA-1000 track equipment using a Shipley MF 312 puddle process.

Via etching was performed in Applied Materials 8120 and 8110 hexode RIE systems.[17] The silicon and titanium films were first etched using a BCl_3, HCl, and oxygen gas mixture in an AME 8120. This first etch is not very selective to photoresist and therefore acts as a one step descum and etch of the vias. The second step of the etch was done in an AME 8110. Oxygen was used to etch through the polyimide, a 50% overetch was provided to insure complete etching of various depth vias, no pinholing of the upper etch step was observed. The resist was completely removed during this etch step. The final etch step was performed *insitu* in the AME 8110 reactor. This etch used a CHF_3 and oxygen mixture to penetrate the silicon nitride encapsulant layer and remove oxidized silicon and silicon from the adhesion layer surface (complete removal of the silicon was not required).

Tungsten was deposited by Chemical Vapor Deposition to a thickness of 4500Å from a tungsten hexafluoride and hydrogen mixture onto the adhesion layer and into the vias. The deposition condi-

was obtained with these conditions. A loadlocked, vertical flow LPCVD system designed at the Microelectronics Center of North Carolina and retrofitted into a conventional Bruce horizontal hotwall furnace was used for the depositions. The system holds 100 wafers per load, is self cleaning, and exhibits better than 5% thickness uniformity across a wafer and ±5% between wafers or runs when used for nonselective depositions of tungsten. A drawing of the MCNC designed deposition chamber is shown in Fig. 2.

Liftoff photolithography was performed next using the MCNC-Genesis process previously described and then the surface was plasma cleaned. The upper layer conductors were evaporated with either Cr-Cu-Cr or Al + Cu layers and the metal on top of the resist is lifted off as was done at the first metal level. Figure 3 demonstrates the excellent profiles obtained using image reversal processing, the micrograph is taken after evaporation of metal.

Etching of the tungsten layer using the evaporated patterns as etch masks was performed in a non commercial parallel plate RIE reactor of IBM design.[15,16] Sulphur hexafluoride was used as the etch gas, Table I gives the observed etch rates of various films in the reactor with 40 sccm SF_6 flow, 3.5 millitorr pressure, a bias voltage of 350 volts and 0.08 Watts per sq cm input power which was the selected etch condition for these samples. The etch was observed to be anisotropic for the conditions used and with a 50% timed overetch. The titanium adhesion layer between the conductor lines was removed during the overetch.

Table II gives a more detailed description of tungsten etch conditions and their effect on etch rate and effect on how anisotropic the etch was.

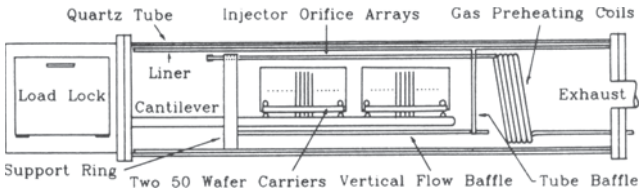


Fig. 2 — Batch LPCVD Tungsten Apparatus—Vertical Flow System.

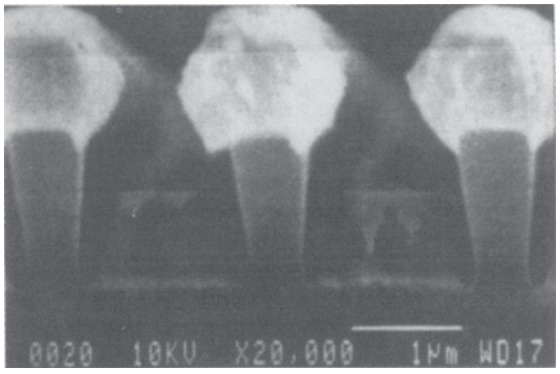


Table I. Tungsten Etch Rates

Film type	Flexible Diode SF6 (40sccm & 3.5 millitorr) angstrom/min
CVD tungsten	1510
Photoresist	300
Silicon	250
Plasma Oxide	140
Plasma Nitride	420
Polyimide	490

Bias: 350 Volts
Power Density: 0.08 watt/sq. cm

Table IIA. Degree Undercut of 1 Micrometer Tungsten Pattern Etched in Carbon Coated Cathode.

100 Watt Carbon Coated Cathode	5 mtorr		10 mtorr		50 mtorr	
	Metal	Resist	Metal	Resist	Metal	Resist
20 sccm	N/N	N/N	N/N	N/N	S/N	N/N
40 sccm	N/N	N/N	N/N	N/N	U/S	U/S
60 sccm	U/N	N/N	U/N	S/N	U/S	U/U

U = Undercut.
S = Slight Undercut.
N = No Undercut.
SF6/CF4.

Table IIB. Degree Undercut of 1 Micrometer Tungsten Pattern Etched in Anodized Aluminum Cathode.

100 Watt Anodized Aluminum Cathode	5 mtorr		10 mtorr		50 mtorr	
	Metal	Resist	Metal	Resist	Metal	Resist
20 sccm	N/N	N/N	S/N	N/N	U/U	U/S
40 sccm	S/N	N/N	U/N	S/N	U/U	U/U
60 sccm	S/S	N/N	U/S	S/N	U/U	U/U

U = Undercut.
S = Slight Undercut.
N = No Undercut.
SF6/CF4.

Passivation of the structure is then performed with PECVD silicon nitride prior to subsequent levels or patterns. A cross section of a via chain segment is shown in Figure 4. As expected, the tungsten provides conformal step coverage into the vias while the liftoff metallurgy on the via walls. Thicker tungsten films may be used to completely fill smaller vias if desired.

EXPERIMENTAL RESULTS

Sheet resistances following a 400° C 30 min 6% hydrogen in argon forming gas anneal were 44 mΩ/sq for the Cr-Cu-Cr on tungsten films and 26 mΩ/

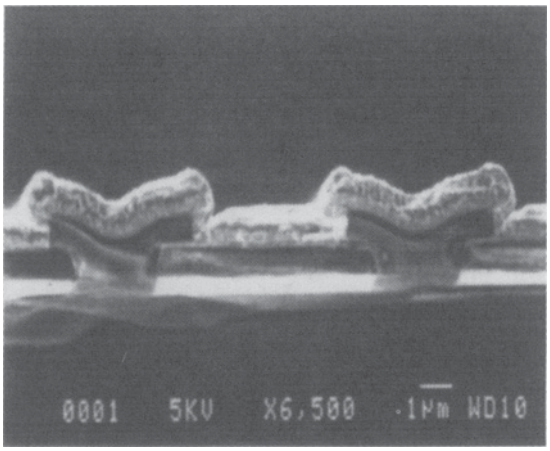
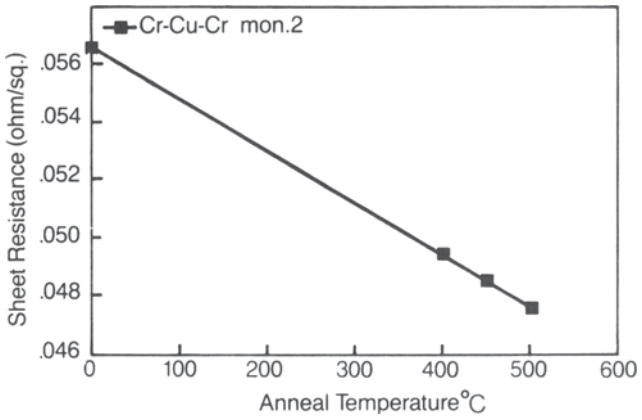


Fig. 4 — Cr-Cu-Cr via chain with CVDW underlayer (titanium adhesion layer −800Å).

sulting from the anneal. Figure 5 shows measured sheet resistance of Cr-Cu-Cr metal films on silicon dioxide after 30 min anneals at various temperatures.

Chains of various size nested vias were measured to obtain contact resistance data, the result of these measurements is shown in Fig. 6 for Cr-Cu-Cr on W, and Fig. 7 for Al + 4% Cu on W. The drop in specific via resistance with via area is primarily attributed to greater relative percentage via filling with the 4500Å tungsten film. Limited measurements of via chains of 0.8 μm in diameter exhibited slightly increased specific via resistance over the one micron vias. Kelvin structures correlated with the via chain measurements, however, they exhibited approximately 5–8% lower specific via resistances than the calculated specific via resistances measured in the via chains.

The specific via resistance distributions for the various nested via sizes of the chromium-copper-chromium on tungsten via resistance is shown in Fig. 8. Good yield and tight distribution of specific contact resistance was measured on the aluminum +4% copper samples while a higher broader distribution of resistances was measured on the chromium-copper-chromium samples. Unnested vias were



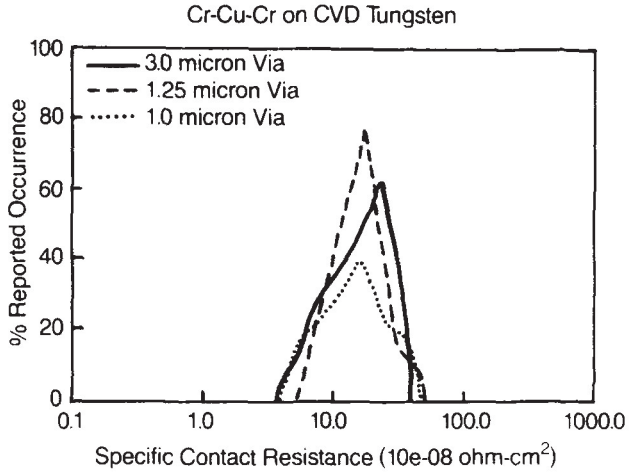


Fig. 6 — Measured distribution of specific contact resistance of via chains fabricated from 700Å Cr on 4500Å Cu on 600Å Cr, all on 4500Å CVD tungsten with similar Cr-Cu-Cr metal 1 layer.

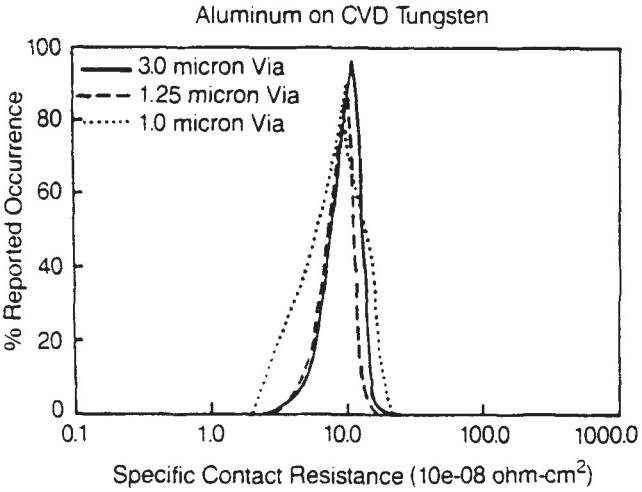


Fig. 7 — Measured distribution of specific contact resistance of via chains fabricated from 8500Å Al + 4% Cu or 4500Å CVD tungsten with Al + 4% Cu metal layer.

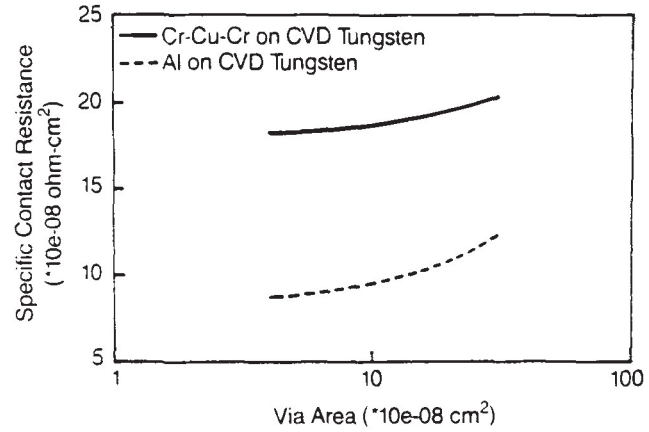


Fig. 8 — Specific contact resistance of vias for layers of Cr-Cu-

also measured, these exhibited 30% to 50% lower via chain resistances than the nested vias along with approximately twice the width distribution of contact resistances. As this process allows for excellent electrical to the walls of metal lines as well as surfaces, this observed effect can be attributed to larger effective electrical contact area in the unnested vias. The design of our unnested via structures did not completely overlap the ends of the first level metal lines so minor alignment changes resulted in large via resistance changes when unnested vias were used, although it did tend to improve via resistance with minor misalignment rather than degrade the via resistance as conventional unnested via processing would have done.

CONCLUSIONS

Successful initial results have been obtained for a new VLSI/ULSI interconnection metallurgy which combines the benefits of metal liftoff and CVD tungsten processing. Two examples of this technique have been fabricated with reasonable via chain resistances and yields. The specific contact resistances for Cr-Cu-Cr on tungsten one micrometer diameter vias were measured to be $17 \times 10^{-8}\ \Omega\ -\text{cm}^2$ nominal for one micrometer diameter vias using liftoff aluminum plus 4% copper on 4500Å tungsten. It is expected that the higher sheet resistance of the Cr-Cu-Cr film with only 4500Å copper and the Cr-Cu-Cr on tungsten interface contact resistance contributed to the marginally acceptable via chain resistance results. High aspect ratio conductors with reasonable smoothed surfaces were obtained, the ability of this type process to support high aspect ratio interconnects potentially permits low resistance interconnects at small dimensions. While further work is still required to determine how to further reduce the contact resistances of these structures as well as their reliability, this technique presents a potentially useful technique to simultaneously solve the micron and submicron ULSI interconnection issues of step coverage, via contact resistance, low effective bulk resistivity, electromigration resistance, and general reliability.

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