United States Patent [19]

Heath

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[45] **Date of Patent: Aug. 11, 1987**

[54] **SELF-ALIGNED CONTACT PROCESS**

[76] Inventor: **Barbara A. Heath,** 615 Hempstead Pl., Colorado Springs, Colo. 80906

[21] Appl. No.: **831,463**

[22] Filed: **Feb. 19, 1986**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 719,073, Apr. 2, 1985, abandoned.

[51] **Int. Cl.**[4] **H01L 21/306;** B44C 1/22; C03C 15/00; C03C 25/06

[52] **U.S. Cl.** **156/643;** 156/644; 156/646; 156/653; 156/657; 156/662; 357/23.1; 357/41; 437/235; 437/241; 437/40

[58] **Field of Search** ..... 29/580, 589, 590, 591, 29/571, 576 W; 156/643, 644, 646, 653, 657, 659.1, 656, 661.1, 662; 427/88–90; 357/23.1, 41, 49, 59, 65, 71; 148/1.5, 187

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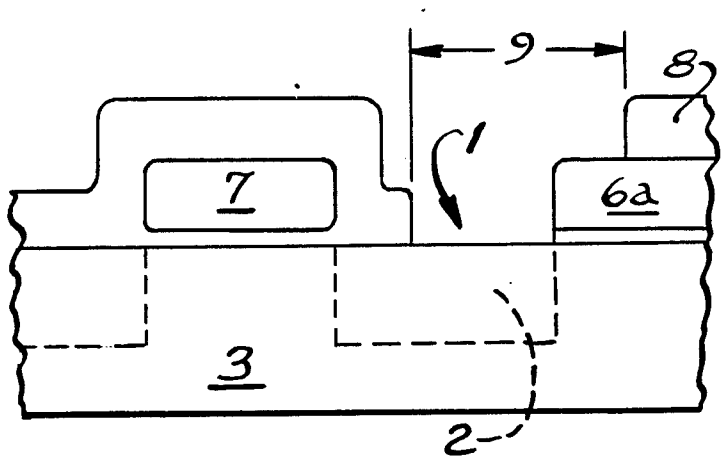
Primary Examiner—William A. Powell

[57] **ABSTRACT**

An improved process for self-aligned contact window formation in an integrated circuit leaves a "Stick" of etch stop on vertical sidewall surfaces to be protected. The technique includes, in the preferred embodiment, a layer of oxide over active areas and on top of the gate electrode of a transistor. The oxide is thicker on top of the gate electrode than over the active area. A silicon nitride layer acting as an etch stop is included between the oxide and interlevel dielectric such as BPSG. Contact windows may deviate from their intended position and partially overlie a poly edge such as a gate electrode or an isolation (field-shield) or field oxide edge. Two-step etching comprises first etching the BPSG down to the etch stop layer, then etching the etch stop and underlying oxide, leaving a "stick" of etch stop on the side of the layer to be protected. This process preserves for the second step of the etch the differential thickness ratio of the oxide over the gate electrodes as compared to the oxide over the active area. This process allows the simultaneous formation of self-aligned contacts to field oxide, field-shield, and gate electrode edges. It is independent of the type of gate dielectric, gate electrode material, and gate electrode sidewall processing.

10 Claims, 20 Drawing Figures



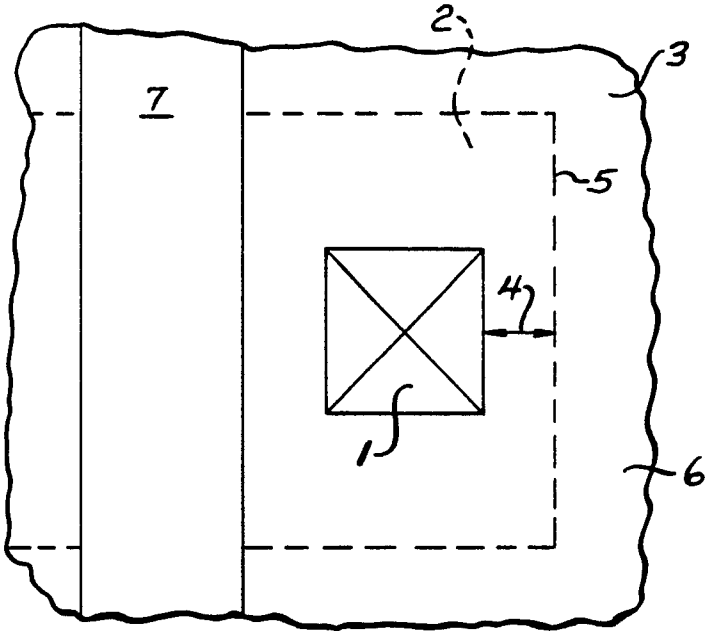


FIG. 1A

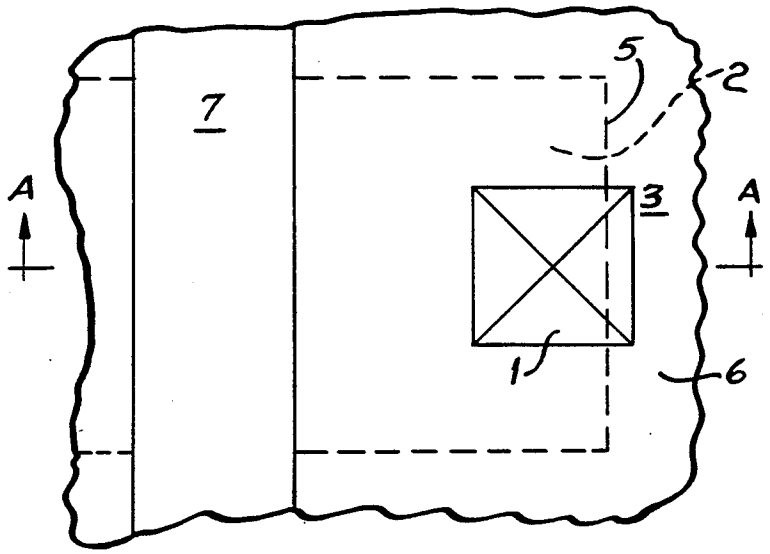


FIG. 1B

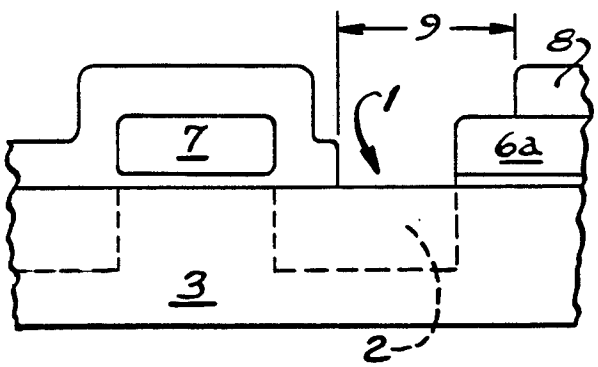


FIG. 1C

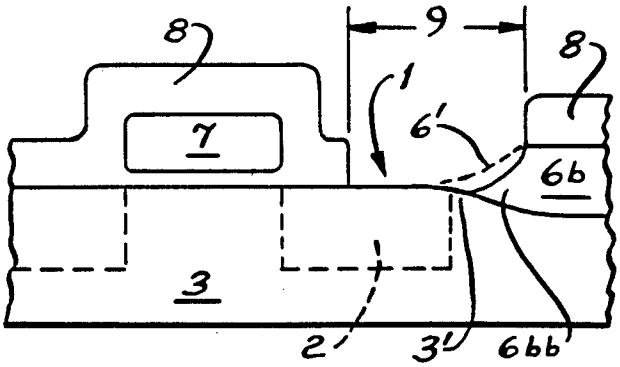
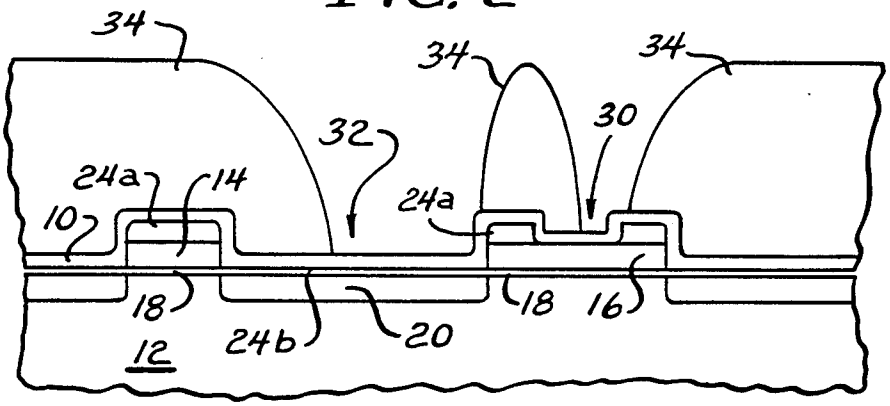


FIG. 1D

FIG. 2



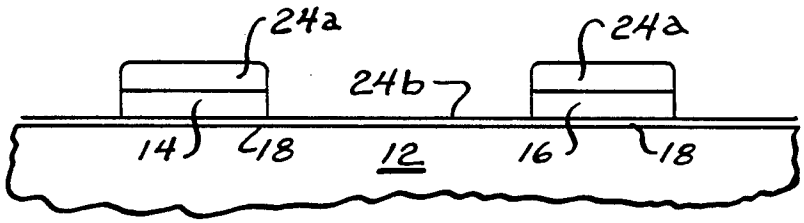


FIG. 3

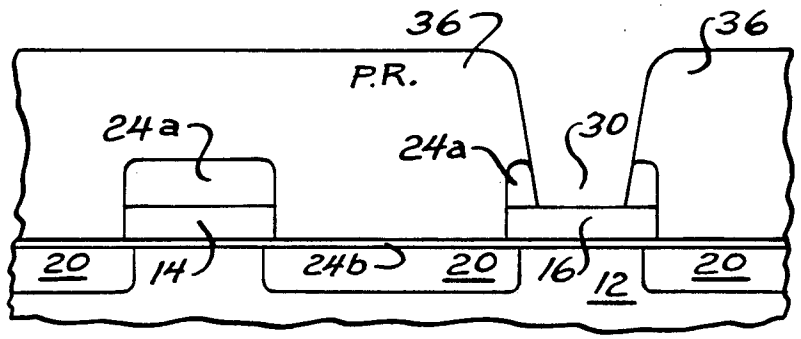


FIG. 4

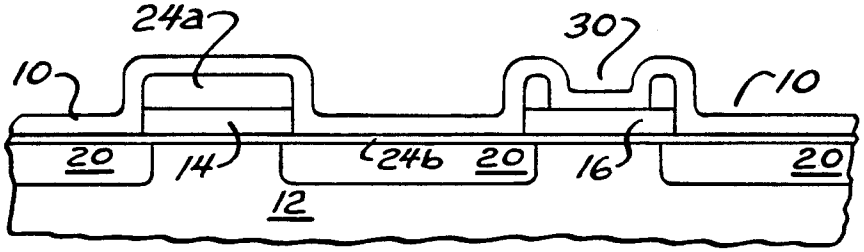


FIG. 5

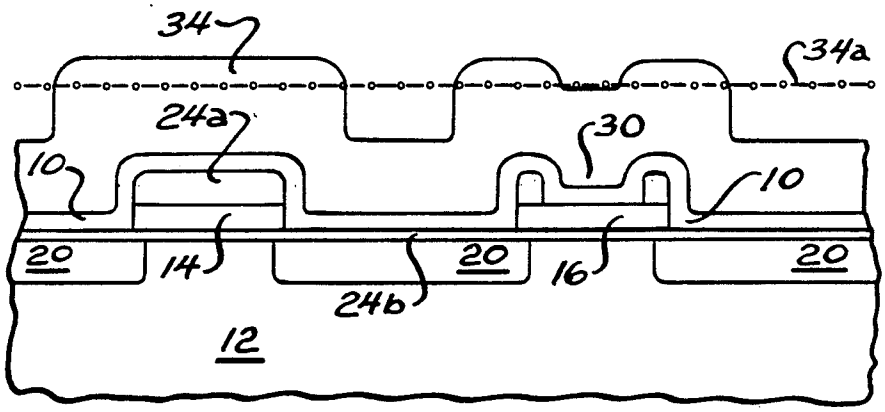


FIG. 6

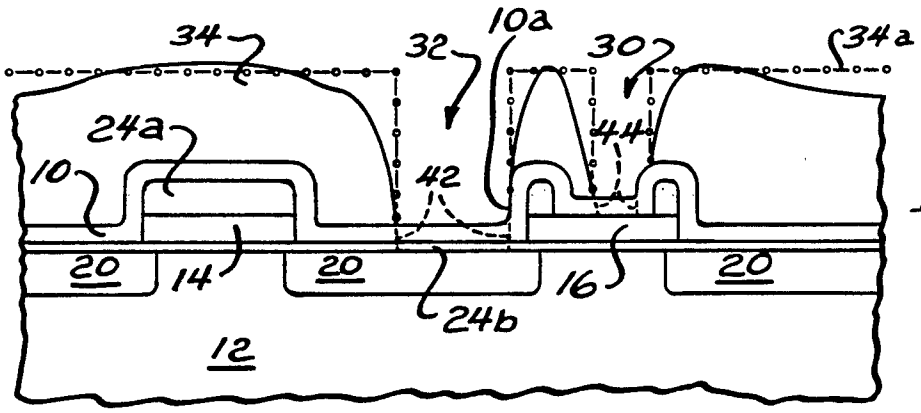


FIG. 7

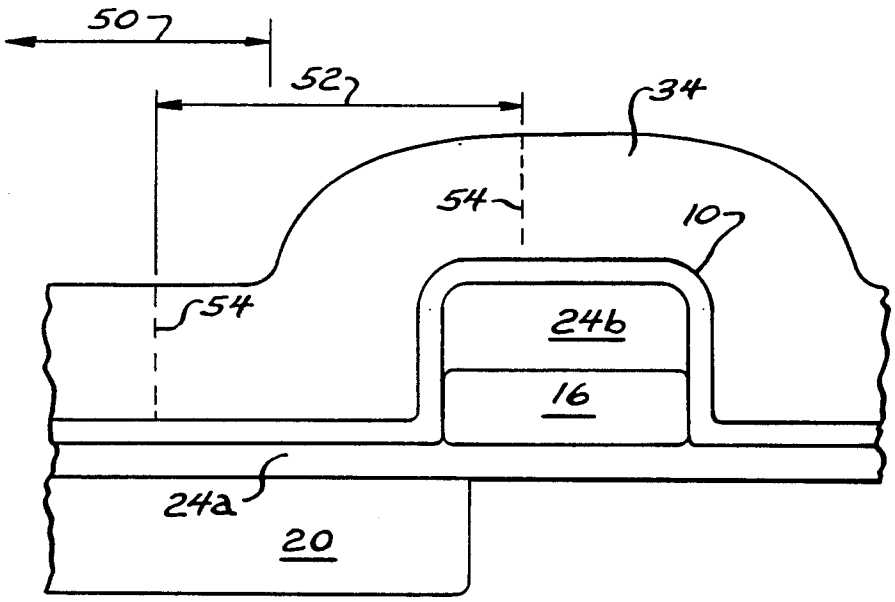


FIG. 8A

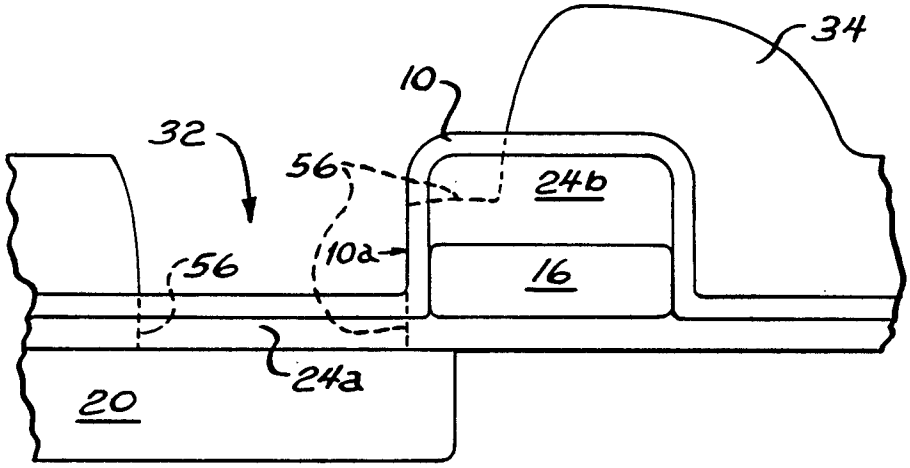


FIG. 8B

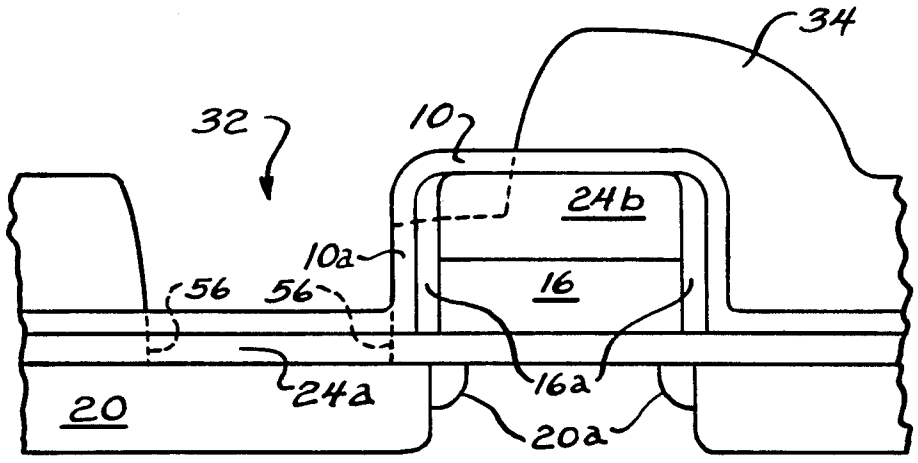


FIG. 8C

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