CONFIDENTIAL

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
RICHMOND DIVISION

SAMSUNG ELECTRONICS CO., LTD., and SAMSUNG ELECTRONICS AMERICA, INC., Plaintiffs, v. NVIDIA CORPORATION, VELOCITY MICRO, INC. D/B/A VELOCITY MICRO, AND VELOCITY HOLDINGS, LLC Defendants.	CIVIL ACTION NO. 3:14-cv-00757-REP .

REBUTTAL EXPERT REPORT OF DR. RICHARD B. FAIR REGARDING
U.S. PATENT NO. 8,252,675

titanium, or tantalum. Thus I conclude that the ’108 Korean Application discloses each element of the Claim 13 of the ’675 Patent.

56. Paragraph 47 (SAMS-NVD-19827; SAMS-NVD-0121866) refers to the layer 20 (the first metal gate electrode layer) formed of titanium nitride or tantalum nitride. Thus I conclude that the ’108 Korean Application discloses each element of the Claim 14 of the ’675 Patent.

57. In light of all of the evidence cited above, it is my opinion that ’108 Korean Application (and, of course, the English language translation of the ’108 Korean Application) discloses all of the elements of all of the asserted claims of the ’675 Patent. Dr. Lee does not challenge that the ’108 Korean Application (or its translation) fully discloses the elements of the asserted claims of the ’675 Patent in his opening expert report. I also understand that NVIDIA does not contend that any element of the asserted claims of the ’675 Patent is missing from the disclosure of the ’108 Korean Application. Should Dr. Lee or NVIDIA challenge the disclosure of the ’108 Korean Application, I will further provide rebuttal opinions to support my conclusion that the ’108 Korean Application adequately supports every element of every claim of the ’675 Patent.

V. CLAIMS 12, 13, AND 14 OF THE '675 PATENT ARE NOT INVALID IN VIEW OF THE ALLEGED PRIOR ART

A. U.S. Patent No. 8,536,660 (the “’660 patent” or “Hsu”)

58. The ‘660 patent discloses structures and methods of making dual metal gate MOS transistors in a gate last process. The ’660 patent addresses the complexity and number of steps involved in the prior art processes and focuses on how to reduce the complexity of forming metal gates for PMOS and NMOS transistors with high-k gate dielectrics over prior art methods. Hsu 2: 39-43.

59. In the ’660 patent, a semiconductor substrate having a first MOS device region and a second MOS device region is provided. Blanket-deposited first and second high-k dielectric layers are formed over the semiconductor substrate. The second high-k dielectric layer is then removed from the second MOS device region. A blanket forming first metal layer is formed over the first and the exposed second high-k dielectric layers, wherein the first metal layer has a thickness great enough for dominating a work-function of a respective MOS device.

60. Dummy gates are then fabricated. A blanket forming polysilicon layer is then deposited over the first metal layer. Masking and patterning the first and the second high-k dielectric layers, the first metal layer, and the polysilicon layer follows to form a first gate stack in the first MOS device region, and a second gate stack in the second MOS device region. Following the application of a blanket insulating layer, gate spacers on sidewalls of the first and the second gate stacks are formed by etching. Next, an inter-layer dielectric (ILD) is deposited over the semiconductor substrate and the first and the second gate stacks. The ILD is planarized to expose a top surface of the polysilicon layer. The second gate stack is etched until at least an upper portion of the first metal layer is removed to form a first opening. The first gate stack is then etched until at least an upper portion of the polysilicon layer is removed to form a second opening, wherein the first metal layer in the first gate stack is not etched. A blanket-forming second metal layer extending into the first and the second openings is deposited. A third metal layer deposition follows to fill the remaining portions of the first and the second openings. A planarization step follows to remove portions of the second and the third metal layers over the ILD. Col. 3: 48-col. 4: 13.

B. Hsu Does Not Anticipate The Asserted Claims Of The ’675 Patent

61. I am informed by counsel that NVIDIA did not disclose the ’660 Patent to Hsu, or the U.S. Patent Application Publication 2009/02340479 in their initial invalidity contention.

Therefore I understand that the Hsu reference was not timely disclosed and Dr. Lee may not be allowed to opine on the alleged invalidity of the ’675 Patent based on Hsu. Nonetheless, I present my opinion regarding Hsu in the following paragraphs in the event Dr, Lee’s opinion on Hsu is permitted..

1. Claim 6

62. Dr. Lee asserts that Hsu (the ’660 patent) discloses every limitation of, and therefore anticipates, Claim 6. Lee ’675 Report at ¶ 78. I disagree for the reasons set forth below.

a. **6(h) “depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer;”**

63. The ’660 patent does not disclose this element. Dr. Lee asserts that “Hsu discloses depositing a second metal gate electrode layer (metal layer 60) onto inner sidewalls of the spacers (spacers 243) and onto an upper surface of the patterned first metal gate electrode layer (metal layer 232), as shown in Fig. 8.” Lee ’675 Report at ¶ 106. I disagree with this assertion.

64. According to the ‘660 patent, the PMOS region is etched while the NMOS region is covered with photoresist: “In the preferred embodiment, metal layer 232 is fully removed without damaging high-k dielectric layer 224.” Hsu 6: 63-64. Thus, in this preferred embodiment the first metal gate electrode layer of the PMOS transistor, 232, is removed. As a result, a second metal gate electrode layer 60 could not be deposited onto an upper surface of the patterned first metal gate electrode layer 232, since it was previously removed.

65. The ’660 patent also states: “If, however, the selectivity of the etching is not high enough, a thin metal layer 232 may be left un-etched to protect the underlying high-k dielectric layer 224. In this case, the thickness of the remaining metal layer 232 is preferably less than 2

nm, for example, between about 0.5 nm and about 2 nm, so that it will not substantially affect the work function of PMOS device 202." Hsu 6: 64-67 to 7: 4.

66. Thus, claim element 6[h] of the '675 Patent recites an essential limitation that requires depositing a second metal layer onto an upper surface of the patterned first metal gate electrode layer. In contrast, the '660 Patent does not require the patterned first metal gate electrode layer, and teaches that the metal layer 232 is removed by etching. Even where the '660 patent discloses an embodiment where the metal layer 232 remains, it teaches etching of layer 232 so that only "a thin metal layer 232 may be left un-etched." Thus, the remaining metal layer 232 would no longer retain the upper surface of the patterned first metal gate electrode layer.

67. The upper surface of the patterned first metal gate electrode layer, 232, is shown in annotated Fig. 5 below. After dummy gate electrode 234 is etched and metal layer 232 is partially etched or removed, the resulting structure is shown in annotated Fig. 6 below.

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