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(54) **HYBRID PROCESS FOR FORMING METAL GATES OF MOS DEVICES**

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USPC 257/369, 371, 374, 410, 411, 412, 257/E27.064, E27.067, E27.108, E29.128, 257/E29.137
See application file for complete search history.

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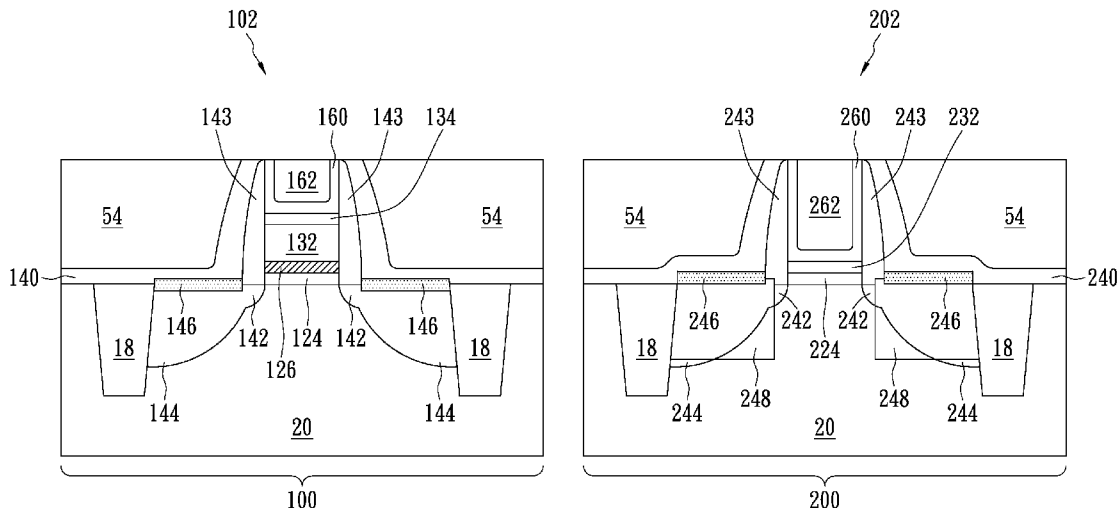
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(57) **ABSTRACT**

A semiconductor structure includes a first MOS device including a first gate, and a second MOS device including a second gate. The first gate includes a first high-k dielectric over a semiconductor substrate; a second high-k dielectric over the first high-k dielectric; a first metal layer over the second high-k dielectric, wherein the first metal layer dominates a work-function of the first MOS device; and a second metal layer over the first metal layer. The second gate includes a third high-k dielectric over the semiconductor substrate, wherein the first and the third high-k dielectrics are formed of same materials, and have substantially a same thickness; a third metal layer over the third high-k dielectric, wherein the third metal layer and the second metal layer are formed of same materials, and have substantially a same thickness; and a fourth metal layer over the third metal layer.

17 Claims, 11 Drawing Sheets



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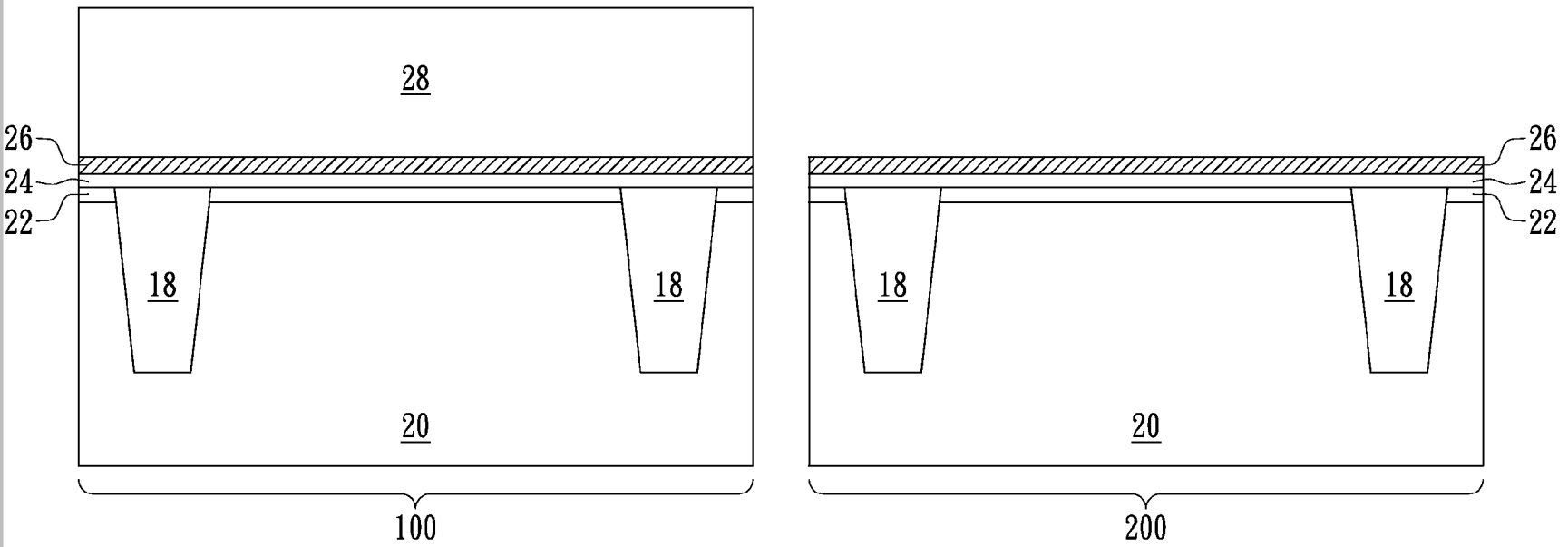


FIG. 1

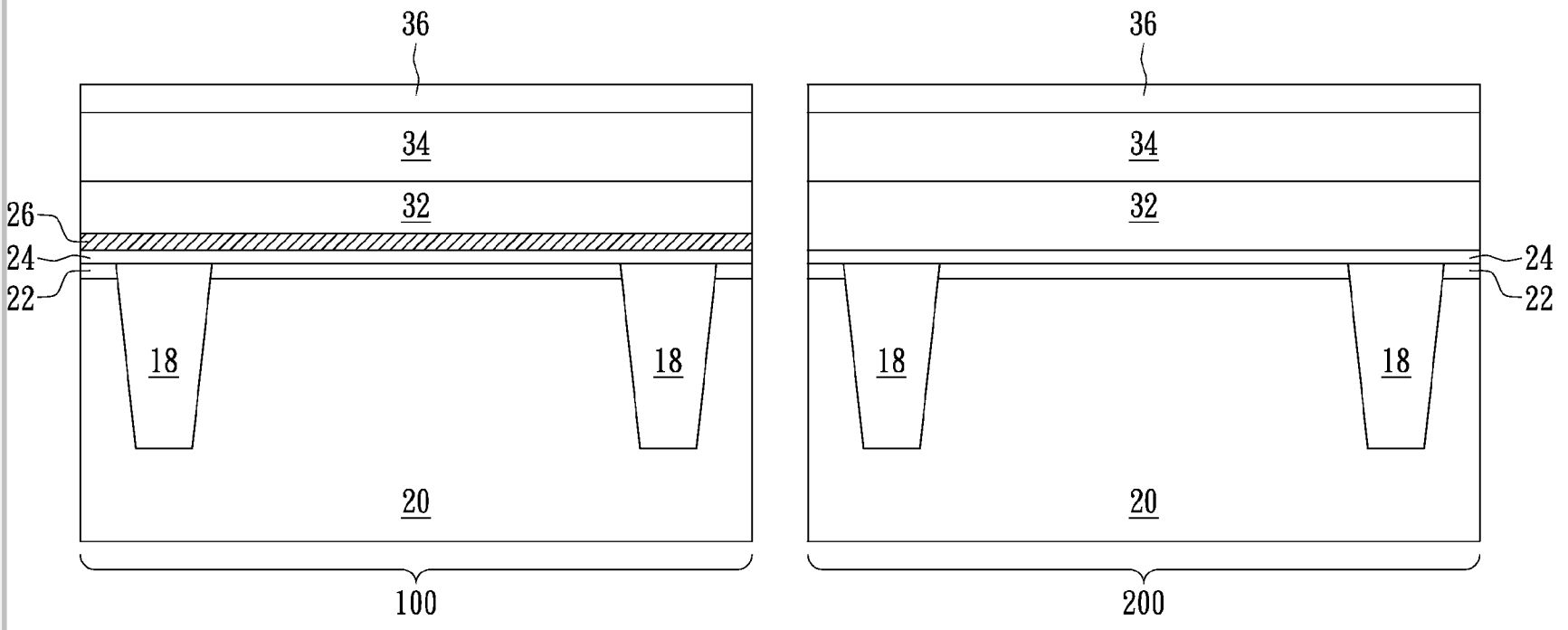


FIG. 2

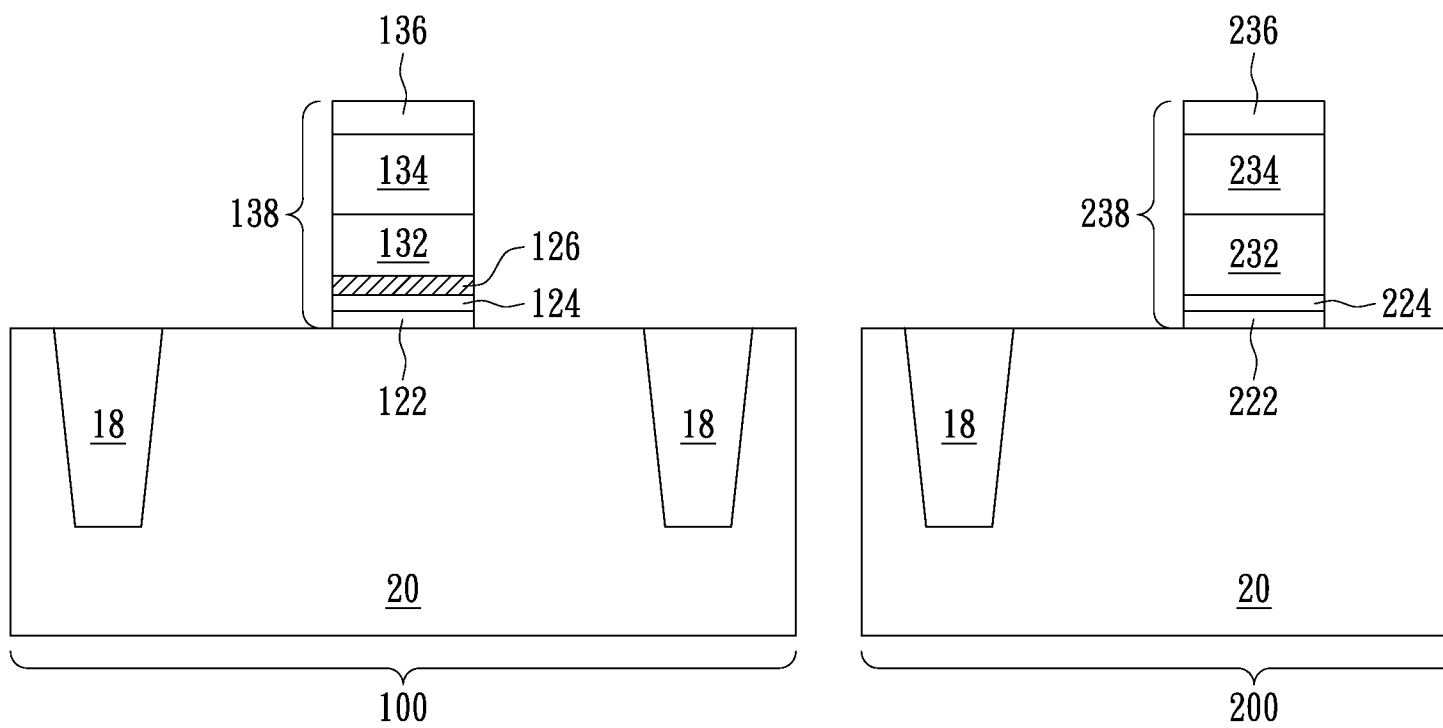


FIG. 3

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