IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Review of:	)
U.S. Patent No. 8,252,675	)
Issued: August 28, 2012	)
Application No.: 12/942,763	)
Filing Date: November 9, 2010	)

For: **Methods of Forming CMOS Transistors with High Conductivity Gate Electrodes**

FILED VIA PRPS

DECLARATION OF JACK LEE IN SUPPORT OF SECOND PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,252,675

For ease of reference, Dr. Lee refers to this second declaration as being in support of the "Second '675 Petition" challenging claims 1-8 and 10-15 of the '675 patent.

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I, Jack Lee, Professor of the Electrical and Computer Engineering Department at The University of Texas at Austin, hereby declare as follows:

I. INTRODUCTION AND QUALIFICATIONS

1. I have been retained by NVIDIA Corporation ("NVIDIA") to provide my opinion concerning the validity of U.S. Patent No. 8,252,675 (Ex. 1101, "the '675 patent") in support of its Second Petition for *Inter Partes* Review of U.S. Patent No. 8,252,675 ("Petition"). I previously submitted a declaration on June 1, 2015 in support of Petitioner's position in IPR2015-01318. The IPR2015-01318 requests institution of *inter partes* review on the '675 patent based on Yamakawa as the primary prior art reference. In Section X, I compare the difference between the reference relied upon (Hsu) in this Petition with Yamakawa, and conclude that Hsu is a stronger reference.

2. I am an expert in the field of semiconductor process technology and semiconductor design. I have over 30 years of first-hand experience as a researcher, educator, and consultant in this field.

3. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

4. From 1979 to 1984, I was a Member of Technical Staff at the

TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

5. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers ("IEEE") International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

6. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised 40 students who received a doctoral degree under my guidance. I am currently the Cullen Trust for Higher Education Endowed Professor in Engineering #4 in the Department of Electrical and Computer Engineering at UT Austin.

7. My current research interests include: high-K gate dielectrics and metal gate electrodes in semiconductor devices (CMOS/MOSFETs); semiconductor device fabrication processes, characterization and modeling; dielectric processes, characterization and reliability; and alternative transistor channel materials. My research has been partially supported by grants from the

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