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# United States Patent [19]

[11] Patent Number: **5,355,339**

Oh et al.

[45] Date of Patent: **Oct. 11, 1994**

[54] **ROW REDUNDANCY CIRCUIT OF A SEMICONDUCTOR MEMORY DEVICE**

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[75] Inventors: **Seung-Cheol Oh; Moon-Gone Kim**, both of Suwon, Rep. of Korea

### OTHER PUBLICATIONS

B. F. Fitzgerald et al., "Memory System with High-Performance Word Redundancy," IBM Technical Disclosure Bulletin, vol. 19, No. 5, Oct. 1976, pp. 1638-1639.

[73] Assignee: **Samsung Electronics Co.**, Suwon, Rep. of Korea

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*Assistant Examiner*—Son Dinh  
*Attorney, Agent, or Firm*—Cushman, Darby & Cushman

[21] Appl. No.: **91,839**

[22] Filed: **Jul. 13, 1993**

### [30] Foreign Application Priority Data

Jul. 13, 1992 [KR] Rep. of Korea ..... 12437

### [57] ABSTRACT

[51] Int. Cl.<sup>5</sup> ..... **G11C 7/00**

[52] U.S. Cl. .... **365/200; 371/10.2**

[58] Field of Search ..... 365/200, 225.7, 230.03; 371/10.1, 10.2

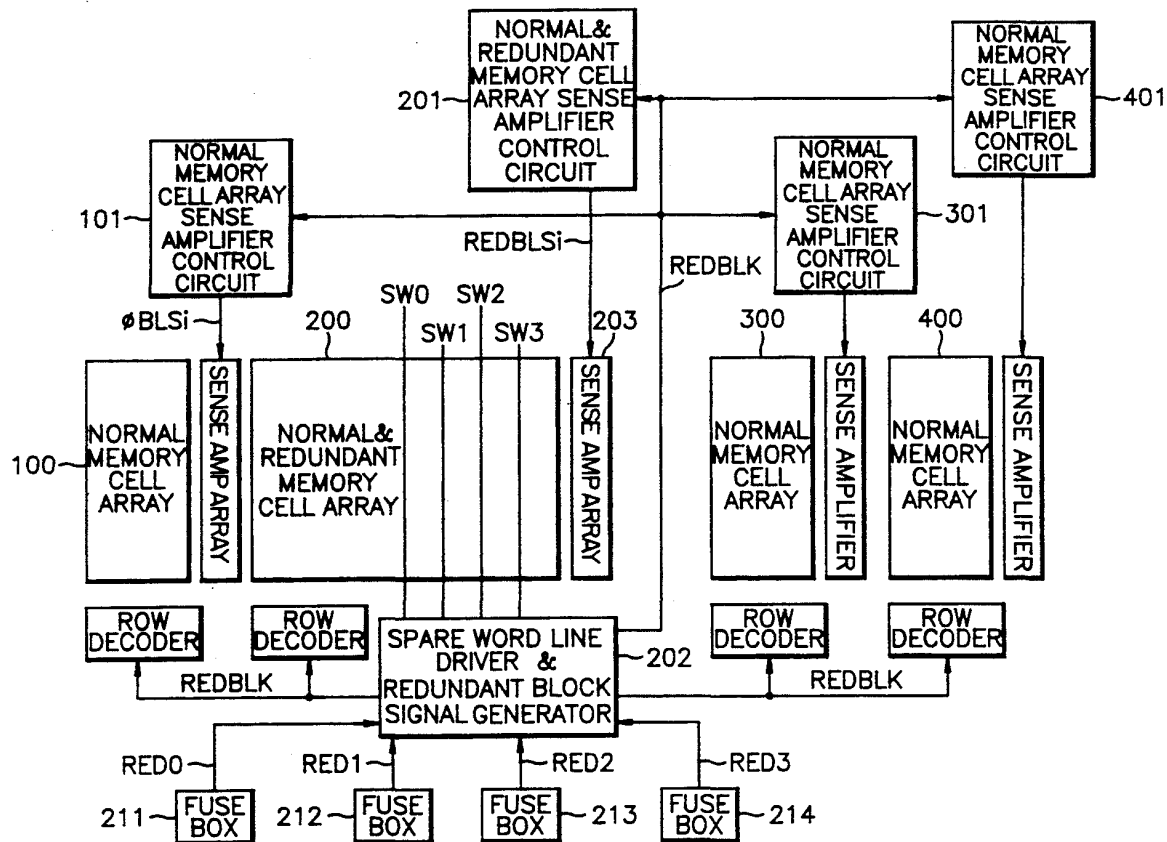
Disclosed is a semiconductor device with redundancy for replacing a memory cell with a predetermined defect with additional spare cells. In a semiconductor memory device having a plurality of normal submemory arrays, the present invention discloses a redundancy technique that allows any redundant address decoder to be used with any of the submemory arrays. This maximizes efficiency in redundant repairs as well as maximizes the use of the chip area.

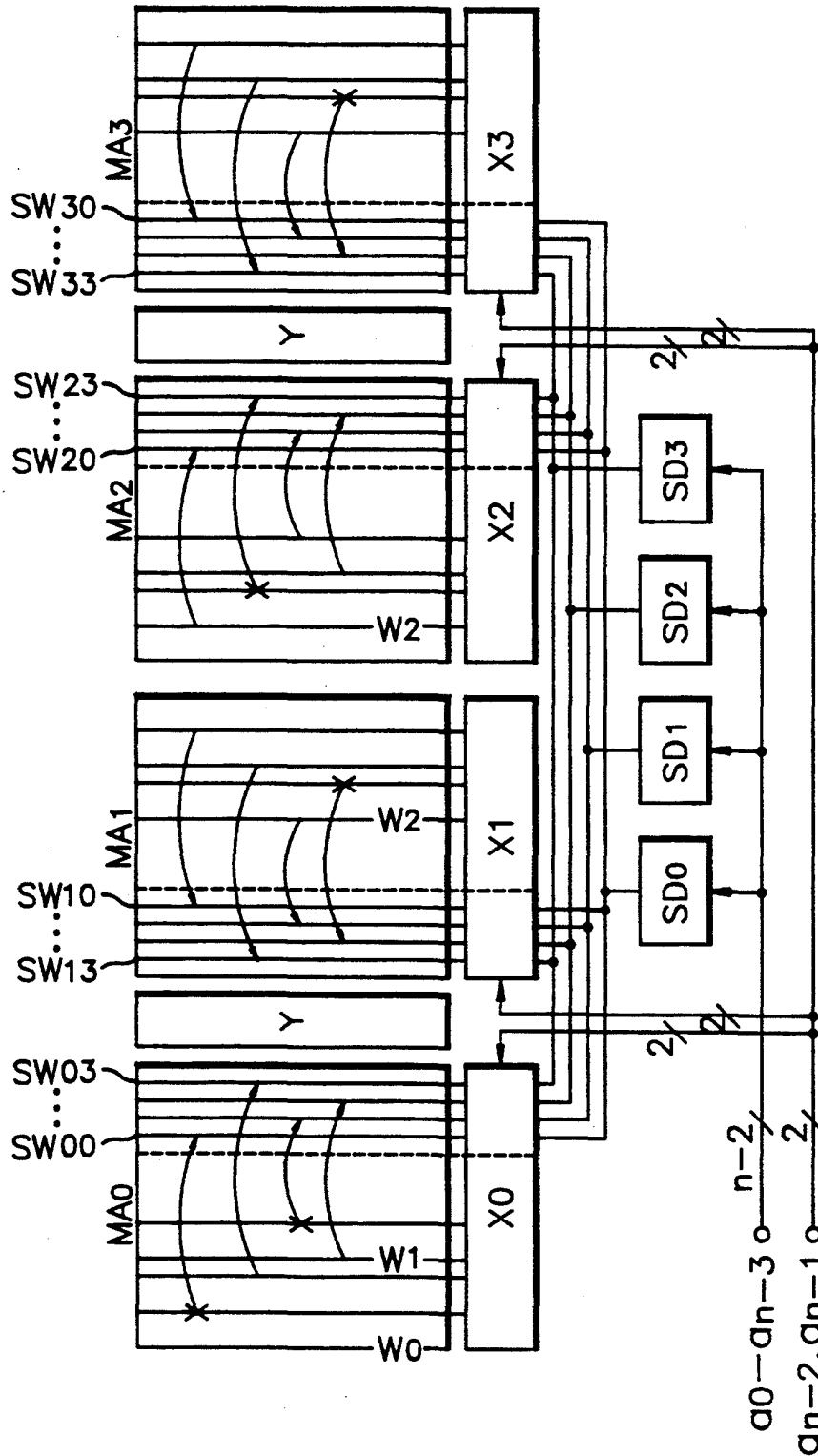
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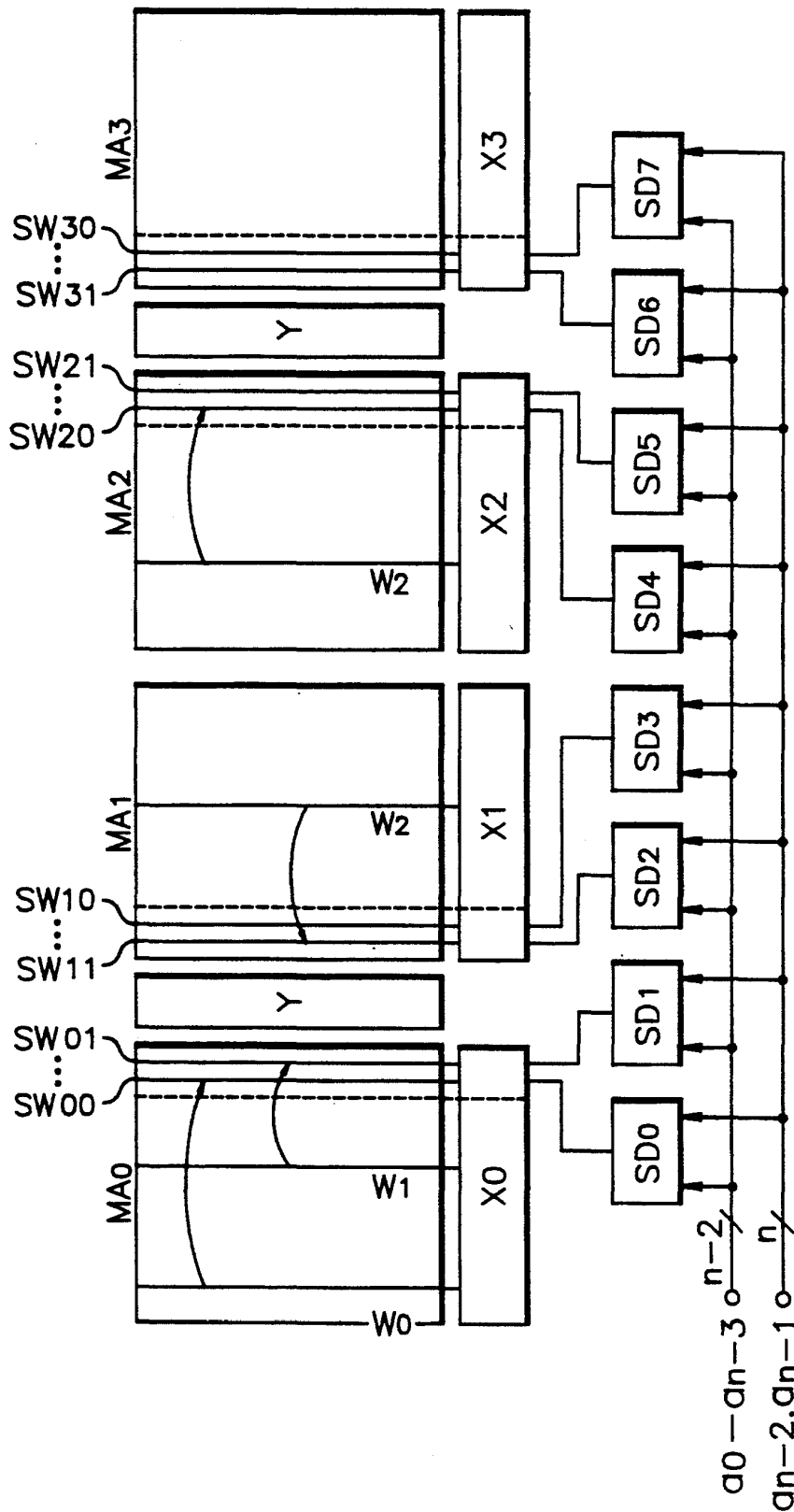
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**11 Claims, 10 Drawing Sheets**

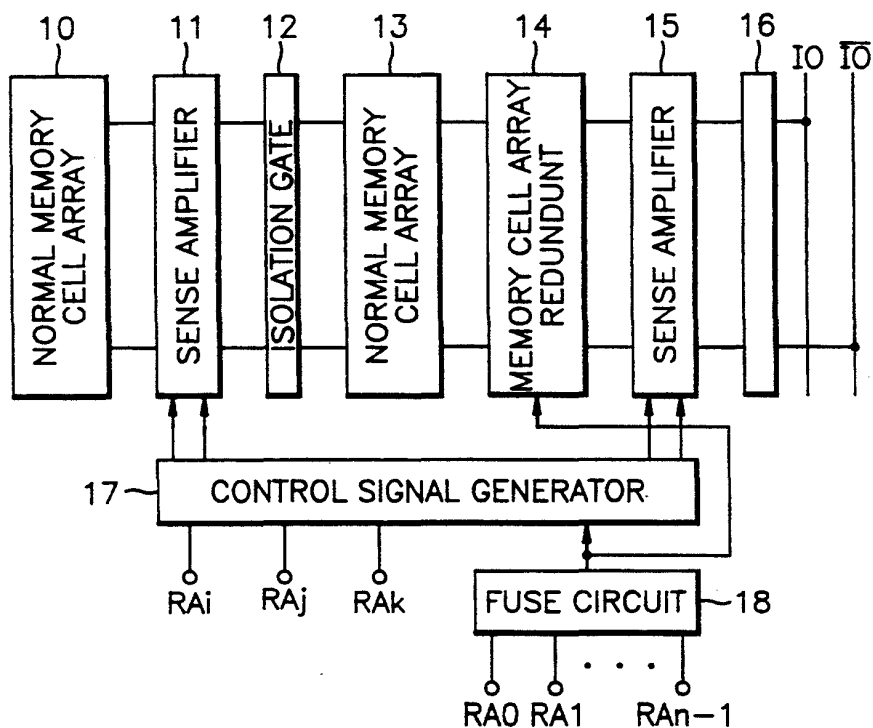




(PRIOR ART)  
FIG. 1



(PRIOR ART)  
*FIG. 2*



(PRIOR ART)  
FIG. 3

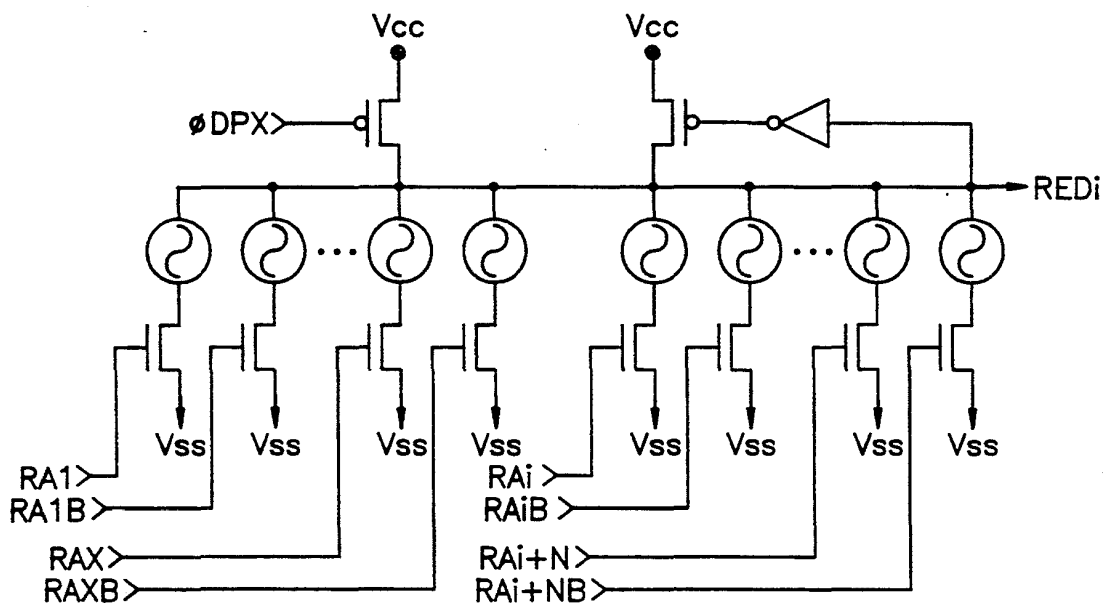


FIG. 5

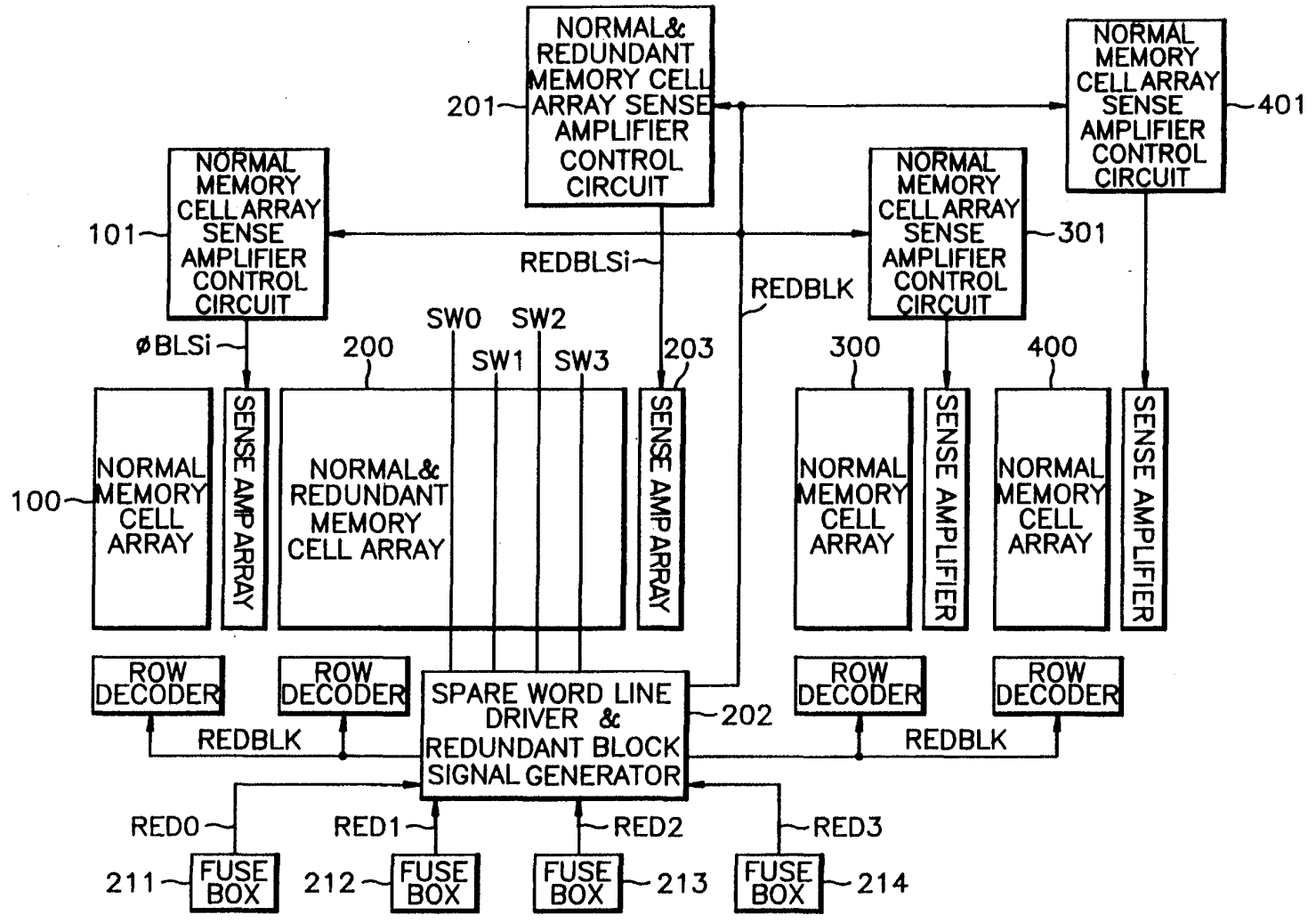


FIG. 4

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