R. JACOB (JAKE) BAKER, PH.D., P.E.



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SUMMARY

- Extensive leadership experience including:
 - Chair, Electrical and Computer Engineering Department, Boise State University;
 - o Dealing with conflict, problems, and limited resources;
 - Leading the department through ABET accreditation;
 - o Creation and implementation of both Master and Doctoral programs in ECE.
- Active scholar (h-index > 30 and an i10-index > 80) whose research is focused on:
 - High-speed interfaces for electro-optic, mixed-signal, and analog integrated circuits;
 - O Design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide);
 - o Analog and mixed-signal circuit techniques for nanometer CMOS; 3D packaging techniques
 - o The design of instrumentation for scientific research
 - o Delivery of circuit design education to off-campus students/engineers via the Internet.
- Mentor to:
 - Approximately 75 graduate students (major professor), <u>http://CMOSedu.com/jbaker/students/students.htm</u>
 - Electrical and Computer Engineering Department faculty;
 - o Engineers locally, nationally, and internationally;
 - o New and established companies.
- Inventor with 137 granted US patents
- Experienced integrated circuit designer and educator with significant industry experience. See additional information at http://cmosedu.com/jbaker/projects/fund.htm
- Textbook authorship and Internet contributions (see http://CMOSedu.com), that have helped tens of thousands of engineers around the world.
- Recognized by the IEEE Power Electronics Society with the Best Paper Award in 2000 (*IEEE Transactions on Power Electronics*) from PhD dissertation work.
- International known in the field of integrated circuit design, recipient of many honors including the Terman Award, the IEEE CAS Education Award, and IEEE Fellow.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas from August 2012 to present. From January 2000 to July 2012 held various positions at Boise State University including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the University of Idaho: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit design. Worked with multidisciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, and the Air Force Research Lab.
- Current research interests are:
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories
 - Analog and mixed-signal circuit design for communication systems, synchronization, energy storage, and data conversion
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
 - o Reconfigurable electronics design using nascent memory technologies
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Methods to deliver circuit design education to industry and off-campus students, see videos here
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college
 curriculum committee (chair), promotion and tenure committee, scholarly activities committee,
 faculty search committee, university level search committees, etc. Collaborate with College of
 Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

- **2013 present:** Working with Freedom Photonics and Attolo Engineering in the Santa Barbara area on the integration of optics with CMOS integrated circuits including Avalanche Photodiodes. Work has resulted, and should continue to result in, support via the SBIR and STTR programs.
- **2013 present:** Working with National Security Technologies, LLC,) on the Design of Integrated electrical/photonic application specific integrated circuit (ASIC) design.
- **2013 2015:** Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.
- **2010 2013:** Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.
- **2013:** Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.
- **2012:** Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, and infrared imaging systems.
- **2010 2012:** Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.
- **2009 2010:** Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.
- **2009 2010:** Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.
- 1994 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory using the MJT memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).
- **January 2008:** Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.
- **May 1997 May 1998:** Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips.
- **Summer 1998:** Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

- **Summers 1994 1995:** Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.
- **September October 1993:** Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.
- **Summer 1993:** Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.
- December 1985 June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.
- **Summer 1985:** Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble shooting electric motors on mining equipment.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services are listed below. I have been deposed eight times and given testimony at one trial.

Paul Hastings LLP (New York City, NY and Washington, DC)

Case – <u>Samsung, Inc.</u> v. Elbrus International Limited

Case Numbers - IPR2015-01523 and IPR2015-01524. Filed on June 26, 2015.

Case Subject Matter – High-speed, low-power data transfer.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for <u>SK hynix</u>, Inc. on matters relating to investigation of certain patents owned by Longitude Licensing Ltd.

Case Subject Matter – Semiconductor random access memory and communication interfaces.

Work Performed – Provided expert consulting services in 2015.

Ropes & Gray LLP (New York City, NY)

Case – <u>Samsung, Inc.</u> v. Imperium IP Holdings (Cayman), Ltd.

Case Number – IPR2015-01233. Filed on May 21, 2015.

Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – <u>Silergy Corporation</u> v. Monolithic Power Systems, Inc.

Case Numbers – IPR2015-00803 and IPR2015-00804. Filed on February 24, 2015.

Case Subject Matter – Microelectronic packaging.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Jones Day LLP (San Diego, CA)

Case – Micron Technology, Inc. v. eDigital Corp.

Case Number - IPR2015-00519. Filed on December 31, 2014.

Case Subject Matter – Methods for memory management in non-volatile flash memories.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (Atlanta, GA and Washington, DC)

Case – Micron Technology, Inc. v. MLC Intellectual Properties and BTG USA/International Inc.

Case Number - IPR2015-00504. Filed on December 24, 2014.

Case Subject Matter – Multi-level non-volatile floating gate memory, e.g. EPROM, EEPROM, and flash technologies.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Skadden, Arps, Slate, Meagher & Flom LLP & Affiliates (Palo Alto, CA)

Case – ALFRED T. GIULIANO, Chapter 7 Trustee of the Ritz Estate; CPM ELECTRONICS INC.; E.S.E. ELECTRONICS, INC. and MFLASH, INC., on Behalf of Themselves and All Others Similarly Situated v. <u>SanDisk Corp.</u>

Case Number – California, ND (Oakland) 4:10-cv-02787. Fourth amended complaint filed on September 24, 2014.

Case Subject Matter – Non-volatile semiconductor flash memory.

Work Performed – Provided expert consulting services.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Monolithic Power Systems v. Inc. Silergy Corporation

Case Number - California, ND 3:14-cv-01745. First amended complaint filed on July 7, 2014.

Case Subject Matter – Microelectronic packaging.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Ropes & Gray LLP (East Palo Alto, CA, New York City, NY, and Washington, DC)

Case – Macronix International Co., Ltd. v. <u>Spansion, Inc.</u>, <u>Aerohive Networks</u>, <u>Allied Telesis</u>, <u>Ciena</u>, <u>Delphi Automotive</u>, <u>Polycom</u>, <u>Ruckus Wireless</u>, <u>ShoreTel</u>, <u>Tellabs</u>, and <u>TiVo</u>

Case Number – ITC Investigation No. 337-TA-922. Complaint filed on June 27, 2014.

Case Subject Matter – Devices containing non-volatile memory and products containing the same.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, Markman tutorial, and expert report.

Ropes & Gray LLP (Boston, MA and New York City, NY)

Case – Imperium IP Holdings (Cayman), Ltd. v. Samsung, Inc.

Case Number – Texas, ED 4:14-cv-00371. Complaint filed on June 9, 2014.

Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Quinn Emanuel Urquhart & Sullivan, LLP (San Francisco, CA and Washington, DC)

Case – Freescale Semiconductor, Inc. v. *MediaTek, Inc.*, et. al.

Case Number – ITC Investigation No. 337-TA-920. Amended complaint filed on May 27, 2014.

Case Subject Matter – Semiconductor integrated circuits and devices containing the same.

Work Performed – Provided expert consulting services.

DLA Piper (East Palo Alto and San Diego, CA)

Case – GSI Technology, Inc. v. Cypress Semiconductor Corporation

Case Number – IPR2014-00419. Filed on February 7, 2014.

Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Ropes & Gray LLP (Washington, DC)

Case - Macronix International Co., Ltd. v. Spansion, Inc., et al.

Case Number – Virginia, ED 3:13-cv-00679. Complaint filed on November 20, 2013.

Case Subject Matter – Non-volatile semiconductor flash memory.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Cooley LLP (San Diego, CA)

Case – HSM Portfolio LLC and Technology Properties Limited LLC v. Fujitsu, AMD, *Qualcomm, Inc.*, Elpida, SK Hynix, Micron, ProMOS, SanDisk, Sony, ST Micro, Toshiba, ON, and Zoran

Case Number – Delaware, 1:11-cv-00770. Third amended complaint filed on June 28, 2013.

Case Subject Matter – Semiconductor sensing circuits.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto and San Diego, CA)

Case – Cypress Semiconductor Corporation v. GSI Technology, Inc.

Case Number – California, ND 3:13-cv-02013. Complaint filed on May 1, 2013.

Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Montgomery McCracken Walker & Rhoads LLP (Philadelphia, PA)

Case – Simon Nicholas Richmond v. Winchance Solar Fujian Technology, <u>Target</u>, <u>Creative Industries</u>, et. al.

Case Number – New Jersey, 3:13-cv-01954. Amended complaint filed on March 27, 2013.

Case Subject Matter – Circuitry including solar cells, re-chargeable batteries, energy conversion for solar lighting.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto, CA)

Case – Intellectual Ventures I/II LLC v. *Toshiba, Inc.*

Case Number – Delaware, 1:13-cv-00453. Complaint filed on March 20, 2013.

Case Subject Matter – Semiconductor memory and interface circuits.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Alston & Bird, DLA Piper, Gibson Dunn, Katten, O'Melveny, Orrick, and WilmerHale (various locations in the USA)

Case – Freescale v. <u>Funai</u>, <u>CSR</u>, <u>Zoran</u>, <u>MediaTek</u>, <u>Vizio</u>, <u>Sanyo</u>, <u>TPF</u>, <u>Top Victory Electronics</u>, <u>Envision</u> Peripherals, AmTRAN, and Marvell

Case Number – Texas, WD 1:12-cv-00644. Amended complaint filed on January 14, 2013.

Case Subject Matter – Semiconductor circuitry for voltage regulators, bus terminations, packaging, and signal processing.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, and Markman tutorial.

Amin, Turocy & Watson LLP (San Jose and San Francisco, CA)

Case - InvenSense, Inc. v. Robert Bosch GmbH

Case Subject Matter – Microelectromechanical systems (MEMS) sensor design and manufacture. Work Performed – Provided expert consulting services in 2013.

Morrison & Foerster LLP (Los Angeles, Palo Alto, and San Francisco, CA)

Case – STMicroelectronics, Inc. v. InvenSense, Inc.

Case Number – California, ND 3:12-cv-02475. Complaint filed on May 16, 2012.

Case Subject Matter – Microelectromechanical systems (MEMS) sensors including Gyroscopes and accelerometers.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for <u>SK hynix</u>, Inc. on matters relating to investigation of certain patents owned by Round Rock Research LLC

Case Subject Matter – Semiconductor random access memory.

Work Performed – Provided expert consulting services in 2012.

Keker & Van Nest LLP (San Francisco, CA)

Case – Round Rock Research LLC v. SanDisk Corp.

Case Number – Delaware, 1:12-cv-00569. Complaint filed on May 3, 2012.

Case Subject Matter – Semiconductor non-volatile flash memory.

Work Performed – Provided expert consulting including: invalidity analysis, non-infringement analysis, expert reports, and was deposed.

Perkins Coie LLP (San Diego, CA)

Case – ASUS Computer International v. Round Rock Research LLC

Case Number – California, ND 3:12-cv-02099. Complaint filed on April 26, 2012.

Case Subject Matter – Semiconductor memory and image sensors.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, expert reports, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Dr. Michael Jaffe' as insolvency administrator for Qimonda AG v. LSI, <u>Atmel Corp</u>, Cypress, MagnaChip, and ON Semiconductor

Case Number – California, ND 3:12-cv-03166. Complaint filed on January 10, 2012.

Case Subject Matter – Semiconductor processing and manufacturing.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Useful Arts IP (Cupertino, CA)

Case – Tezzaron (formerly Tachyon Semiconductor) v. Elm Technology Corporation

Case Number – Patent Interference No. 105,859. Declared on December 1, 2011.

Case Subject Matter – Packaging of semiconductors and through semiconductor vias.

Work Performed – Patent interference, wrote declaration, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Nanya Technology Corporation v. *Elpida Memory, Inc. and Kingston Technology Company, Inc.*

Case Number – ITC Investigation No. 337-TA-821. Complaint filed on November 21, 2011.

Case Subject Matter – Semiconductor DRAM design and manufacture.

Work Performed – Provided expert consulting and reports on validity, infringement, and domestic industry. Also provided declarations and was deposed.

Morgan, Lewis & Bockius LLP (Washington, DC)

Case – Elpida Memory, Inc. v. Nanya Technology Corporation

Case Number – ITC Investigation No. 337-TA-819. Complaint filed on November 15, 2011.

Case Subject Matter – Semiconductor DRAM design and manufacture.

Work Performed – Provided expert consulting and reports on infringement, domestic industry, and validity. Also provided Markman tutorial, declarations, deposition, and testimony at the trial.

Ropes & Gray LLP (New York City, NY)

Case – Intellectual Ventures v. Sendai Nikon Corporation

Case Number - Delaware, 1:11-cv-01025. Complaint filed on October 26. 2011.

Case Subject Matter – Image sensor design and manufacture.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Farella Braun + Martel LLP (San Francisco, CA)

Case - Round Rock Research LLC v. Dell, Inc.

Case Number - Delaware, 1:11-cv-00976. Complaint filed on October 14, 2011.

Case Subject Matter – Semiconductor DRAM design and manufacture.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Latham & Watkins LLP (San Francisco, CA)

Case – Altera Corp. v. *LSI Corp. and Agere Systems, Inc.*

Case Number – California, ND 4:11-cv-03139. Complaint filed on June 24, 2011.

Case Subject Matter – Semiconductor devices including phase-locked loops and clock recovery circuits.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Fish & Richardson P.C. (Washington, DC)

Case – Spansion LLC v. <u>Samsung Electronics Co., Ltd.</u>, Apple, Inc., Nokia Corp., PNY Technologies, Inc. Research In Motion Corporation, Transcend Information Inc.

Case Number – ITC Investigation No. 337-TA-735. Complaint filed on August 6, 2010.

Case Subject Matter – Semiconductor flash memory manufacture and design.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Jones Day LLP (Palo Alto, CA)

Case – LSI and Agere, Inc. v. Xilinx, Inc.

Case Number – New York, SD 1:09-cv-09719. Complaint filed on November 23, 2009.

Case Subject Matter – Semiconductor digital design and clocking.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Morrison & Foerster LLP (New York City, NY)

Case – Innurvation, Inc. et al v. *Fujitsu Microelectronics America, Inc.*, Sony Corporation of America, Toshiba America Electronics Components, Inc., and Freescale Semiconductor, Inc.

Case Number – Maryland, 1:09-cv-01416. Complaint filed on May 29, 2009.

Case Subject Matter – Semiconductor circuit layout.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Wilson Sonsini Goodrich & Rosati P.C. (Palo Alto, CA)

Case – Panavision Imaging, LLC, v. <u>OmniVision Technologies, Inc.</u>, Canon U.S.A., Inc., Micron Technology, Inc., Aptina Imaging Corporation, and Aptina, LLC.

Case Number – California, CD 2:09-cv-01577. Complaint filed on March 6, 2009.

Case Subject Matter – CMOS image sensor design and manufacture.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and wrote declaration.

McDermott Will & Emery (Menlo Park, CA)

Case – Volterra Semiconductor Corp. v. Primarion <u>& Infineon Technologies North America &</u> Infineon Technologies, A.G.

Case Number – California, ND 3:08-cv-05129. Complaint filed on November 12, 2008.

Case Subject Matter – High-performance analog and mixed-signal power management semiconductors.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and was deposed.

pre-2008 Miscellaneous minor expert witness work, was deposed twice.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013) Member of the honor societies Eta Kappa Nu and Tau Beta Pi Licensed Professional Engineer

HONORS AND AWARDS

- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013 2015
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2013 2014
- IEEE Circuits and Systems (CAS) Education Award 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education 2007
- President's Research and Scholarship Award, Boise State University 2005
- Honored Faculty Member Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee

(2011-present), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as the Technology Editor (2012-2014) and Editor-in-Chief (2015 - present) for the *IEEE Solid-State Circuits Magazine*, as a Distinguished Lecturer for the SSCS (2013-2014), and as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015.

ARMED FORCES

6 years United States Marine Corps reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge, October 23, 1987

TEXTBOOKS AUTHORED

- Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition" *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) **Over 50,000 copies of this book's three editions in print.**
- Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)
- Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", Wiley-IEEE, 2008, 201 pages. ISBN: 978-0-470-18475-2
- Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", Wiley-IEEE, 2001, 201 pages. ISBN 0-7803-6014-1
- Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

BOOKS, OTHER (edited, chapters, etc.)

- Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.
- Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)
- Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 1999. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)
- Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 1999. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

INVITED TALKS AND SEMINARS

Have given invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICySSS keynote, IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National

Laboratory, Lehigh University, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2015) "Radiation Hardened Optoelectronics for Optical Interconnects," Electronics Defense Threat Reduction Agency (DTRA), \$45,000 submitted for funding
- Baker, R. Jacob, (2015) "Low Light Short Wave Infrared Focal Plane Arrays," Missile Defense Agency (MDA), \$44,999 submitted for funding
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